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(54) Electronic equipment

(57) It is an object of the present invention to provide a technology for realising new high performance portable electronic equipment featuring small size, low cost, and low power consumption especially in relation to configuration of an antenna as well as to configuration of a receiving circuit and a signal decoding circuit in the field of portable electronic equipment for modifying clock display or displaying a message by receiving electric means.

An electronic equipment according to the present invention solves the problems as described above by employing a Hall effect device (5007) with a ferromagnetic body (5003, 5005) adjacent thereto as an antenna.

FIG. 1A

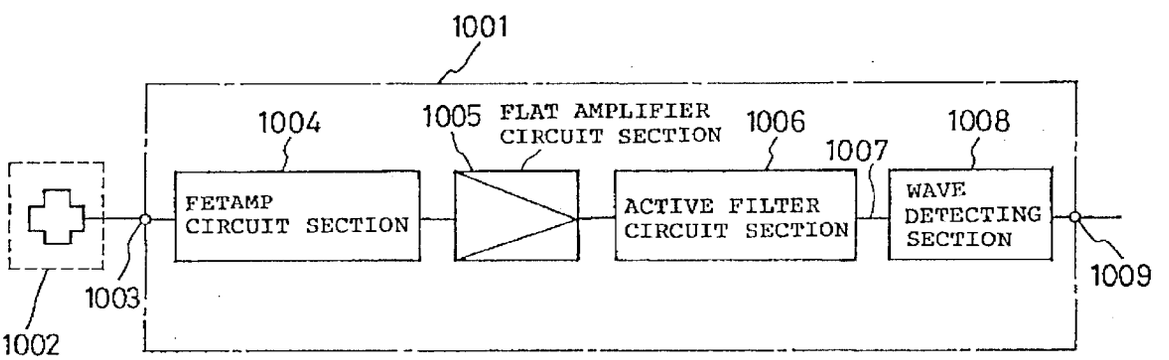

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FIG. 1B 

FIG. 1C 

Description

The present invention provides a technology for realising new high performance portable electronic equipment featuring small size, low cost, and low power consumption.

Fig. 20A is a view showing external appearance of a wrist watch based on an analog pointer which is a conventional type of electric wave clock (generic name of clocks and electronic equipment having a function to receive an electronic wave indicating a standard time to correct a time display).

This figure shows a state where a conventional type of coil antenna 17003 based on a ferrite bar system is accommodated in a non-metallic antenna case (housing) 17001 placed in an upper section of a dial plate.

Fig. 20B is a view showing appearance of a coil antenna based on the ferrite bar system in the conventional type of electric wave clock. This figure shows a state where coil winding 17005 is wound around a ferrite bar (core) 17006 by several hundred turns. An outer diameter 17004 of the coil winding is in a range from several millimeters up to 10 mm Ø, and a length 17007 of the ferrite bar is in a range from 1 cm at the shortest up to several centimetres at the longest Fig. 20C is a cross-sectional view of the conventional type of coil antenna based on a ferrite bar system described above.

In this figure, designated at the reference numeral 17008 is a dimension of an outer diameter of the coil winding, at 17009 a dimension of a diameter of the ferrite bar, at 17010 the ferrite bar, at 17014 a dimension of the ferrite bar in the longitudinal direction, at 17011 a dimension of the ferrite bar in the longitudinal direction with the coil winding 17012 wound therearound and at 17013 effect of state of passing magnetic flux through change in a magnetic field caused by an electric wave.

Fig. 21 is a system block diagram showing a receiving circuit of a conventional type of electric wave clock. A coil (L element and inductance element) 18005 in an antenna section 18004 comprises a capacitor (C element) 18006 and an L/C resonance circuit, takes out change in a magnetic field caused by an electric wave as an electric power, and sends a signal via a power amplifying circuit section 18001 and a tuning circuit section 18002 in the downstream side therefrom to a signal processing circuit in the further downstream side therefrom, and herein the tuning circuit section has generally a reference oscillation circuit section 18003 and is based on the heterodine configuration.

In the conventional technology in this art, generally the configuration as described above is employed, so that there are problems as described below.

Firstly, the type of antenna is based on a magnetic field to power conversion system using a coil winding antenna, and to secure a certain degree of sensitivity (such as, for instance, a radius of 500 km in case of JG2AS, 40 kHz, and 1 kw transmission), a certain cross-sectional area decided by a diameter 17009 of the ferrite bar shown in Fig. 20C is required against the passing magnetic flux 17013 shown in Fig. 20C, and at the same time the number of turns of the coil winding must be several hundred turns (at least 200 turns).

Length 17014 of the ferrite bar shown in Fig. 20C itself is not an important parameter. Herein as described above, this type of antenna is based on a conversion system from a magnetic field to an electric power, and the impedance decided by the total number of turns of the coil winding can not be so large, which means that a diameter of the coil winding can not be so small. For this reason, in a case where a dimension 17011 of a total length of the coil winding in Fig. 20C is short, then an outer diameter 17008 of the coil winding in Fig. 20c becomes larger. In the current state of art, in the state as shown in Fig. 20B, there is no way but to employ the minimum dimensional configuration in which a dimension of a length 17007 of a ferrite bar is around 2 cm, a dimension of an outer diameter 17004 of the coil winding is around 5 mm. So required is a section such as a casing 17001 for an antenna section as shown in Fig. 20A (also in this case, metal can not be used because it gives a shielding effect to a magnetic field, and there is no way but to use such materials as plastic or ceramics), and in a case of a wrist watch, there are strict disadvantageous restrictions in design and adaptability as commercial products because of the volume ratio against a basic system of a watch.

Secondly, as described above, as power amplification and heterodyne tuning are employed, the circuit scale becomes substantially large, which causes not only cost increase, but also increase in power consumption.

In a first aspect, this invention provides electronic equipment comprising:

an antenna;
a receiving circuit with functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a clock display; and characterised in that;
said antenna comprises a semiconductor device having the magnetic Hall effect and said semiconductor device has a ferromagnetic body adjacent thereto.

In a second aspect, this invention provides electronic equipment comprising:

an antenna;
a receiving circuit having functions to amplify, differentiate and detect an electric wave received by said antenna, and characterised in that;
said receiving circuit has a differential amplifier comprising a MOS transistor, has a comparator comprising a MOS transistor in succession to said differential amplifier, and also has an electric charge container comprising a MOS transistor provided in

parallel to said comparator.

In a third aspect, this invention provides electronic equipment comprising:

an antenna;
a receiving circuit having the functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a decoding circuit having a function to decode a coded signal superimposed to said electric wave, and characterised in that;
said receiving circuit has a differential amplifier comprising a MOS transistor, has a comparator comprising a MOS transistor in succession to said differential amplifier, and also has an electric charge container comprising a MOS transistor provided in parallel to said comparator.

Alternatively, the differential amplifier, comparator and electric change container can form part of the decoding circuit.

In a fourth aspect, this invention provides electronic equipment comprising:

an antenna;
a receiving circuit with functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a clock display function, and characterised in that;
said antenna has a semiconductor device having the magnetic reluctance effect, and a plurality of said semiconductors are electrically connected to each other in series.

Thus firstly, a Hall element is used in place of a winding coil in the antenna section.

Secondly, a Hall element is used as an antenna as described above, as a receiving circuit, and in place of the conventional type of system comprising the steps of taking out an electric power, amplifying the electric power, and then tuning the power, there is employed a circuit means comprising the steps of detecting a change in a magnetic field, detecting change in reluctance (Hall effect), detecting change in a voltage, taking out the voltage change, amplifying the voltage change, and filtering the amplified voltage (active filter).

Thirdly, a charge amplifier is used for amplifying voltage change, and further a receiving circuit is used in which tuning is executed with an analog filter (FIR) comprising an analog memory (sample-and-hold) having a circulating type of shift register and a comparator.

Fourthly, a charge amplifier for amplifying voltage change is used in a decode circuit for decoding signals superimposed on electric waves, and decoding is executed by the analog filter comprising an analog memory (sample-and-hold) having a circulating type of shift register and a comparator.

Fifthly, the antenna section comprises magnetic reluctance elements.

Other objects and features of this invention will become understood from the following description with reference to the accompanying drawings.

Embodiments of the invention will now be described by way of example only, with reference to the accompanying diagrammatic figures, in which:

Fig. 1A is a system block diagram showing a Hall element antenna and a receiving circuit according to Embodiment 1 of the present invention;
Fig. 1B is a view showing a signal waveform at the node 1 1007 in Fig. 1A;
Fig. 1C is a view showing a signal waveform at the output terminal 1009 in Fig. 1A;
Fig. 2 is a detailed circuit diagram showing the Hall element antenna and the receiving circuit according to Embodiment 1 of the present invention;
Fig. 3A and Fig. 3B are a simulated views for illustrating operations of the Hall element in Embodiment 1 of the present invention and a graph showing electric characteristics thereof;
Fig. 4 is a time code waveform for an electric wave for the standard time (in Japan) in Embodiment 1 of the present invention;
Fig. 5A is a view showing external appearance of a wrist watch based on an analog pointer system for an electric wave clock realised by using the Hall element antenna and the receiving circuit according to Embodiment 1 of the present invention;
Fig. 5B is a view showing external appearance of the Hall element antenna section in Embodiment 1 of the present invention;
Fig. 5C is a cross-sectional view showing the Hall element antenna section in Embodiment 1 of the present invention;
Fig 6 is a system block diagram showing a receiving circuit for an electric wave clock according to Embodiment 2 of the present invention;
Fig. 7 is a circuit diagram showing a charge amplifier circuit section in an analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;
Fig. 8 is a circuit diagram showing a comparator circuit section in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;
Fig. 9 is a simulated view showing a situation of waveform computing for 1 bit in the sample-and-hold circuit in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;
Fig. 10 is a circuit diagram showing the sample-and-hold (analog memory) circuit section in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;
Fig. 11 is a detailed circuit diagram for 1 bit in the

sample-and-hold circuit section in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;

Fig. 12 is a circuit diagram showing the buffer circuit section in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;

Fig. 13 is a graph showing an FM multiplex broadcast base-band spectrum for illustrating a receiving circuit for a receptor and a decoder circuit according to Embodiment 3 of the present invention;

Fig. 14 is a system block diagram for illustrating a receiving circuit for a receptor according to Embodiment 3 of the present invention;

Fig. 15 is a system block diagram showing a subcarrier decoding circuit for a receptor according to Embodiment 3 of the present invention;

Fig. 16A is a view showing external appearance of an MR element used in electronic equipment according to Embodiment 4 of the present invention;

Fig. 16B is a graph showing characteristics of an MR element used in electronic equipment according to Embodiment 4 of the present invention;

Fig. 16C is a block diagram showing a receiving circuit in the initial stage in a case where the MR element according to Embodiment 4 of the present invention is used in an antenna;

Fig. 17 is a circuit diagram showing an analog amplifier-and-filter circuit for the receiving circuit according to Embodiment 1 of the present invention;

Fig. 18 is a circuit diagram in which the analog amplifier-and-filter circuit for a receiving circuit according to Embodiment 1 of the present invention comprises a CMOS inverter;

Fig. 19 is a circuit diagram showing a comparator circuit section in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention;

Fig. 20A is a view showing external appearance of a wrist watch based on an analog pointer system for the conventional type of electric wave clock; Fig. 20B is a view showing external appearance of a coil antenna based on a ferrite bar system in an electric waveform based on the conventional technology;

Fig. 20C is a cross-sectional view showing the coil antenna based on the ferrite bar system described above; and

Fig. 21 is a system block diagram showing a receiving circuit in an electric wave clock based on the conventional technology.

Fig. 1A is a system block diagram showing a Hall element antenna and a receiving circuit 1001 in Embodiment 1 of the present invention. In this figure, designated at the reference numeral 1002 is a Hall element antenna according to the present invention, at 1003 an input terminal, at 1004 an FET amplifier (AMP) circuit section (where the power is amplified by around 30 dB), at 1005 a flat amplifier circuit section (where the power is further amplified by around 30 dB), at 1006 an active filter circuit section (where the power is further amplified by around 20 to 25 dB. For this reason, in this system, the total amplification factor is around 85 dB. The selectivity; Q = 10 to 30, at 1007 a node 1, at 1008 a wave detecting section (for detecting, biasing, and rectifying electric waves), at 1009 an output terminal.

Fig. 1B shows a signal waveform at the node 1 1007 in Fig. 1A.

Fig. 1C shows a signal waveform at the output terminal 1009 in Fig. 1A. As an electric wave for standard time in Japan, JG2AS is transmitted from Nazaki Transmission Center in Miwa-Machi, Ibaraki Prefecture with the frequency of 40 kHz and a power of 1 kw. The signal format is described in detail later, but is based on coding processing with ASK coding (Amplitude Shift Keying) . Accordingly, the signal as shown in Fig. 1B is required to be transmitted with a rectangular wave as shown in Fig. 1C in the final stage. Logically, the signal is used after being inverted once by an inverter.

Fig. 2 is a detailed circuit diagram showing the Hall element antenna and a receiving circuit 2001 (equivalent to the receiving circuit 1001 in Fig. 1A) in Embodiment 1 of the present invention. This circuit comprises a Hall element antenna section 2016 with constant current bias 2003 added to the Hall element therein; an input terminal 2017 connected to the Hall element; an FET amplifier (AMP) circuit 2019 (equivalent to the circuit 1004 in Fig. 1) in which a resistor 2018; a JFET (junction, J; FET) 2020 and a constant current bias 2004 having a same value as that of a constant current bias added to the Hall element are connected to each other as shown in the figure; a flat amplifier (AMP) circuit section 2005 (equivalent to the section 1005 in Fig. 1) in which a serial capacitance (coupling capacitance, a coupling capacitor) 2021, an NPN transistor 2022, a resistor 2011, a resistor 2012, and a resistor 2013 are connected as shown in the figure; an active filter circuit section 2002 (equivalent to the section 1006 in Fig. 1A)) in which a serial capacitance (coupling capacitance), an NPN transistor 2025, a resistor 2026, a resistor 2027, a resistor 2028, a capacitance 2007, a capacitance 2008, and a resistor 2014 are connected as shown in the figure; a wave detecting circuit section (for detecting, biasing, and rectifying waveforms) 2010 (equivalent to the section 1008 in Fig. 1A) in which a serial capacitance 2015, a diode 2029, a resistor 2030, a capacitance 2031, an NPN transistor 2032, and a resistor 2033 are connected as shown in the figure; an output terminal 2034; a Vdd terminal 2035; and a GND terminal 2036. In the figure, a capacitance 2023 is provided between the Vdd 2006 and GND. The reference numeral 2024 indicates a serial capacitance.

Fig. 17 is a detailed circuit diagram showing a case where the flat amplifier circuit section 2005 and the active filter circuit section 2002 in Embodiment 1 of the present invention as shown in Fig. 2 are realised with another configuration.

In this figure, an input terminal 19007 to which output from the FET amplifier circuit section 2019 shown in Fig. 2 is inputted; an amplifier circuit section 19001 in which a serial capacitance (1000pF) 19011, a resistor (1MΩ) 19012, a resistor (4.7 KΩ) 19013, a resistor (15 KΩ) 19014, and an NPN transistor 19015 are connected as shown in the figure; an active filter circuit section 19002 in which a serial capacitance (1000 pF) 19016, a resistor (27 KΩ) 19017, a resistor (27 KΩ) 19018, a resistor (15 KΩ) 19020, a resistor (13 KΩ) 19023, a capacitance (300 pF) 19019, a capacitance (150 pF) 19022, a capacitance (150 pF) 19024, and an NPN transistor 19021 are connected as shown in the figure; a crystal filter section 19003 in which a serial capacitance (1000 pF) 19025, and a crystal filter (with the oscillation frequency of 40 kHz) 19026 are connected as shown in the figure, an amplifier circuit section 19004 in which a resistor (2.7 MΩ) 19027, a resistor (15 KΩ) 19028, and an NPN transistor 19029 are connected as shown in the figure; an amplifier circuit section 19005 in which a serial capacitance (1000 pF) 19030, a resistor (1.7 MΩ) 19031, a resistor (15 KΩ) 19032, a resistor (13 KΩ) 19034, and an NPN transistor 19033 are connected as shown in the figure; and an output terminal 19008 for outputting a signal to the wave detecting circuit 2010 in Fig. 2 are connected to each other.

With the configuration as described above, noises are cut off to some extent by the active noise filter circuit section 19002, and noises are further cut off by the crystal filter section 19003, so that a signal with few noises can be outputted to the wave detecting circuit.

Fig. 18 is a detailed circuit diagram showing a case where the flat amplifier circuit section 2005 and the active filter circuit section 2002 in Embodiment 1 of the present invention as shown in Fig. 2 are realised with a CMOS inverter respectively.

In the circuit, an input terminal 20010 to which output from the FET amplifier circuit section 2019 shown in Fig. 2 is inputted; an amplifier circuit section 20001 in which a serial capacitance (1000 pF) 20011, an HC type of unbuffer type CMOS inverter 20012, and a resistor (1 MΩ) 20013 are connected as shown in the figure; an active filter circuit section 20002 in which a serial capacitance (1000 pF) 20014, a capacitance (300 pF) 20018, a capacitance (150 pF) 20020, a capacitance (150 pF) 20022, a resistor (4.7 KΩ) 20015, a resistor (27 KΩ) 20016, a resistor (27 KΩ) 20017, a resistor (13 KΩ) 20021, an HC type of unbuffered type CMOS inverter 20019 are connected as shown in the figure; a crystal filter 20003 resonating at 40 kHz, an amplifier circuit 20004 in which an HC type of unbuffered CMOS inverter 20024, the same type of CMOS inverter 20026, a resistor (1 MΩ) 20023, and a resistor (4.7 KΩ) 20025 are connected to each other as shown in the figure; and an output terminal 20027 which outputs a signal to the wave detecting circuit section 2010 in Fig. 2 are connected as shown in the figure.

It should be noted that a power source for each CMOS inverter is connected to the Vdd terminal 2035 in Fig. 2.

With the configuration as described above, as CMOS inverters are used in this configuration, power consumption is low, and further as noises are cut off to some extent in the active filter circuit section and are further cut off in the crystal filter, an output signal with low noise can be outputted to the wave detecting circuit.

It is needless to say that the receiving circuit 2001 in Embodiment 1 described above can effectively receive signals also from a coil antenna, and that an amplifier circuit section may be added to each section and an amplifier section in each section may be removed according to an output signal level from the Hall element antenna or the coil antenna, or an input signal level required for the wave detecting circuit.

Fig. 3A and Fig. 3B are a simulated view (a) for illustrating operation of the Hall element in Embodiment 1 of the present invention and a graph (b) showing the electric characteristics thereof respectively.

The Hall element obtains a voltage which appears at a terminal crossing a bias current Ic at right angles when the bias current Ic as shown in the figure is flowing through a semiconductor pellet 3003 made of such a material as InSb (indium/antimony), GaAs (gallium/arsenic) or Si (Silicon), and when a magnetic flux B 3002 is loaded in the positional relation as shown in the figure, namely a Hall voltage V_H, and the Hall voltage V_H increases in proportion to the magnetic flux density B and also increases in proportion to the bias current Ic. This is because a reluctance (factor) of a Hall element (semiconductor) changes according to magnetic flux density B. In this embodiment, the reluctance change (Hall effect) is converted to a voltage change signal by the circuit configuration in the Hall element antenna section 2016 in Fig. 2 as well as by the resistor 2018, then the voltage (it may be called transimpedance herein) is once amplified in the FET 2020 and then changed into a differential signal by the serial capacitance 2021 and further amplified, and then signal selection (tuning) is executed in the active filter circuit section 2002. Thcn wave detection and wave rectification are executed. What is important herein is that, in contrast to the fact that an L/C resonance circuit formed with an antenna based on a winding coil based on the conventional technology as described above makes use of a resonance frequency according to L/C elements (selectivity), the Hall element according to the present invention makes use of the attenuation characteristics (up to around 100 kHz) of a response speed against change of a magnetic field in the Hall element.

Fig. 4 is a time code waveform of an electric wave for the standard time (in Japan) in Embodiment 1 of the present invention. As described above, JG2AS is an ASK coded signal with the frequency of 40 kHz, but the signal as one cycle is 1 sec, and as a code a signal for 1 is 0.5 sec, and a signal for 0 is 0.8 sec, and a signal for P is 0.2 sec each for coding. Information on minute,

hour, and days is transmitted as a combination of these signals for 1, 0, and P. In Japan, a frequency of the clock signal is 40 kHz, but the frequency is 77.5 kHz in Germany, and 60.0 kHz in England, but in the present invention, only some of constants for the active filter circuit section are required to be selectable, and there is no need for changing constants for the antenna section itself like in the L/C resonance type of antenna, which means that the Hall element antenna is more excellent as compared to the L/C resonance type of antenna. The processing system for coding for 1, 0 and P varies from country to country, but it is needless to say that the means with a digital circuit using a microcomputer (CPU) in a section after the wave detecting circuit section can quite easily to allow for variations in coding.

Fig. 5A is a view showing external appearance of a wrist watch 5002 based on the analog pointer system for an electric wave clock realised with the Hall element antenna and receiving circuit in Embodiment 1 of the present invention.

Fig. 5B is a view showing external appearance of the Hall element antenna section in Embodiment 1 of the present invention, This section is accommodated in the antenna case section 5001 shown in Fig. 5A. As described above, though not shown in the electric circuit, practically ferrite (or other ferromagnetic body) disks 5003, 5005 each having a diameter 5006 of several millimetres are stacked at both sides of the Hall element 5007, and the thickness 5004 is several millimetres.

Fig. 5C is a cross-sectional view showing a portion of the Hall element antenna section according to Embodiment 1 of the present invention. An area of the cross section decided by a diameter 5008 of a ferrite disk 5009 through which a magnetic flux 5013 passes decides the sensitivity, so that a diameter 5008 of several millimetres is enough, and at the same time the length does not increase like in a coil antenna (for the reasons as described above), and also the thickness of the antenna as a whole is within several millimetres. Accordingly, as shown by the wrist watch shown in Fig. 5A as an example thereof, it is understood that restrictions in designing are largely reduced as compared with those in the conventional technology because a volume ratio of the antenna section against a total volume of a watch as a whole can substantially be reduced.

It has become possible to substantially reduce restrictions in designing as well as in adaptability for products to be sold to consumers because problems causing troubles in practical operations seldom occur even if the Hall element antenna is accommodated not in the section like that shown in Fig. 5A, but in other sections. In this figure, designated at the reference numeral 5012 is a ferrite disk, at 5011 a Hall element chip (pellet), and at 5010 a housing case (package) for the Hall element.

Fig. 6 is a system block diagram showing a receiving circuit 6001 for an electric wave clock according to Embodiment 2 of the present invention. The reference numeral 6018 indicates a block diagram showing a charge amplifier (for amplifying signals) in the receiving circuit and a signal identifying circuit according to Embodiment 2 of the present invention. This circuit includes base-grounded type initial stage amplifying circuit section 6009 connected to the antenna 6003 in which a resistor 6008, a capacitance 6007, a resistor 6006, an NPN transistor 6004, and a resistor 6005 are connected as shown in the figure; a charge amplifying (signal amplification) and signal identifying (selection (tuning) to filtering) circuit block (analog amplifier-and-filter circuit) 6018 having the configuration in which a coupling capacitance 6010, a charge integration amplifier [charge amplifier, gmn = 3 ms (Siemens). This symbol is hereinafter called a charge amplifier in the present specification] 6012, a feedback capacitance (0.2 pF) 6011, a switch element (Although this type of switch symbol is used for simplifying description of the system, actually a transmission gate comprising a MOS transistor is used) 6002, a feedback capacitance 6015, a switch element 6014, a charge amplifier (x 10-times amplifier) 6016, a coupling capacitance (2.0 pF) 6013, a comparator circuit section 6019, a shift register circuit section (8 stages) 6021, a 40 kHz clock circuit section (It is recommended that the clock circuit section has the configuration in which a frequency can be switched according to an area such as, for instance, Japan or Germany) 6017, a sample-and-hold (analog memory) circuit section 6023, an output control circuit section 6025, and a buffer circuit 6028 are connected to each other by, in addition to the regular signal lines through which received signals flow, hit signal lines 6020 and 6027, a reset signal line 6022, output instruction signal lines 6026 and 6029, and a clock signal line 6024 as shown in the figure; a wave detecting circuit section (Refer to Embodiment 1) 6030; a Cs (Chip Select; for receiving an instruction of "Operate", for instance, from a microcomputer or the like in the downstream therefrom) terminal 6031; a read (for alerting that "a signal to be read has come" to a microcomputer or the like in the downstream therefrom) terminal 6032, and a Vout output terminal 6033. In the antenna section, both the conventional type of coil antenna as shown in the figure and the analog amplifier-and-filter circuit according to Embodiment 2 operate effectively, and also a combination of the Hall element antenna according to Embodiment 1 therewith is effective. In this case, as described above, a receiving circuit with lower power consumption can be realised by matching to the selectivity characteristics in the Hall element antenna.

Fig. 7 is a circuit diagram showing a charge amplifier circuit section 7002 (equivalent to thc circuits 6012, 6016 in Fig. 6, circuits 8009, 8011 in Fig. 8, circuit 12004 in Fig. 12, and circuits 15012, 15014 in Fig. 15) in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention. The circuit has a Vdd terminal 7001 as well as the configuration in which a P-channel type of MOS transistor (PMOS) 7004, a PMOS 7003, an N-channel type of MOS transistor (NMOS)

7006, an NMOS 7005, and an NMOS 7009 are connected to each other as shown in the figure, and also the circuit has a GND terminal 7010 and a Vref input terminal 7011 as well as the configuration in which a Vref voltage 7013 is connected to the Vref input terminal in the state where a depression type of NMOS 7012 and an enhancement type of NMOS 7014 are connected to a differential amplifier comprising a signal input terminal 7007. The reference numeral 7008 indicates an output terminal.

Fig. 8 is a circuit diagram showing a comparator circuit 8001 (equivalent to the circuit 6019 in Fig. 6 and the circuit 15004 in Fig. 15) in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention. This comparator circuit section 8001 has an input terminal 8007 as well as the configuration in which a coupling capacitance (0.2 to 1.4 pF) 8008, a charge amplifier 8009, a feedback capacitance (0.2 pF) 8005, a switch element 8003, a switch element 8004, a reset signal line 8002 working on the switch elements, a feedback capacitance (0.2 pF) 8006, a coupling capacitance (1.0 pF) 8010, a charge amplifier 8011, a trigate inverter (INV1, Vth < Vdd/2) 8012, a trigate inverter (INV2, Vth > Vdd/2) 8013, an inverter 8014, and an exclusive OR (EOR) circuit 8015 are connected as shown in the figure, and the comparator circuit section 8001 also has an output signal terminal (hit signal output) 8016. For this reason, the comparator circuit section operates in synchronism to the 40 kHz clock, determines a significant signal which is not noise, and outputs a hit signal.

Fig. 19 is a detailed circuit diagram showing a case where a sample hold signal input terminal 21001 for receiving a sample hold signal input 21002 and a switch element 21003 operating in synchronism to the sample hold signal are added to the comparator circuit section 8001 in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention as shown in Fig. 8.

Fig. 10 is a circuit diagram showing a sample-and-hold (analog memory) circuit section 10003 (equivalent to the circuit 6023 in Fig. 6 and to the circuit 15015 in Fig. 15) in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention. This sample-and-hold circuit section 10003 has a signal input terminal 10001 as well as the configuration in which a plurality (8 stages herein) of Write switch elements (Write for signal write) 10002, a capacitor 10004 for storing and maintaining a plurality of data (analog values), a plurality of SEL switch elements (SEL: Select for signal read or output) 10006, a Write address line 10005, a SEL address line 10007, a circulating type of (free-run) shift register (8 stages). (The number of stages should be increased more for higher data resolution) 10009 are connected as shown in the figure, and the sample-and-hold circuit 10003 also has a signal output terminal 10008, a SEL signal input terminal 10011, and a clock signal input terminal 10010.

An analog signal waveform from the charge amplifier 6016 inputted into the sample-and-hold circuit 10003 simultaneously when is inputted into the comparator circuit 6019, a hit signal determined as a significant signal by the comparator circuit section is inputted into the shift register circuit section 6021 and then into the output control circuit section 6025, and a memorised analog signal is outputted from the output terminal 10008.

Fig. 11 is a detailed circuit diagram for 1 bit in the sample-and-hold circuit section 10003 in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention. In this figure, designated at the reference numeral 11034 is an input signal, at 11013 a switch element, at 11012 a switch element, at 11016 a PMOS, at 11014 a Write address line, at 11015 a capacitance (1.0 pF), at 11026 a switch element, at 11027 a PMOS, at 11017 an NMOS, at 11019 an NMOS, at 11025 an OUT-A output (current) terminal, at 11028 an NMOS, at 11029 an NNOS, at 11033 an OUT-A output (current) terminal, at 11022 a SEL signal input, at 11023 an OUT-A address signal input, at 11024 an OUT-B address signal input, at 11018 a switch element, at 11020 a switch element, at 11021 a SEL-A signal line, at 11030 a switch element, at 11032 a switch element, at 11031 a SEL-B signal line, at 11035 and 11036 an AND circuit respectively.

Fig. 9 is a simulated view showing waveform computing for 1 bit in the sample-and-hold circuit 10003 in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention. Now assuming that two samples 9003, 9004 closest to a sample (data, value) for the i-th sample of the analog signal waveform 9008 are samples (i-2) and (i-1) and the values are Ai-2 and Ai-1, the average value is outputted to OUT-A output terminal 11025 shown in Fig. 10. In this step also conversion from V (voltage) to I (current) is executed (in the circuit in Fig. 11). Also assuming that the oldest samples 9006, 9007 are the samples (i+1) and (i+2) and the values are Bi+1 and Bi+2, the average value is outputted to the OUT-B output terminal in Fig. 11. (Also the V to I conversion is executed like in this step line as described above) . With these operations, signals are treated in the analog mode, but substantially 4-dimensional FIR is executed by this sample-and-hold circuit 10003 as a band-pass filter. As all of these steps are executed in the analog mode (with V to I conversion executed simultaneously), it is possible to realise an extremely high speed operation with low power consumption.

Fig. 12 is a circuit diagram showing a buffer circuit 12001 (equivalent to the circuit 6028 in Fig. 6 and to the circuit 15021 in Fig. 15) in the analog amplifier-and-filter circuit according to Embodiment 2 of the present invention.

The buffer circuit 12001 has the configuration in which PMOS 12002, resistors 12012 and 12013, Vref (2.5 V) 12011, a charge amplifier 12004, an NMOS 12003, a constant current source 12005, switch elements 12009 and 12010 are connected as shown in the figure, and the buffer circuit 12001 also has an output

terminal 12006 (Herein, as all the Vout-A or Vout-B again converted to a voltage, and the systems A and B described above are buffer circuits, so that they are displayed with a common sign), and a SEL signal input terminal 12007.

In this figure, the reference numeral 12008 indicates an output signal OUT-A or OUT-B from the sample-and-hold circuit. Because of the configuration as described above, only a significant hit signal is selected, and further only a significant signal element synchronised to the frequency of 40 kHz is buffered, so that further power saving can be realised.

As described above, by using a signal-amplifying and signal-identifying circuit having the configuration according to Embodiment 2 of the present invention, it has become possible to realise a high performance and low power consumption system as a receiving circuit for an electric wave clock, but this embodiment can effectively be applied not only to the electric wave clock as described above, but also to signal processing for signals from a photo sensor (photodiode or a device comprising a plurality of photo sensors integrated therein), a temperature sensor, an acceleration sensor and an angular speed sensor with the functions for signal amplification and filtering (Use of the charge amplifier or execution of analog FIR for realising the functions in this invention is also novel) because of its features of low power consumption and high-speed operation.

Fig. 13 is a graph showing an FM multiplex broadcast base-band spectrum for explaining a receiving circuit and a decoder circuit for a receptor according to Embodiment 3 of the present invention. As a wrist watch receiving a signal carried on electric wave and playing some functions, there is a so-called receptor having an appearance similar to that of the electric wave clock described above. Also this receptor receives electric waves and performs some functions, but the functions are slightly different from those of an electric wave clock, and information delivered by a sub-carrier multiplexed on an electric wave for FM broadcasting (Carrier: Several tens MHZ to 200 MHz) plays, for instance, a role of paging function (pocket-bell function). In this specification, equipment which looks like a wrist watch (or any other portable equipment) and has the function is called receptor. As shown in Fig. 13, a spectrum allocated to the receptor is a sub-carrier multiplexed centring on a frequency of 66.5 kHz as shown in Fig. 13. A technological object of this receptor equipment is to accurately decode the sub-carrier with low power consumption.

Fig. 14 is a system block diagram for illustrating a receiving circuit for a receptor according to Embodiment 3 of the present invention. This receiving circuit has an antenna 14001, an RF (radio) circuit block 14002; has a sub-carrier decoding circuit block 14004 comprising an A/D converter circuit section 14005, a timing circuit section 14009, a digital filter circuit section 14006, a wave detecting circuit section 14007, a protocol decoder circuit section 14008; and also has a CPU circuit block 14011 built with a CPU 14012 at the centre. As indicated by the analog signal stage at the left from a dotted centre line 14013 in the figure and also by the digital signal stage at the right therefrom, a Base-band signal fetched into the RF circuit block (base-band signal like 14003) is at first converted to a digital signal by the A/D converter 14005 simultaneously when the signal goes into the decoder circuit block 14004, and then the signal is subjected to processing (such as decoding). This system configuration is based on the so-called DSP (Digital Signal Processing) system with a number of processing stages (resulting in a large circuit scale and high cost), so that large clock noise is generated (so that a further deeply structured circuit configuration is required for filtering), resulting in high power consumption (as the entire system is operating according to a high-speed clock). To overcome the problems as described above, the present invention provides the decoder circuit as described below.

Fig. 15 is a system block diagram 15001 showing a sub-carrier decoding circuit for the receptor according to Embodiment 3 of the present invention. The sub-carrier circuit has the configuration in which coupling capacitances 15011 and 15013, charge amplifiers 15012 and 15014, feedback capacitances 15007 and 15008, switch elements 15002 and 15003, a clock oscillator (a central frequency of 66.5 kHz of a sub-carrier for the receptor) 15019, a comparator circuit section 15004, a shift register 15006, a sample-and-hold circuit section 15015, an output control circuit section 15033, a buffer circuit section 15021, an AM-PSK (AM; Amplitude Modulation, PSK: Phase Shift Keying) wave-detecting circuit section 15022, a protocol decoder circuit section 15023, and a CPU interface circuit section 15024 are connected by, in addition to a signal line through which a base-band signal 15031 basically passes, hit signal lines 15005 and 15010, a reset signal line 15009, a clock signal line 15020, SEL signal lines 15032 and 15016, a Read signal line 15017, and a CS signal line 15018 as shown in the figure. In this figure, designated at the reference numeral 15025 is a data output terminal, at 15026 a CS terminal, at 15027 a WR terminal, at 15028 an INT terminal, and at 15029 a SLEEP terminal. A section at the left from the dotted line 15030 is an analog signal stage, and at the right therefrom a digital signal stage. With this configuration, a sub-carrier is decoded from the base-band signal in the charge amplifier-and-analog filter circuit described in relation to Embodiment 2. Processing up to decoding is executed with an analog FIR filter in this analog signal stage, and wave detection and conversion of the signal to digital signal waveform are executed simultaneously in said AM-PSK wave detecting circuit (which may have the configuration like that of the wave detecting circuit in Embodiment 1), and the further processing is executed in the digital signal stage. As described above, most operations executed in the sub-carrier decoding circuit are executed in the analog mode (which provides a substantial advantage because an A/

D converter or a digital FIR is not used), so that a low-noise (clock noise) (and accordingly small scale and low-cost) circuit with the small number of processing stages and low power consumption can be realised. This embodiment is not only applicable to decoding of a sub-carrier for the receptor, but is effective and at the same time useful from viewpoints of low power consumption and low cost, even if it is applied to decoding of coded signals in communications using a photo sensor (a photo-diode or the integration thereof) or to a similar decoding circuit or antenna tuning (for control of the section 14014 in Fig. 14) in other type of radio equipment (such as a portable telephone set, a pager, or a character-multiplexed radio set).

Fig. 16A is a view showing external appearance of an MR element used in electronic equipment according to Embodiment 4 of the present invention.

Fig. 16B is a graph showing characteristics of an MR element used in the electronic equipment according to Embodiment 4 of the present invention.

Fig. 16C is a block diagram showing a receiving circuit in the initial stage in a case where the MR element according to Embodiment 4 of the present invention is used in an antenna.

As described above, as portable equipment receiving electric wave and executing some functions, there is an electric-wave clock or a so-called receptor, and in Embodiment 1 of the present invention relating configuration of an antenna section therein, a Hall element antenna was described, but this embodiment relates to a case where an MR (magnetic reluctance) element is used. The magnetic reluctance element (MR element) is obtained by providing patterns on a magnetic reluctance film 16003 made of such a material as InSb or CoNi on a pellet (substrate) 16001 as shown in Fig. 16A, and when a magnetic flux B comes onto a plate surface in the vertical direction, resistance between electrodes 16002 and 16010 shows the characteristics as shown in Fig. 16B. The vertical axis indicates minus. Namely when a magnetic flux increases, the resistance drops. The fact that there is provided an offset 16005 is one of the features of the present invention, but also the sensitivity is high. However, there is substantial influence by a temperature.

The circuit should preferably have the configuration as shown in Fig. 16C in which two pieces of MR elements 16007 and 16008 are used in series to form the circuit. In this figure, the reference numeral 16006 indicates a coupling capacitance, and the reference numeral 16009 indicates a JFET.

As described above, with the present invention, a small-sized and low cost system with low power consumption, which has not been realised with the conventional technology, is provided for an antenna and a receiving circuit making use of electric waves described above or those from a GPS (Global Positioning System) satellite or the like.

Although the invention has been described with respect to a specific embodiment for a complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modifications and alternative constructions that may occur to one skilled in the art which fairly fall within the basic teaching herein set forth.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

Claims

1. Electronic equipment comprising:

an antenna (1002);
a receiving circuit (1001) with functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a clock display; and characterised in that;
said antenna comprises a semiconductor device (5007) having the magnetic Hall effect and said semiconductor device has a ferromagnetic body (5003, 5005) adjacent thereto.

2. Electronic equipment according to claim 1; wherein said antenna makes use of the attenuation characteristics (up to around 100 kHz) of a response speed against change of a magnetic field.

3. Electronic equipment according to claim 1; wherein said antenna is a magnetic reluctance element.

4. Electronic equipment according to any preceding claim; wherein said receiving circuit comprises at least a FET amplifier (1004), a flat amplifier (1005), an active filter (1006) and a wave detector(1008).

5. Electronic equipment according to claim 1; wherein said receiving circuit has a function to amplify voltage change in output from said antenna and said differentiation is executed by way of a self-activating circuit operation.

6. Electronic equipment comprising:

an antenna (6002);
a receiving circuit (6001) having functions to amplify, differentiate and detect an electric wave received by said antenna, and characterised in that;
said receiving circuit has a differential amplifier (7002) comprising a MOS transistor, has a comparator (8001) comprising a MOS transistor in succession to said differential amplifier, and also has an electric charge container (6023) comprising a MOS transistor provided

in parallel to said comparator.

7. Electronic equipment according to claim 6; wherein said receiving circuit has a function to amplify voltage change in output from said antenna and said differentiation is executed by way of self-activating circuit operations.

8. Electronic equipment comprising:

an antenna (14001);
a receiving circuit (14004) having the functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a decoding circuit (14008) having a function to decode a coded signal superimposed to said electric wave, and characterised in that;
said receiving circuit has a differential amplifier (7002) comprising a MOS transistor, has a comparator (8001) comprising a MOS transistor in succession to said differential amplifier, and also has an electric charge container (6023) comprising a MOS transistor provided in parallel to said comparator.

9. Electronic equipment according to claim 8; wherein said receiving circuit has a function to amplify voltage change in output from said antenna and said differentiation is executed by way of a self-activating circuit operations.

10. Electronic equipment comprising:

an antenna;
a receiving circuit with functions to amplify, differentiate, and detect an electric wave received by said antenna; and
a clock display function, and characterised in that;
said antenna has a semiconductor device (16007, 16008) having the magnetic reluctance effect, and a plurality of said semiconductors are electrically connected to each other in series.

11. Electronic equipment according to claim 10; wherein said receiving circuit has a function to amplify voltage change in output from said antenna and said differentiation is executed by way of a self-activating circuit operation.

FIG. 1A

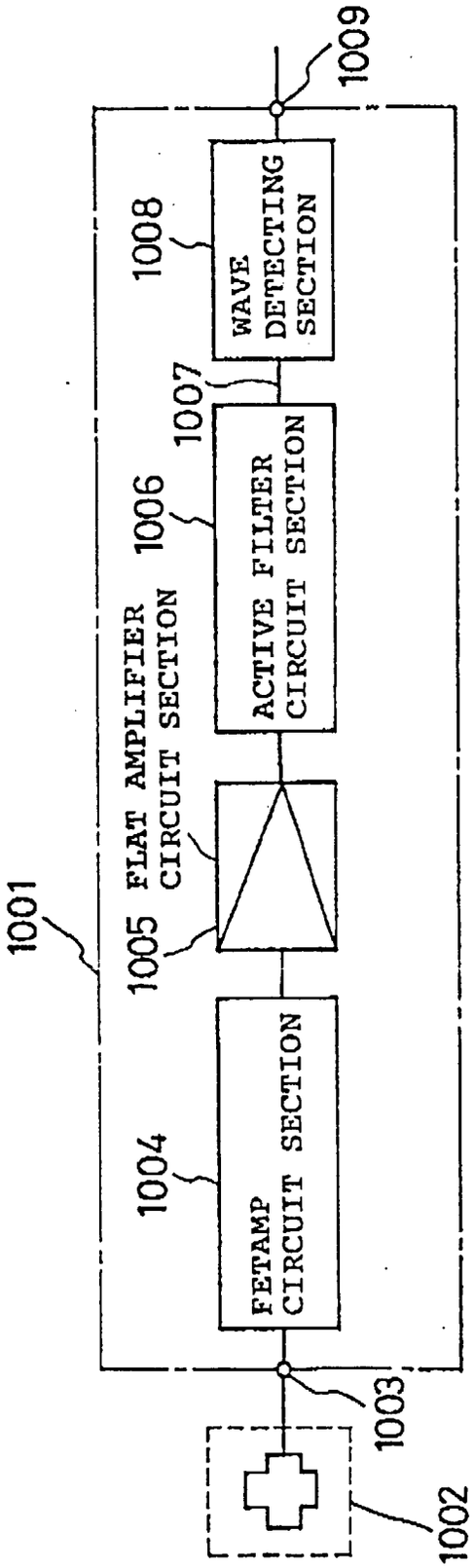


FIG. 1B NODE 1

FIG. 1C OUTPUT WAVEFORM

FIG. 2

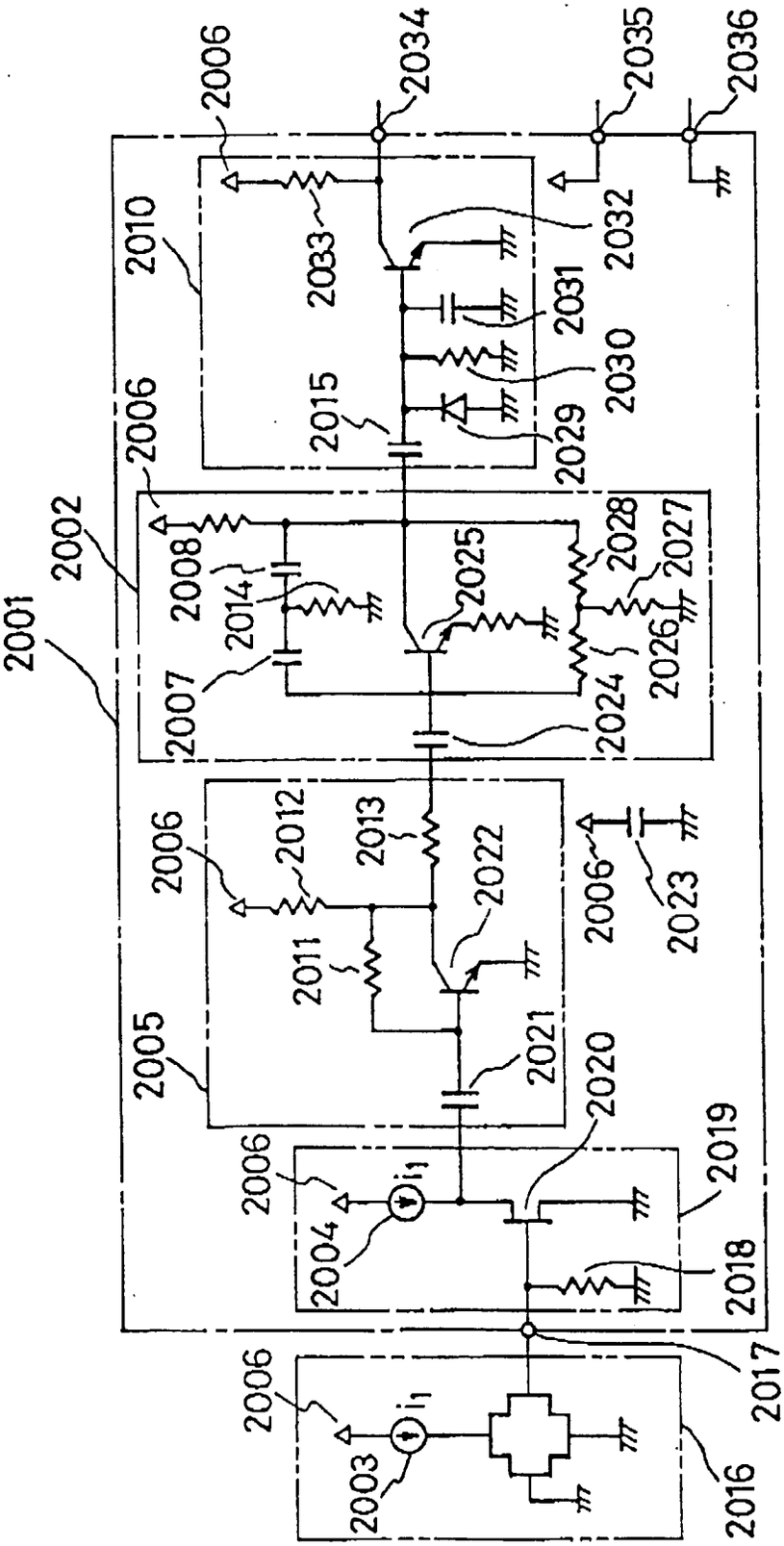
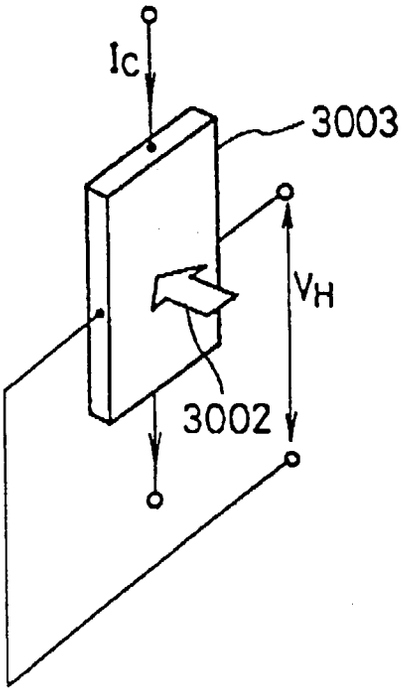

2001
2002
2003
2004
2005
2006
2007
2008
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
i1

FIG. 3A


Ic
3003
V_H
3002

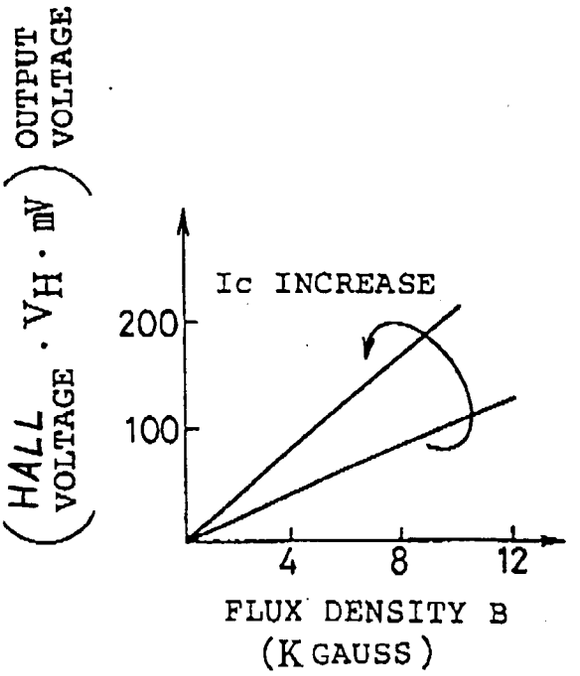

(HALL VOLTAGE · V_H · mV) OUTPUT VOLTAGE
Ic INCREASE
200
100
4
8
12
FLUX DENSITY B
(K GAUSS)

FIG. 3B

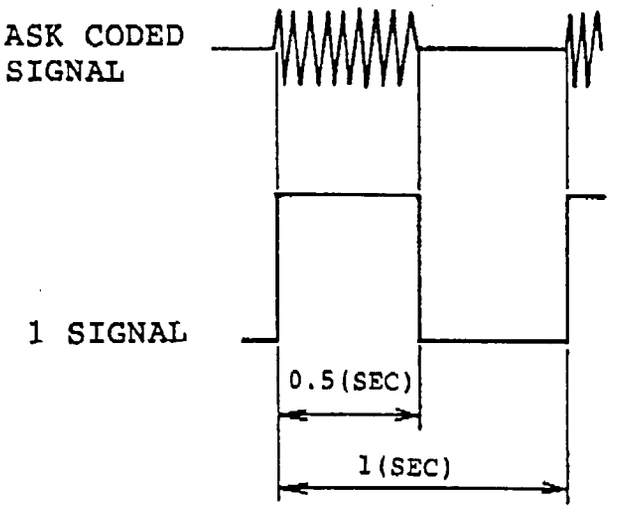


FIG. 4A

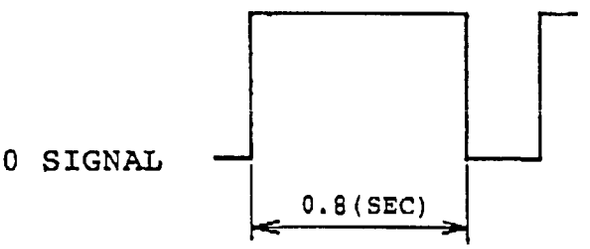


FIG. 4B

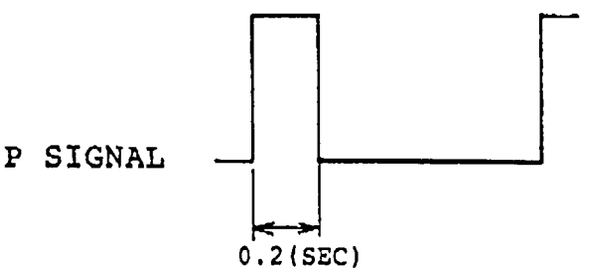


FIG. 4C

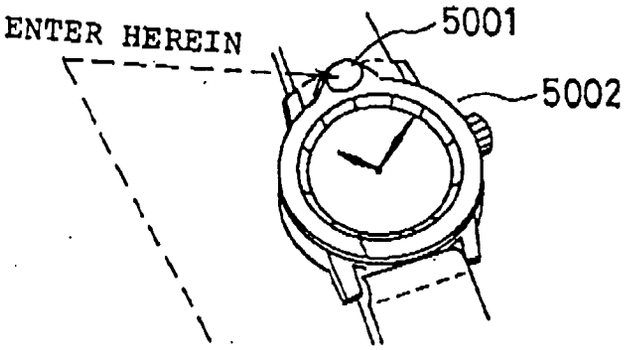


FIG. 5A

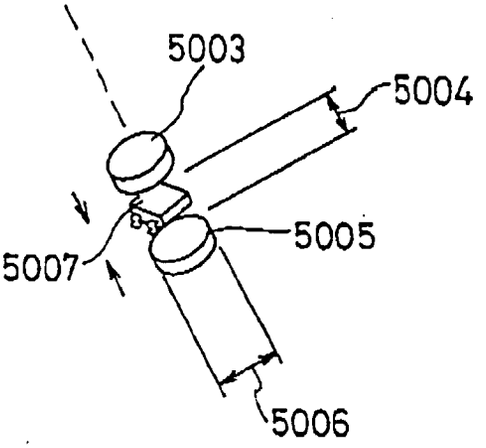


FIG. 5B

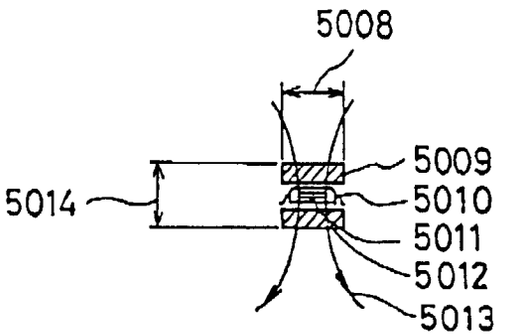
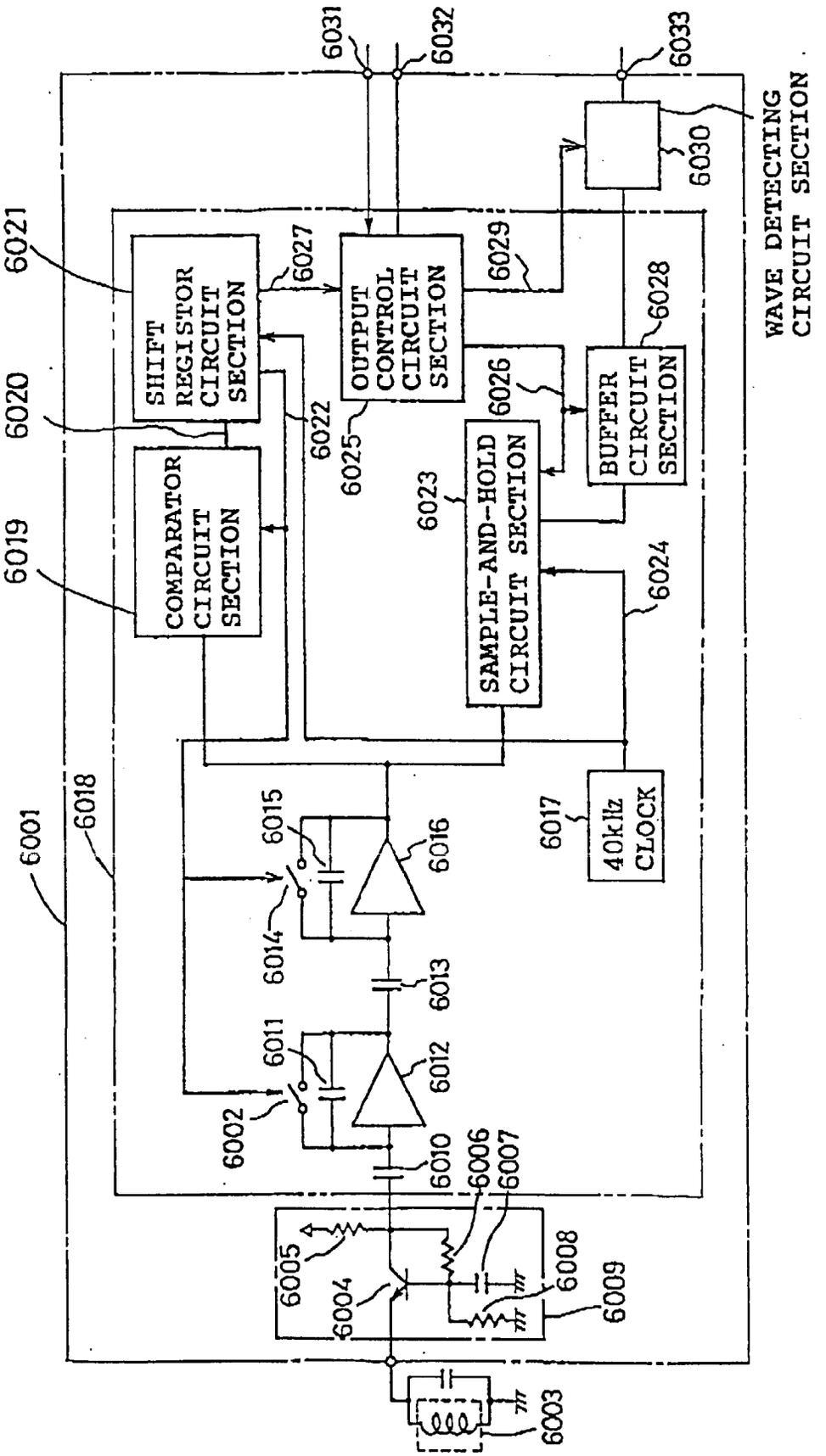


FIG. 5C

FIG. 6


WAVE DETECTING CIRCUIT SECTION
SHIFT REGISTOR CIRCUIT SECTION
OUTPUT CONTROL CIRCUIT SECTION
BUFFER CIRCUIT SECTION
COMPARATOR CIRCUIT SECTION
SAMPLE-AND-HOLD CIRCUIT SECTION
40kHz CLOCK
6001
6002
6003
6004
6005
6006
6007
6008
6009
6010
6011
6012
6013
6014
6015
6016
6017
6018
6019
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6027
6028
6029
6030
6031
6032
6033

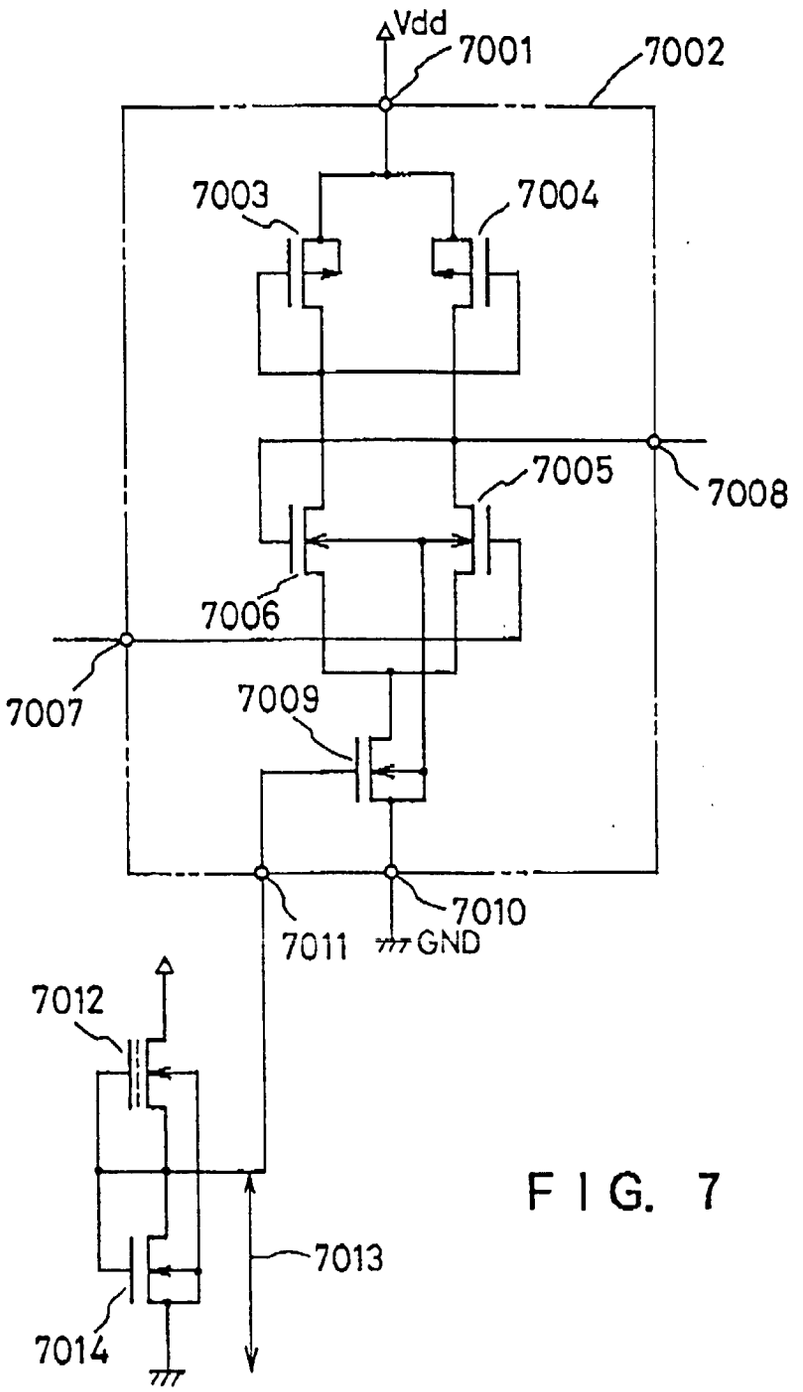

Vdd
7001
7002
7003
7004
7005
7008
7006
7007
7009
7011
7010
GND
7012
7013
7014

FIG. 7

FIG. 8

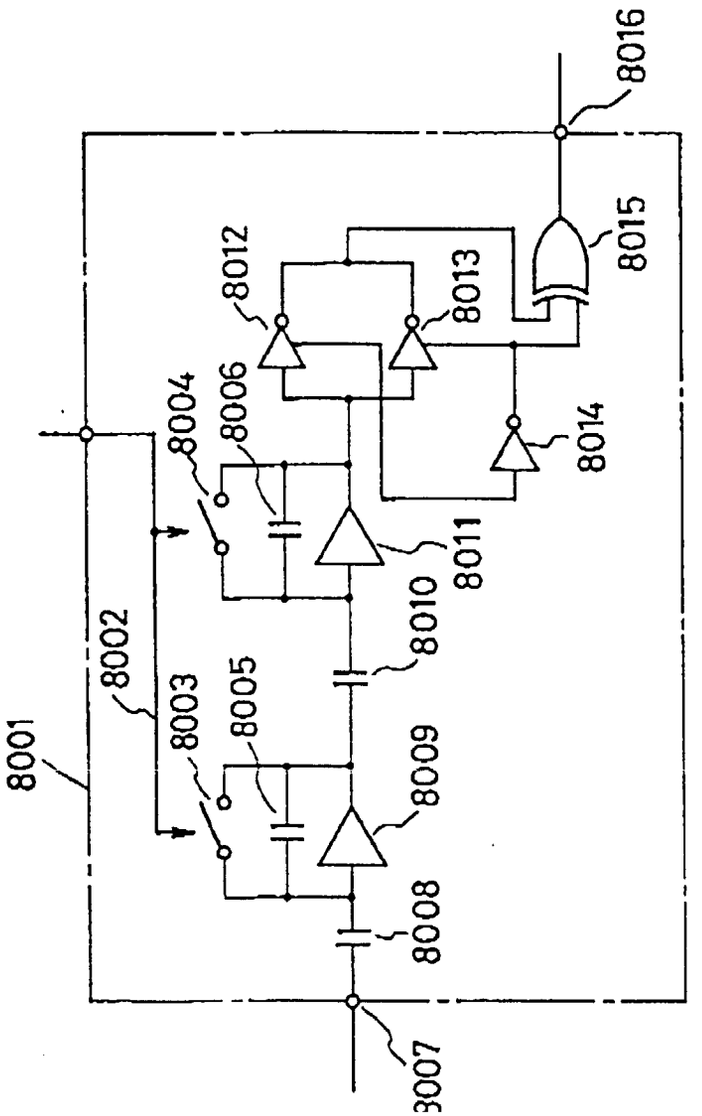
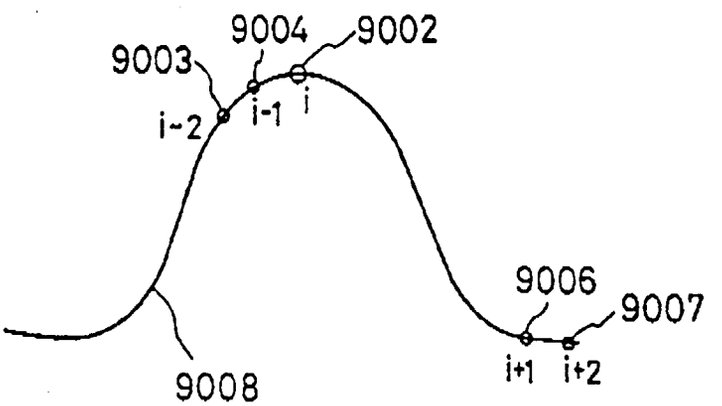

8001
8002
8003
8004
8005
8006
8007
8008
8009
8010
8011
8012
8013
8014
8015
8016

FIG. 9



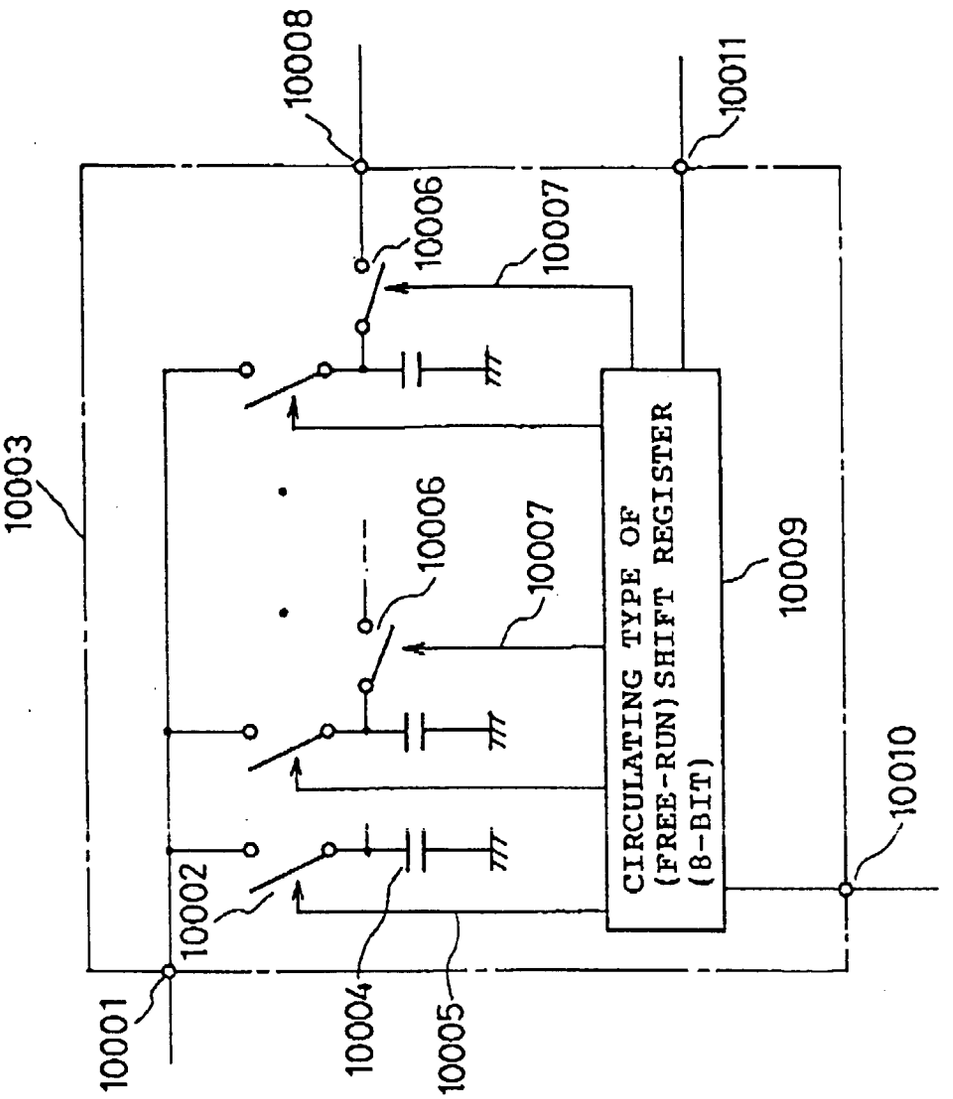

10008
10011
10006
10007
10003
10006
10007
CIRCULATING TYPE OF
(FREE-RUN) SHIFT REGISTER
(8-BIT)
10009
10010
10002
10001
10004
10005

FIG. 10

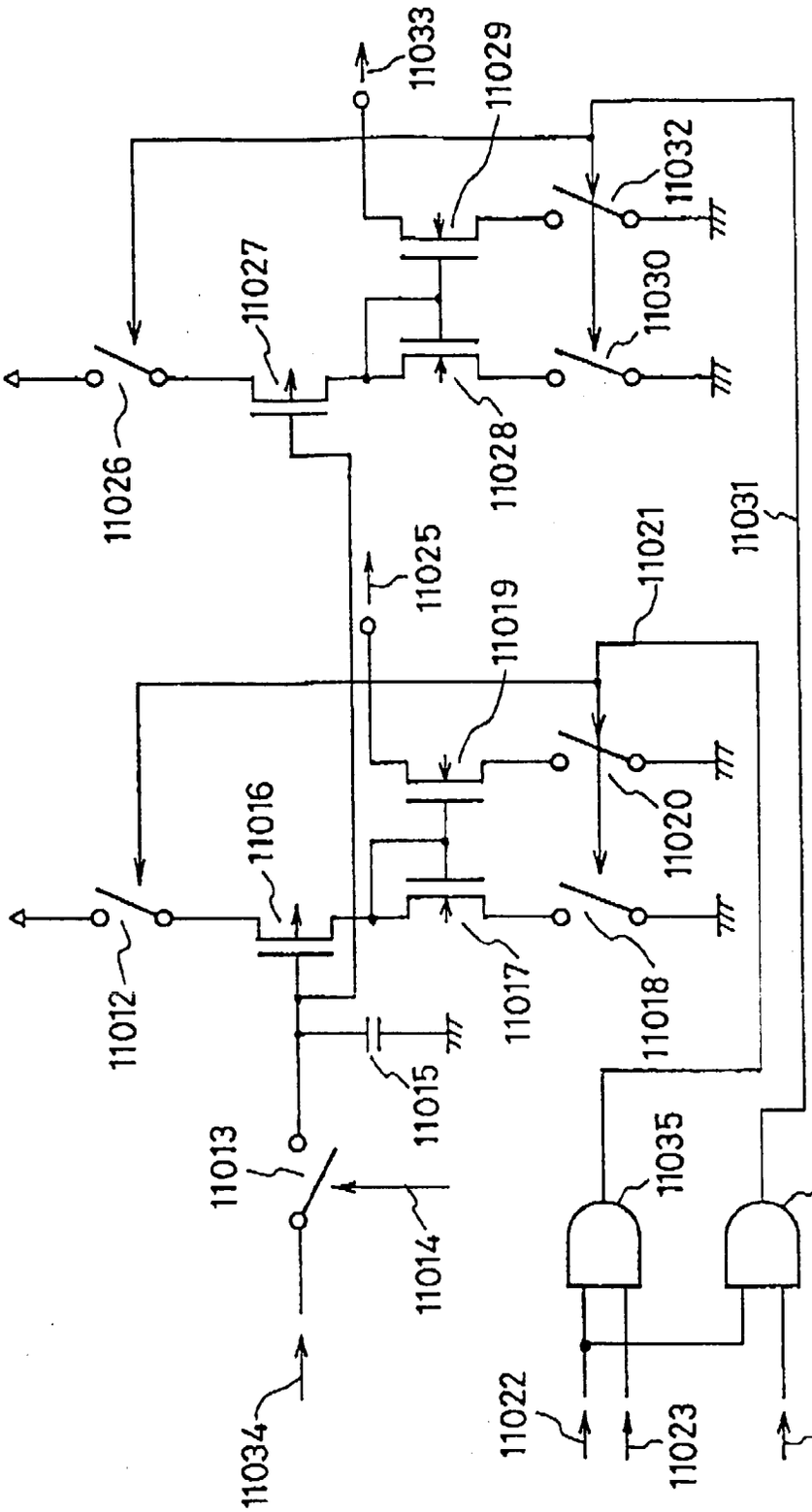

11033
11029
11032
11027
11030
11026
11028
11031
11025
11021
11019
11016
11020
11012
11017
11018
11015
11013
11035
11036
11014
11034
11022
11023
11024

FIG. 11

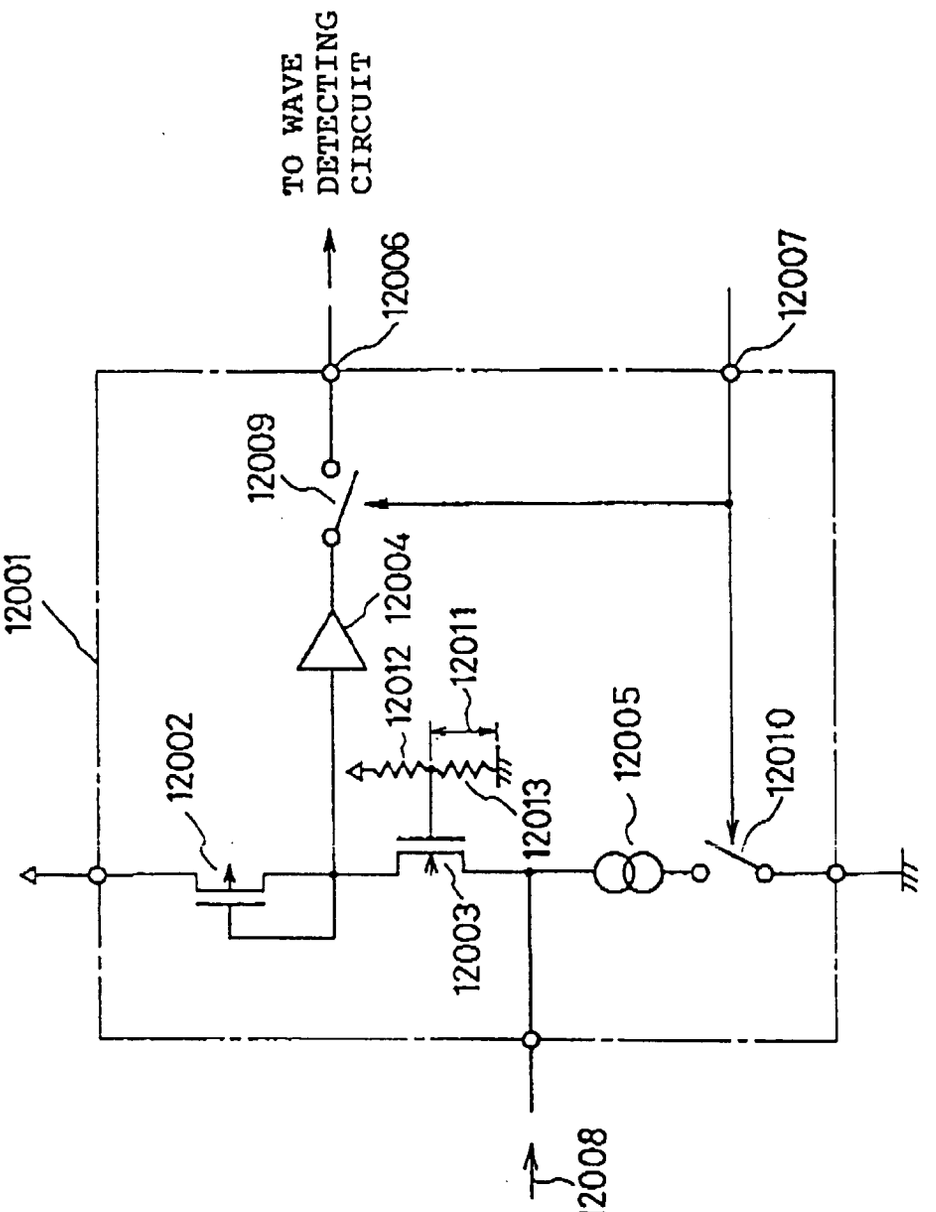

TO WAVE DETECTING CIRCUIT
12006
12007
12009
12001
12004
12012
12011
12002
12005
12010
12013
12003
12008

FIG. 12

FIG. 13

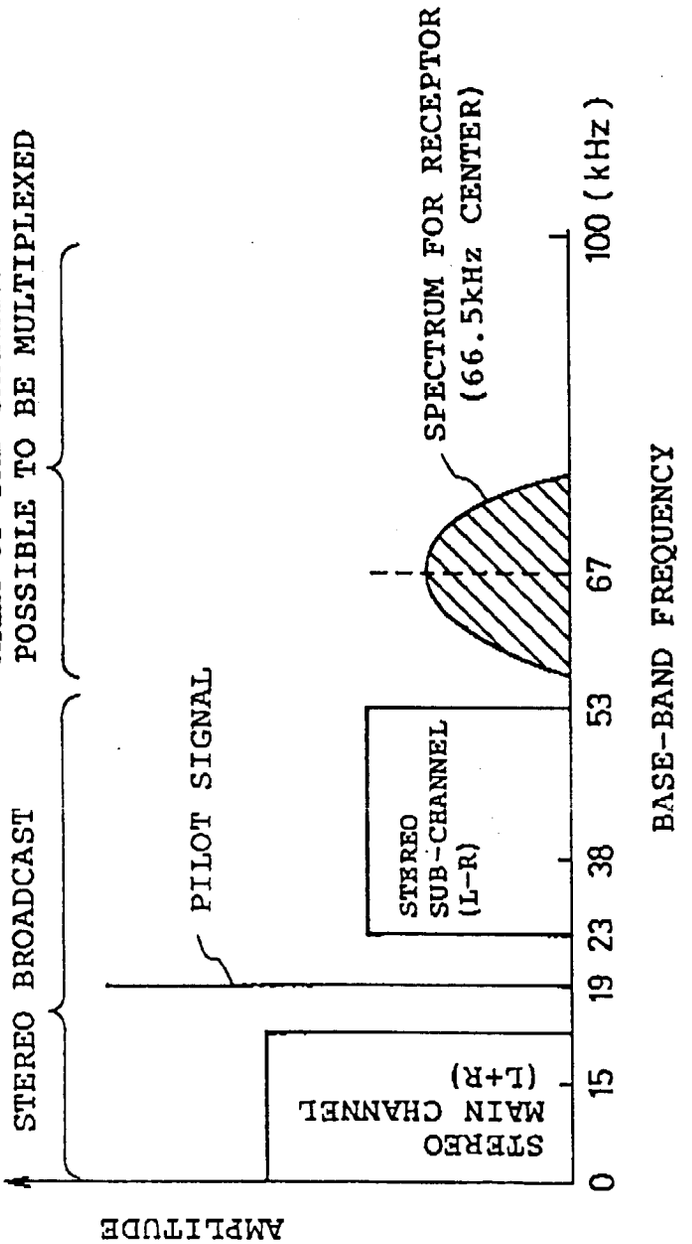

AREA OF SAB-CARRIER
POSSIBLE TO BE MULTIPLEXED
STEREO BROADCAST
PILOT SIGNAL
SPECTRUM FOR RECEPTOR
(66.5kHz CENTER)
STEREO
MAIN CHANNEL
(L+R)
STEREO
SUB-CHANNEL
(L-R)
AMPLITUDE
0
15
19
23
38
53
67
100 (kHz)
BASE-BAND FREQUENCY

FIG. 14

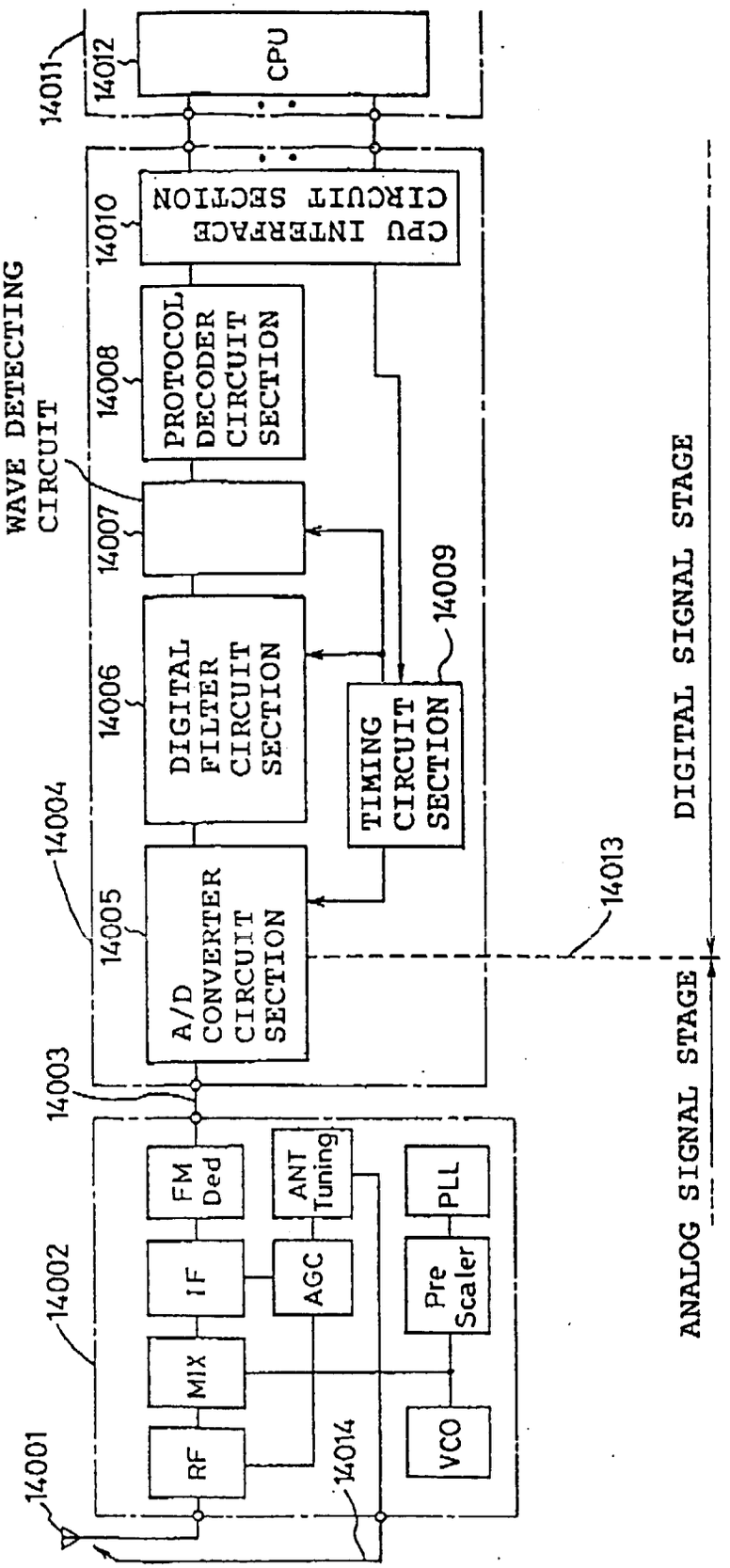

14011
14012
CPU
CPU INTERFACE CIRCUIT SECTION
14010
PROTOCOL DECODER CIRCUIT SECTION
14008
WAVE DETECTING CIRCUIT
14007
DIGITAL FILTER CIRCUIT SECTION
14006
TIMING CIRCUIT SECTION
14009
14004
14005
A/D CONVERTER CIRCUIT SECTION
14013
DIGITAL SIGNAL STAGE
ANALOG SIGNAL STAGE
14003
14002
FM Ded
IF
MIX
RF
ANT Tuning
AGC
PLL
Pre Scaler
VCO
14001
14014

FIG. 15

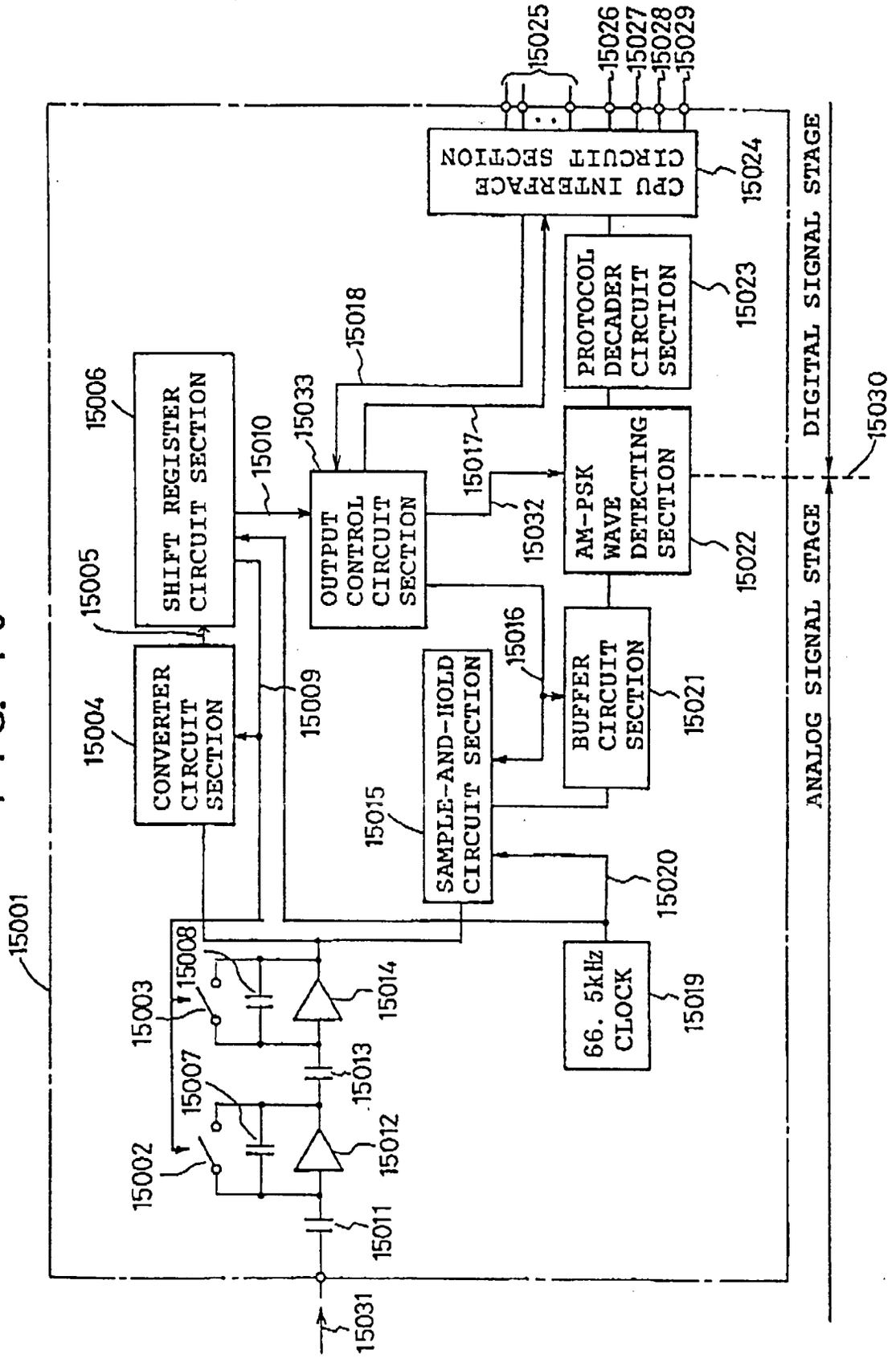

15001
15002
15003
15004
15005
15006
15007
15008
15009
15010
15011
15012
15013
15014
15015
15016
15017
15018
15019
15020
15021
15022
15023
15024
15025
15026
15027
15028
15029
15030
15031
15032
15033
SHIFT REGISTER CIRCUIT SECTION
CONVERTER CIRCUIT SECTION
OUTPUT CONTROL CIRCUIT SECTION
SAMPLE-AND-HOLD CIRCUIT SECTION
BUFFER CIRCUIT SECTION
AM-PSK WAVE DETECTING SECTION
PROTOCOL DECADER CIRCUIT SECTION
CPU INTERFACE CIRCUIT SECTION
66. 5kHz CLOCK
ANALOG SIGNAL STAGE
DIGITAL SIGNAL STAGE

FIG. 16A

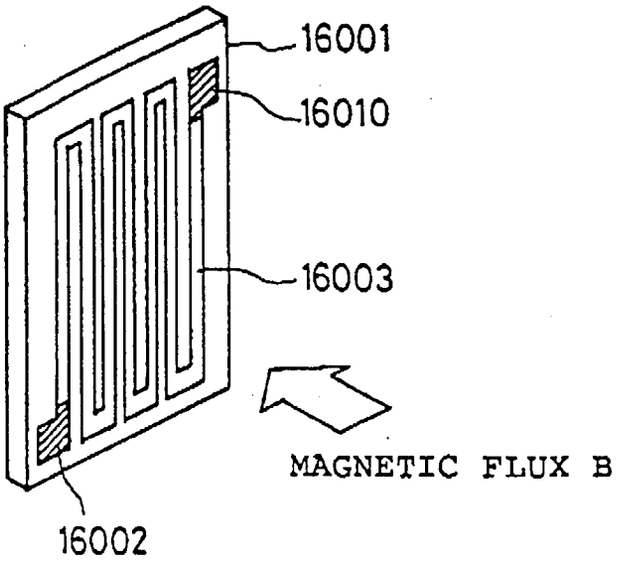
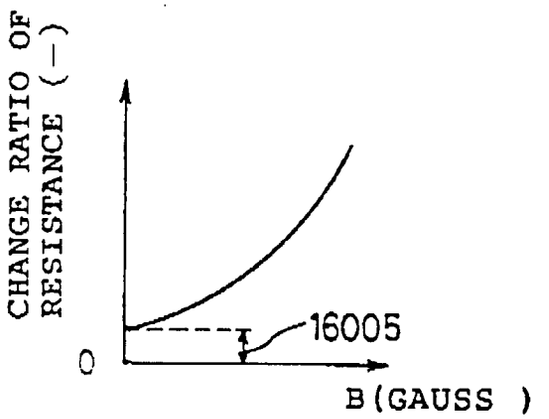


FIG. 16B



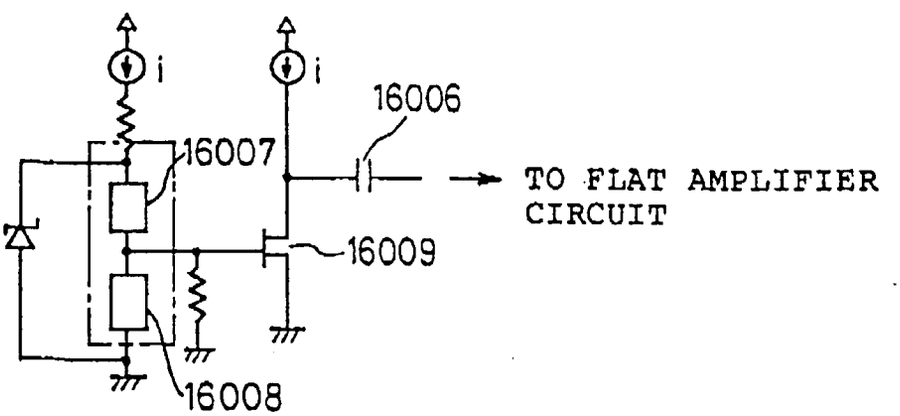


FIG. 16C

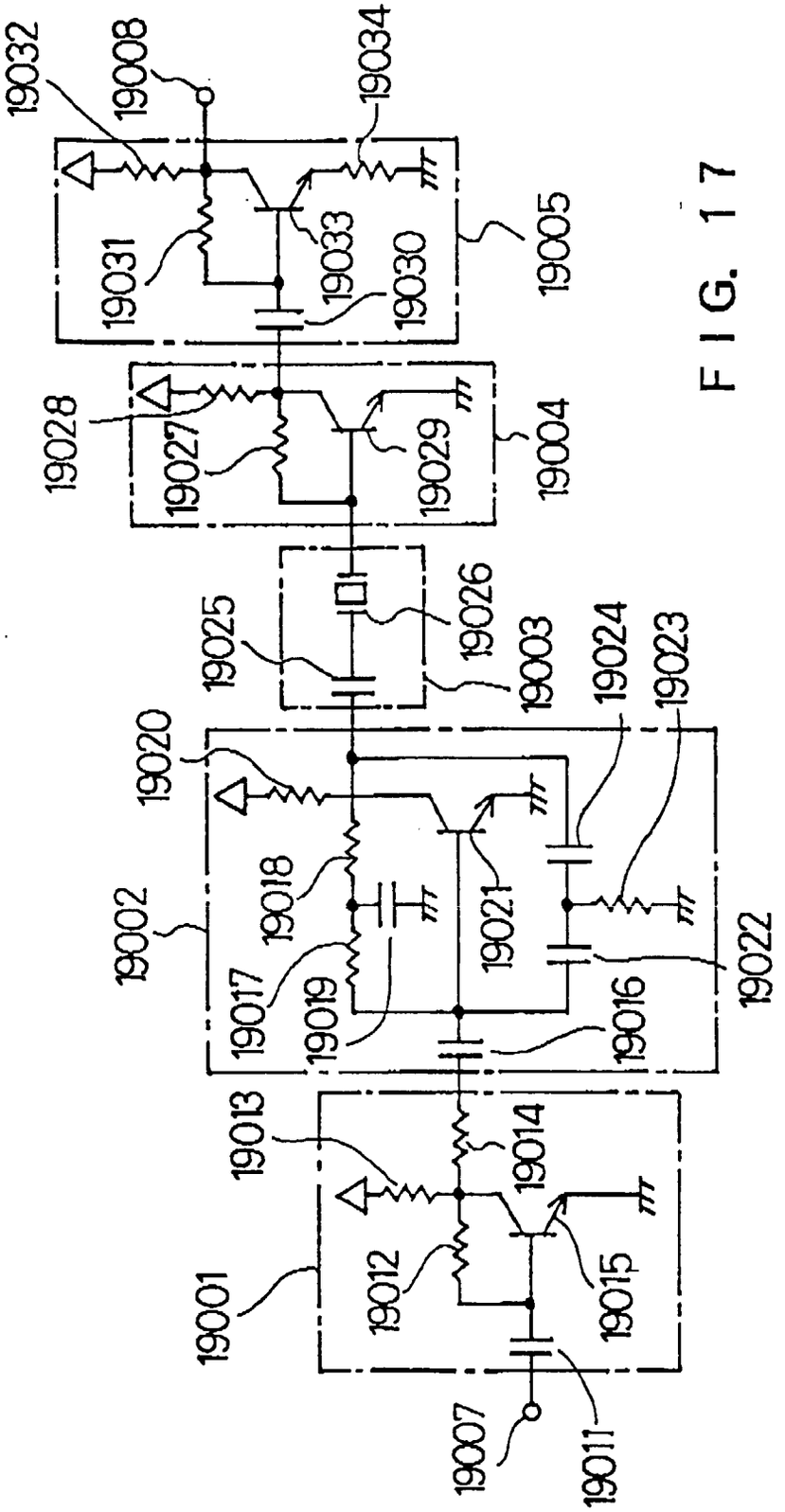

19032
19008
19034
19031
19033
19030
19005
19028
19027
19029
19004
19025
19026
19003
19024
19023
19020
19018
19021
19002
19017
19019
19016
19022
19013
19014
19001
19012
19015
19007
19011

FIG. 17

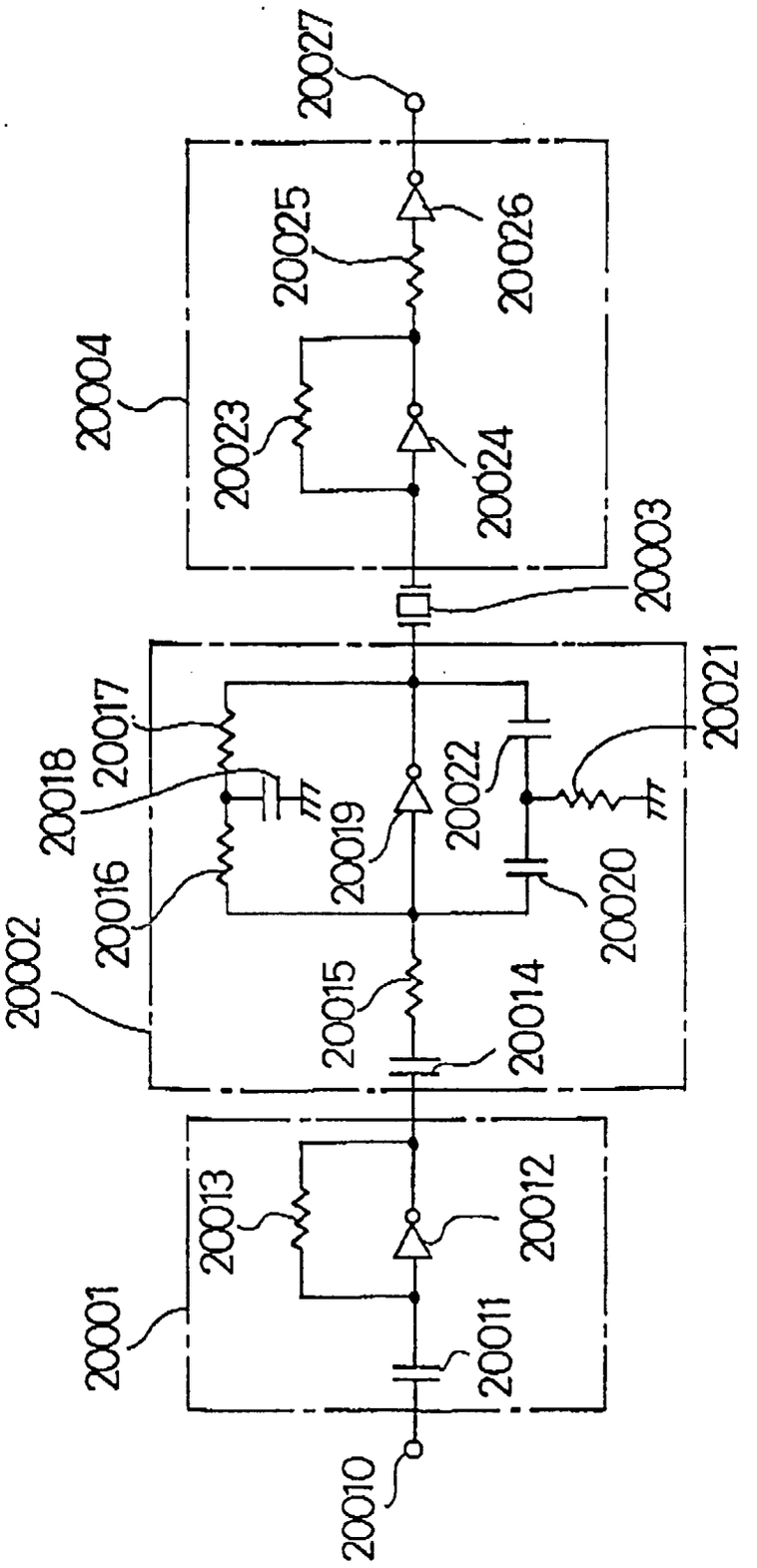

20010
20001
20013
20012
20011
20002
20015
20014
20016
20017
20018
20019
20022
20020
20021
20003
20004
20023
20024
20025
20026
20027

FIG. 18

FIG. 19

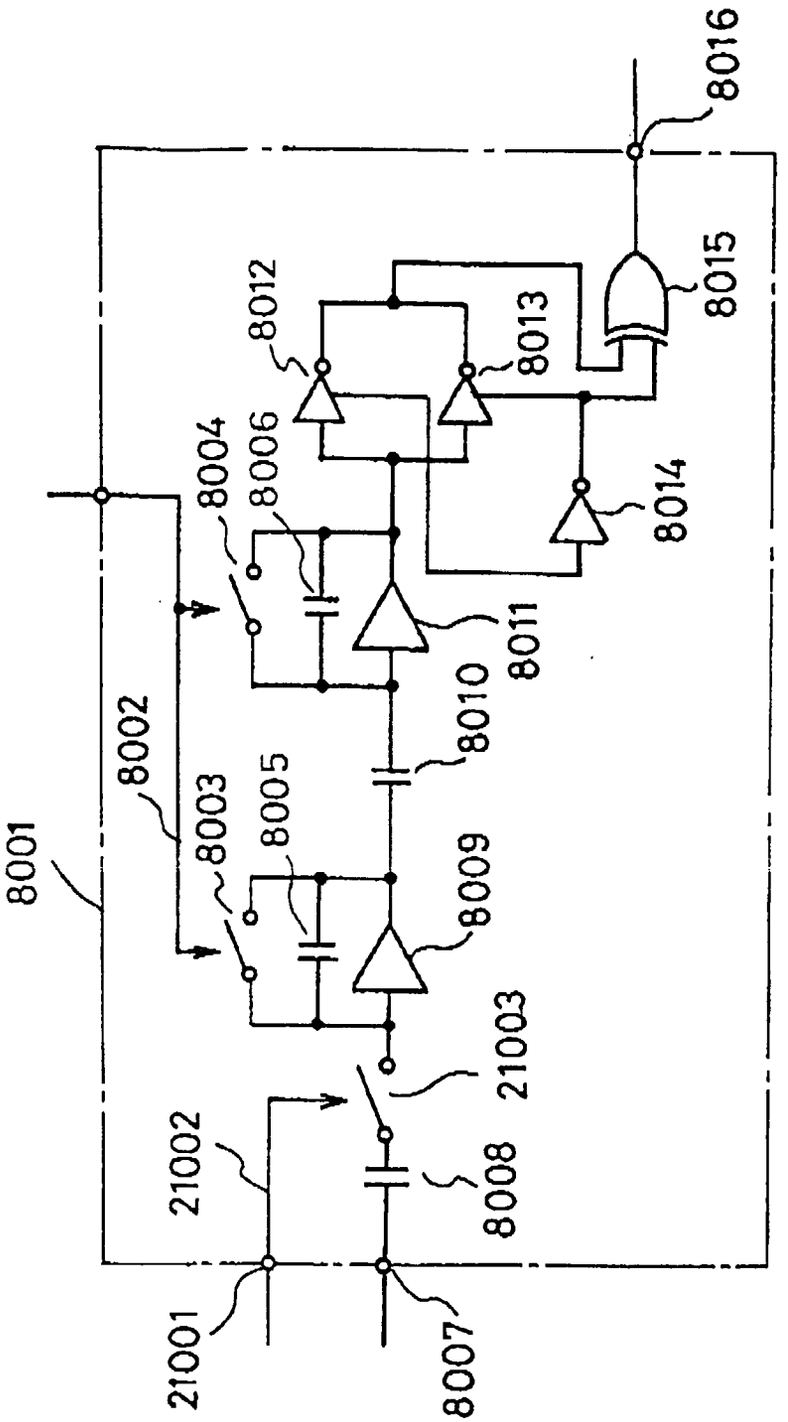

8001
8002
8003
8004
8005
8006
8007
8008
8009
8010
8011
8012
8013
8014
8015
8016
21001
21002
21003

FIG. 20A

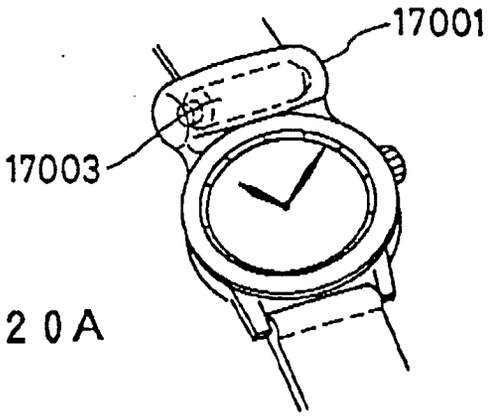


FIG. 20B

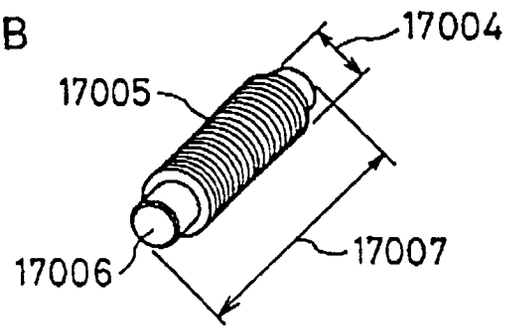


FIG. 20C

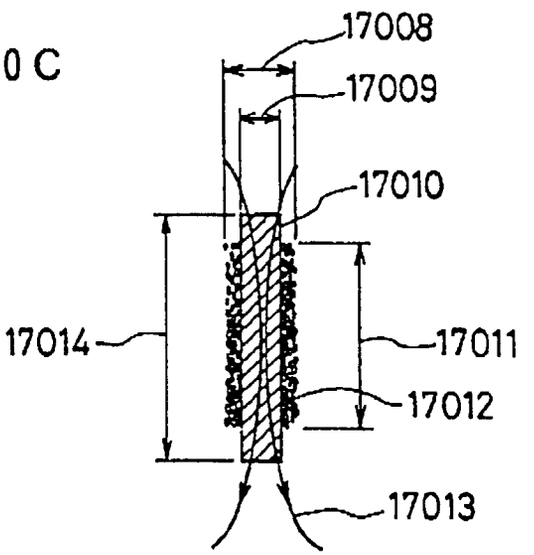
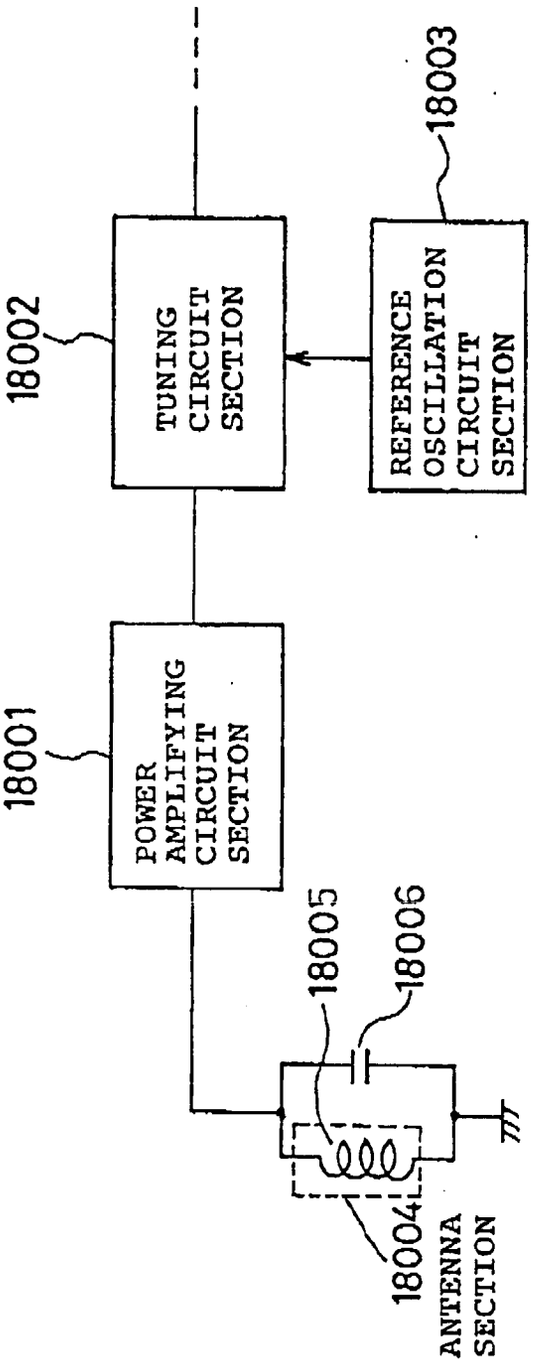


FIG. 21


18001
POWER AMPLIFYING CIRCUIT SECTION
18002
TUNING CIRCUIT SECTION
18003
REFERENCE OSCILLATION CIRCUIT SECTION
18004
ANTENNA SECTION
18005
18006