(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 818 900 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
14.01.1998 Bulletin 1998/03

(51) Int. Cl.[6]: **H04J 3/16**, H04H 1/00

(21) Application number: **97111462.4**

(22) Date of filing: **07.07.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **08.07.1996 JP 195235/96**

(71) Applicant:
KABUSHIKı KAISHA KENWOOD
Shibuya-ku Tokyo (JP)

(72) Inventors:
- **Matsushima, Yukio**
  Sagamihara-shi, Kanagawa (JP)
- **Sakai, Shouichirou**
  Yokohama-shi, Kanagawa (JP)
- **Kitano, Masahiro**
  Yokohama-shi, Kanagawa (JP)
- **Tsurumi, Atsushi**
  Kawasaki-shi, Kanagawa (JP)

(74) Representative:
Patentanwälte
Leinweber & Zimmermann
Rosental 7
80331 München (DE)

(54) Digital signal multiplexing apparatus

(57) A digital signal multiplexing apparatus is provided which can multiplex service data having a plurality of different bit rates and change the bit rate even during signal transmission. A controller generates multiplex configuration information indicating how service data is multiplexed, in accordance with instructions, and generates commands whose contents match the multiplex configuration information. The generated multiplex configuration information is written in a memory circuit, and the generated command is converted by a CPU into a control signal for encoders. The multiplex configuration information read from the memory circuit is encoded by a convolution encoder into a predetermined format. A plurality of service data sets are encoded by convolution encoders into predetermined formats in accordance with control signals converted by CPU, and multiplexed by a multiplexer circuit. The data encoded by the convolution encoder and the data multiplexed by the multiplexer circuit are further multiplexed by another multiplexer circuit.

EP 0 818 900 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a digital signal multiplexing apparatus for multiplexing a plurality of service data sets time sequentially on a baseband, and more particularly to a digital signal multiplexing apparatus of a test signal generator used for simulation of a receiver of a digital audio broadcasting system of European Telecommunication Standard.

2. Description of the Related Art

A CS PCM music broadcasting system using a communication satellite CS is known as a broadcasting system which multiplexes service data time divisionally on a baseband. With this system, six channels of signals of 2.048 Mbps of the PCM music broadcasting format of BS broadcasting are multiplexed. Service data to be multiplexed has a fixed bit rate of 2.048 Mbps.

The digital audio broadcasting (hereinafter represented by DAB) system of European digital audio broadcasting specifications uses formats by which service data corresponding to one channel of conventional broadcasting (programs) can be multiplexed a plurality of times at different bit rates and by which bit rates of multiplexed service data can be made variable during broadcasting without deteriorating time sequential continuity (this case will be called multiplex re-configuration where applicable).

As stipulated in the European DAB specification (European Telecommunication Standard, ETS300 401), information to be transmitted includes a sync channel for transmitting sync information required for synchronization at a receiving site, a fast information channel (hereinafter represented by FIC where applicable) for multiplexing information necessary for tuning at a receiving site and program auxiliary information, and a main service channel (hereinafter represented by MSC where applicable) for multiplexing service data such as audio data.

For a digital signal multiplexing apparatus of the DAB specification, it is necessary to convert multiplex configuration information (hereinafter represented by MCI where applicable) into the FIC format and multiplex the information. It is also necessary to encode MSC so as to match the multiplex configuration information (MCI). If the bit rate of the service data is changed during multiplex re-configuration, it is necessary to change settings of an encoder at the designated timing. Particularly, time interleave is performed over frames in the unit of frame with the interleave depth of 15 frames at a maximum. Therefore, if the bit rate is changed in multiplex re-configuration, it is necessary to consider a time required for a time interleave process in order to correct the timing for switching of puncturing by a convolution encoder. Specifically, if the bit rate is changed slow, puncturing is required to be changed 15 frames before such a change.

However, a digital signal multiplexing apparatus has been realized as yet which can multiplex a plurality of service data sets having different bit rates in the form matching multiplex configuration information designated by a user in advance and which can change bit rates even during signal transmission.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a digital signal multiplexing apparatus which can multiplex a plurality of service data sets having different bit rates in the form matching multiplex configuration information designated by a user in advance and which can change bit rates even during signal transmission.

According to one aspect of the present invention, a digital signal multiplexing apparatus for multiplexing, time divisionally on a baseband, a plurality of service data sets having different bit rates is provided which comprises: information generating means for generating multiplex configuration information indicating how service data sets are multiplexed, in accordance with designated information, and generating a command whose contents match the multiplex configuration information; a memory circuit for storing the multiplex configuration information generated by the information generating means; means for controlling to write the multiplex configuration information into the memory circuit and converting the command generated by the information generating means into control signals for encoders; a first encoder for encoding the multiplex configuration information read from the memory circuit in accordance with a predetermined format; second encoders for encoding the plurality of service data sets in accordance with the control signals converted by the controlling and converting means and in accordance with predetermined formats; a first multiplexer circuit for multiplexing the plurality of service data sets encoded by the second encoders; and a second multiplexer circuit for multiplexing the data encoded by the first encoder and the data multiplexed by the first multiplexer circuit.

A plurality of service data sets having difference bit rates can be multiplexed in the following manner. The information generating means generates multiplex configuration information indicating how service data sets are multiplexed, in accordance with designated information, and generating a command whose contents match the multiplex configuration information. The controlling and converting means controls to write the generated configuration information into the memory circuit and converting the generated command into control signals for encoders. The first encoder encodes the multiplex configuration information read from the memory circuit

in accordance with a predetermined format. The second encoders encode a plurality of service data sets in accordance with the control signals converted by the controlling and converting means and in accordance with predetermined formats. The first multiplexer circuit for multiplexing the plurality of service data sets encoded by the second encoders, and the second multiplexer circuit multiplexes the data encoded by the first encoder and the data multiplexed by the first multiplexer circuit.

The digital signal multiplexing apparatus may further comprise an encoder control circuit for switching control signals of the second encoders at each designated frame in accordance with the plurality of multiplex configuration information data sets read from the memory circuit, wherein the multiplexing states are periodically changed while retaining a time sequential continuity.

The encoder control circuit switches control signals of the second encoders at each designated frame in accordance with the plurality of multiplex configuration information data sets read from the memory circuit, wherein the multiplexing states are periodically changed while retaining a time sequential continuity.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of a digital signal multiplexing apparatus according to an embodiment of the invention.

Figs. 2A and 2B are schematic diagrams illustrating the contents of a memory circuit of the digital signal multiplexing apparatus of the embodiment.

Figs. 3A, 3B-1 and 3B-2 are schematic diagrams illustrating CIF multiplexing positions according to the digital signal multiplexing apparatus of the embodiment.

Figs. 4A and 4B are schematic diagrams illustrating the change in the sub channel size at the input/output of a time interleave circuit during multiplex re-configuration according to the digital signal multiplexing apparatus of the embodiment.

Figs. 5A to 5B are schematic diagrams illustrating switching timings when an encode control circuit outputs a control signal during multiplex re-configuration according to the digital signal multiplexing apparatus of the embodiment.

Fig. 6 is a flow chart illustrating the operation of a CPU upon reception of a command according to the digital signal multiplexing apparatus of the embodiment.

Fig. 7 is a schematic diagram showing the transmission format used by the digital signal multiplexing apparatus of the embodiment.

Fig. 8 is a schematic diagram showing the relationship between a CIF, a sub channel and a CU used by the digital signal multiplexing apparatus of the embodiment.

Fig. 9 is a schematic diagram showing the FIB format used by the digital signal multiplexing apparatus of the embodiment.

Fig. 10 is a schematic diagram showing the format of the FIG field of a type "0" used by the digital signal multiplexing apparatus of the embodiment.

Fig. 11 is a schematic diagram showing the format of the FIG field of a type "0" and an extension "1" used by the digital signal multiplexing apparatus of the embodiment.

Fig. 12 is a schematic diagram showing the format of the FIG field of a type "0" and an extension "0" used by the digital signal multiplexing apparatus of the embodiment.

Figs. 13A to 13C are schematic diagrams illustrating switching by a convolution encoder used during multiplex re-configuration according to the digital signal multiplexing apparatus of the embodiment.

Fig. 14 is a table showing the relationship between an index and a sub channel size (puncturing information) according to the digital signal multiplexing apparatus of the embodiment.

Fig. 15 is a block diagram showing the structure of a convolution encoder used by the digital signal multiplexing apparatus of the embodiment.

Fig. 16 is a table showing the relationship between an index and a protective profile according to the digital signal multiplexing apparatus of the embodiment.

Fig. 17 is a table showing puncturing vectors of the digital signal multiplexing apparatus of the embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The digital signal multiplexing apparatus of this invention will be described in connection with preferred embodiments. Fig. 1 is a block diagram showing the structure of a digital signal processing apparatus according to an embodiment of the invention, in which one channel c of MPEG audio signals and another channel c' of MPEG audio signals are used as service data to be multiplexed.

Prior to the description of the digital signal multiplexing apparatus according to the embodiment of the invention, the fundamental data structure stipulated in the DAB specification (European Telecommunication Standard, ETS300 401) will be briefly described.

As shown in Fig. 7, a transmission frame is constituted of a sync channel (Sync), an FIC and an MSC. FIC is constituted of a plurality of data blocks of 256 bits called a fast information block (hereinafter represented by FIB where applicable). FIB has control information about service data multiplexed as MSC, and the essential part of this control information is multiplex information data called an MCI. FIC is not time-interleaved, whereas MSC is time-interleaved.

As shown in Fig. 7, MSC is constituted of one common interleaved frame (hereinafter represented CIF where applicable) if the transmission mode is "2" or "3, or of four CIF's if the transmission mode is "1". CIF is

data of MPEG audio signals made of frames of 24 ms period and a plurality of encoded service data sets multiplexed in the unit of 24 ms frame. This frame is a basic unit of time interleave process. The structure of this frame is shown in Fig. 8. The relationship between CIF and MSC is as shown in Fig. 7.

As shown in Fig. 8, CIF is constituted of a plurality of sub channels. A sub channel means encoded service data. CIF is constituted of addressable capacity units (hereinafter represented by CU where applicable). CU is made of 64 bits, and CIF is made of 55296 bits. Therefore, CIF is constituted of 864 CU's. In Fig. 8, a term "SubChId" means a sub channel identification symbol.

A general structure of FIB is shown in Fig. 9. FIB is constituted of a plurality of fast information groups (hereinafter represented by FIG where applicable) called a data group and a cyclic redundancy code (CRC). FIG is constituted of a FIG header and a FIG data field. The FIG header is made of three bits (b7 to b5) indicating an FIG type and five bits (b4 to b0) indicating a length of the FIG data field.

The FIG data field for a FIG type "0" is structured as shown in Fig. 10. C/N at the bit b7 is a flag indicating whether the FIG data field is current or next multiplex information. The bits b4 to b0 (extension bits) are an identification code indicating the type of contents of the FIG data field, and essential information about the multiplex configuration is stored in the extensions "0" and "1".

The FIG data field for the FIG type "0" and for the extension "1" (FIG 0/1 is shown in Fig. 11. Ten bits from the bit b9 to b0 indicate a start address (0 to 863) of CU. Of a term "short/long form", the short form indicates audio service and the long form indicates data service. The size and protection of the short form is indicated by indices.

The FIG data field for the FIG type "0" and for the extension "0" (FIG 0/0) is shown in Fig. 12. In Fig. 12, thirteen bits from the bit b12 to b0 labeled as "CIF COUNT" indicate a count of a CIF counter for counting succeeding CIF's. Of these bits, five bits from the bit b12 to b8 are upper bits of the CIF counter, and the remaining eight bits from the bit b7 to b0 are lower bits of the CIF counter. A change flag is a flag indicating a presence/absence of multiplex re-configuration. If this flag is "00", it means no multiplex re-configuration and in this case an occurrence change is not added. In other cases, eight bits of the occurrence change are added.

Time interleave is performed between frames and the depth of time interleave has sixteen variations over the range from the 0-th frame to 15-th frame. Therefore, a time interleave process takes a time corresponding to 15 frames at a maximum, and this process time is required to be considered when multiplex re-configuration occurs.

In Figs. 13A to 13C, the abscissa represents the number of frames and the ordinate represents a bit rate (bits per frame). Fig. 13A shows a sub channel No. 1 before time interleave. If the units increase from four CU's to six CU's, the bit rate changes at time t2, and if the units decrease from six CU's to four CU's, the bit rate changes at time t3. Fig. 13B shows a sub channel No. 2 before time interleave. If the units decrease from six CU's to four CU's, the bit rate changes at time t1, and if the units increase from four CU's to six CU's, the bit rate changes at time t4. The periods between the times t1 and t2 and between the times t3 and t4 are each 15 frames.

Fig. 13C shows sub channels after time interleave. The time t2 corresponds to the first occurrence change position, i.e., the first switching position, and the time t4 corresponds to the second occurrence change position, i.e., the second switching position. The period between the times t2 and t4 corresponds to a fixed number of frames which is stipulated to be 250 frames at a minimum.

Returning back to Fig. 1, a controller 1 such as a personal computer generates multiplex configuration information (MCI) of a DAB format (i.e., assembles fast information block (FIB)) and generates a command having contents matching MCI, the command being used as a control signal for an MSC encoder. FIB including MCI of the DAB format is indicated at a and the command having contents matching MCI and generated as a control signal for the MSC encoder is indicated at b. The controller 1 communicates with a CPU 3 via an interface circuit 2.

FIB data (multiplex configuration data) a of the DAB format is stored in a memory circuit 4 via and under the control of CPU 3. The stored FIB data (multiplex configuration data) a is read synchronously with a count of a CIF counter 7 which is a frame counter for counting CIF's in the unit of frame. The read FIB data is scrambled by a scramble circuit 5, and convolution-encoded by a convolution encoder 6 and output therefrom as FIC data f.

Commands for MSC encoders 150 and 151 are converted by CPU 3 into commands easy to be processed by the encoders 150 and 151, and input to an encoder control circuit 8. Control signals d and e output from the encoder control circuit 8 are supplied synchronously with a count of the CIF counter 7 to a convolution encoder 10 and a multiplexer circuit 12 serving as a main service multiplexer, respectively.

An MPEG audio signal c of one service data input to the MSC encoder 150 is scrambled by a scramble circuit 9, convolution-encoded by the convolution encoder 10 which is controlled by the control signal d, and time-interleaved by a time interleave circuit 11.

Similarly, another MPEG audio signal c' of the other service data input to the MSC encoder 151 is scrambled, convolution-encoded, and time-interleaved.

The MPEG audio signal c time-interleaved and output from the MSC encoder 150 and MPEG audio signal c' time-interleaved and output from the MSC encoder

151 are multiplexed and converted into MSC data (CIF) by the multiplexer circuit 12 which is controlled by the control signal e from the encoder control circuit 8. The MSC (CIF) data d multiplexed by the multiplexer circuit 12 is further multiplexed with the FIC data f by another multiplexer circuit 13 which is a transmission multiplexer, and output as a DAB transmission frame.

The operation of the digital signal multiplexing apparatus of this embodiment constructed as above will be described. In correspondence with two types of the multiplex re-configuration, terms such as service A, index A and start address A are used for one type and terms such as service B, index B and start address B are used for the other type.

A user first designates from the controller 1 "0" or "1" to set the multiplex re-configuration flag, one of "0 to 249" to set the occurrence change position, one of "0 to 863" to set the start address A, one of "0 to 63" to set the index address A, one of "0 to 863" to set the start address B, and one of "0 to 63" to set the index B.

These values set by the user are supplied, as the commands b, from the controller 1 to the interface circuit 2 and to CPU 3 which converts the commands b into data easy to be processed by the encoders. The converted data is supplied to the control circuit 8.

In accordance with the values set by the user, the controller 1 generates FIB data a. This FIB data a is generated by setting the start address, table index and index (size) of the FIG data field for the FIG type "0" and for the extension "1" (FIG 0/1) (refer to Fig. 11). If the re-configuration flag is "1", i.e., if the multiplex re-configuration is instructed, the occurrence change value set by the user is set to the occurrence change position of the FIG data field for the FIG type "0" and for the extension "0" (FIG 0/0) (refer to Fig. 12).

The FIG data fields of FIG (0/1) and FIG (0/0) set with the above values are added with the FIG headers in conformity with the formats shown in Figs. 9 and 10. In accordance with the format shown in Fig. 9, other FIG's are multiplexed and a CRC is added to thereby obtain the FIB data a. The FIB data a of 500 frames converted in the above manner is supplied via the interface circuit 2 to CPU 3.

Setting the number of frames to 500 frames allows multiplexing of two service data sets from the following reason. As described with Figs. 13A to 13C, the minimum number of frames between the first and second occurrence positions is stipulated to be 250 frames. This means that the multiplex configuration of at least 250 frames is not changed so that 500 frames are sufficient to realize multiplexing of two service data sets.

If the multiplex re-configuration flag is set, in one frame of service (A) among 500 frames, the start address A and index A are set to FIG (0/1) whose C/N flag (refer to Fig. 10) is "0 (current multiplex configuration)", whereas the start address B and index B are set to FIG (0/1) whose C/N flag (refer to Fig. 10) is "1 (next multiplex configuration)".

In one frame of the other service (B) among 500 frames, the start address B and index B are set to FIG (0/1) whose C/N flag (refer to Fig. 10) is "0 (current multiplex configuration)", whereas the start address A and index A are set to FIG (0/1) whose C/N flag (refer to Fig. 10) is "1 (next multiplex configuration)".

If the multiplex re-configuration flag is not set, i.e., if there is no multiplex re-configuration, information of the start address and index is set in accordance with the format (FIG (0/1)) of the DAB specification. FIG (0/0) and FIG (0/1) in FIB constitute multiplex configuration information (MCI).

The CIF counter 7 for counting CIF's in the unit of frame is a 13-bit counter in which the upper five bits count from "0 to 19" and the lower eight bits count from "0 to 249" so that this counter is a base 5000 (20 x 250) frame counter.

The FIB data a of the FIB format generated by the controller 1, interface circuit 2 and CPU 3 is stored in the memory circuit 4. As described earlier, the capacity of the memory circuit 4 is set so that data of 500 frames can be stored which is the minimum necessary capacity for realizing multiplexing of two service data sets.

As described earlier, the multiplex configuration information is stipulated to be constant over 250 frames. Therefore, the capacity of the memory circuit 4 is required to store information of 500 frames in order to realize the multiplex configuration of two service data sets. In this connection, since the memory circuit 4 has a capacity of 500 frames, the most severe conditions that the configuration state changes most frequently, i.e., the state changes every one 250-th frame, can be simulated.

The memory circuit 4 stores therein information (FIG 0/1) of the start address and index in conformity with the DAB specification. In the digital signal multiplexing apparatus of this embodiment, two inputs are used. For example, assuming that SubChId of the MPEG audio signal c is "1", start address and index corresponding to the MPEG audio signal c are written in the start address and index of SubChId = 1 in the FiG (0/1) format. In the example shown in Fig. 2A, a start address "0" and index "11" are written. The FIG data stored in the memory circuit 4 is read synchronously with counting of the CIF counter 7.

For the storage contents of the memory circuit 4 with the multiplex configuration, as shown in Fig. 2B the multiplexing state of one service A and the other service B changes every one 250-th frame. The occurrence change is written in the format of FIG (0/0) at the position corresponding to the value of the lower eight bits of the CIF counter 7 where the multiplex re-configuration occurs. In this example, the occurrence change position is at "100". The start address and index are written in FIG (0/1). In this example, the start address A of the one service A is "0" and the index A is "11", whereas the start address B of the other service B is "6" and the index B is "10".

The FIB multiplexing data a generated in the above manner and stored in the memory circuit 4 is read synchronously with counting CIF's by the CIF counter 7, scrambled, convolution-encoded, and sent to the multiplexer circuit 13.

The MPEG audio signal c as the one service data is scrambled by the scramble circuit 9 and convolution-encoded by the convolution encoder 10. For the convolution encoding, convolution puncturing and the like are switched in accordance with the index corresponding to the command d output from the encoder control circuit 8. After the convolution encoded output is time interleaved by the time interleave circuit 11, it is multiplexed with the other service data by the multiplexer circuit 12 which is controlled by the control signal e output from the encoder control circuit 8, and further multiplexed as a DAB transmission format.

Next, the operation of the convolution encoder 10 will be described. Each index corresponding to the command d for the MPEG audio signal c output from the encoder control circuit 8 is allocated with a sub channel size, a protection size representative of error correction intensity, and a bit rate to thereby determine the sub channel size (the number of bits per frame) for an output of the convolution encoder 10. Namely, in accordance with the index, the convolution encoder 10 performs puncturing and outputs the time interleaved MPEG audio signal c having the stipulated size.

More in particular, the number of bits input to the convolution encoder 10 in the unit of frame depends on the index. For example, if the index is 11, the bit rate is 56 kbps as shown in Fig. 14, and 1344 (56 x 24) bits per frame are input to the convolution encoder 10 since one frame is 24 ms. As shown in Fig. 15, the convolution encoder 10 is constituted of a shift register 27 made of six one-bit delays 21 to 26 and modulo-2 adders 28 to 38, and has a constraint length of "7" and an encoding factor of 1/4. Therefore, input data is converted into a mother code of 5400 (1344 x 4 + 24) bits.

Of 5400 bits, the first 5376 (128 x 42) bits are divided into 42 blocks each having 128 bits. 42 blocks are classified into levels (L1 to L4) of "6", "10", "23" and "3" corresponding to the index "11" of an audio service component protection profile of the DAB standard shown in Fig. 16. These four levels are allocated with puncturing indices (PI1 to PI4) of "9", "6", "4" and "5".

The 42 blocks are divided into sub blocks of 32 bits and punctured in accordance with puncturing vectors of the DAB specification shown in Fig. 17, by using as parameters the above described puncturing indices (a puncturing index "9" for the first 6 blocks, a puncturing index "6" for the next 10 blocks, a puncturing index "4" for the next 23 blocks, and a puncturing index "5" for the last 3 blocks). The remaining 24 bits as tail bits are punctured in a predetermined manner.

Convolution puncturing is switched in accordance with indices as described above. Namely, the encoding factor is changed by using the index as a parameter. Data punctured in the above manner, in this example, 35 CU's or 2240 bits, are output. This output from the convolution encoder 10 is time interleaved. Similar operations are executed also by the encoder 151.

Time interleaved data output from the encoders 150 and 151 is multiplexed by the multiplexer circuit 12 which is supplied with the start address and size as the control signal e from the encoder control circuit 8. This multiplexing will be further detailed. The multiplexing position is determined from the start address and the size obtained basing upon the index. Figs. 3A, 3B-1 and 3B-2 are diagrams illustrating multiplexing positions of CIF's.

An example shown in Fig. 3A has no multiplex re-configuration. In this example, the start address is "0" and the index is "11" so that the sub channel size is 35 CU's (refer to Fig. 14). Multiplexing is executed from 0-th CU to 34-th CU. Since each CU has 64 bits, multiplexed data is a multiple of 64 bits. Examples shown in Figs. 3B-1 and 3B-2 have multiplex re-configuration. In these examples, the service A state (Fig. 3b-1) and service B state (Fig. 3B-2) switch every one 250-th frame. In the service B state, the start address is set to 6-th CU (Fig. 3B-2).

If there is no multiplex re-configuration, the values of the start address and index are constant. As shown in Figs. 13A to 13C, if there is multiplex re-configuration and the bit rate becomes small, in this case if the service A state changes to the service B state, the state is changed 15 frames before the occurrence change because the index supplied to the convolution encoder 10 is for the period before time interleave. If the service B state changes to the service A state, the state changes at the occurrence change position.

The data used at the multiplexer circuit 12 is for the period after interleave. Therefore, the state changes always at the occurrence change position.

This will be described with reference to Figs. 4A and 4B. Fig. 4A shows the sub channel size before time interleave, and Fig. 4B shows the sub channel size after time interleave. The lower 8 bits of the count of the CIF counter 7 are illustrated in Fig. 5A. As shown in Fig. 5B, the LSB (5-th bit) of the upper 5 bits inverts when the counter counts 250 CIF's. The index supplied from the encoder control circuit 8 to the convolution encoder 10 is switched at the timing shown in Fig. 5C. Namely, the service A changes to the service B at the timing 15 frames before the 100-th frame. The start address and sub channel size supplied from the encoder control circuit 8 to the multiplexer circuit 12 are switched at the timing shown in Fig. 5D. Namely, switching from the service A to service B or vice versa is always executed at the 100-th frame or occurrence change position.

The controller 1 transfers as the command the multiplex configuration data same as that written in the memory circuit 4 to CPU 3. The contents of the command include the multiplex re-configuration flag, occurrence change position, start address A, index A, start

address B and index B.

The operation of CPU 3 is illustrated in the flow chart shown in Fig. 6. When a command is received, it is checked whether the multiplex re-configuration flag is set (Step S1). If it is judged at Step S1 that the multiplex re-configuration flag is not set, the sub channel size of the service A is calculated (Step S2). Calculation of the sub channel size corresponds to reference to the table shown in Fig. 14 by using the index as a search key. After Step S2, the start address A, sub channel size A and index A are output (Step S3) as indicated Process "1" in Fig. 6.

If it is judged at Step S1 that the multiplex re-configuration flag is set, the sub channel sizes of the services A and B are calculated (Step S4). After Step S4, it is checked whether the sub channel size of the service A is larger than that of the service B (Step S5).

If it is judged at Step S5 that the sub channel size of the service A is larger than that of the service B, the processes corresponding to the following are executed and the results are output (Step S6) as indicated Process "2" in Fig. 6.

Start address A, Sub channel Size A, Index A,
Start address B, Sub channel Size B, Index B,
Occurrence Change A = Occurrence Change,
Occurrence Change B = Occurrence Change - 15,
Occurrence Change C = Occurrence Change.

If it is judged at Step S5 that the sub channel size of the service A is not larger than that of the service B, it is checked whether the sub channel size of the service A is equal to that of the service B (Step S7).

If it is judged at Step S7 that the sub channel size of the service A is equal to that of the service B, the processes corresponding to the following are executed and the results are output (Step S8) as indicated Process "3" in Fig. 6.

Start address A, Sub channel Size A, Index A,
Start address B, Sub channel Size B, Index B,
Occurrence Change A = Occurrence Change,
Occurrence Change B = Occurrence Change,
Occurrence Change C = Occurrence Change.

If it is judged at Step S7 that the sub channel size of the service A is not equal to that of the service B, the processes corresponding to the following are executed and the results are output (Step S9) as indicated Process "4" in Fig. 6.

Start address A, Sub channel Size A, Index A,
Start address B, Sub channel Size B, Index B,
Occurrence Change A = Occurrence Change - 15,
Occurrence Change B = Occurrence Change,
Occurrence Change C = Occurrence Change.

One of the outputs obtained by the processes (1) to (4) is supplied to the encoder control circuit 8. If the multiplex re-configuration flag is "0" (if the output of the process "1" is supplied), the index A is supplied to the convolution encoder 10 and the start address A and size A are supplied to the multiplexer circuit 12.

If the multiplex re-configuration flag is "1" (if one of the outputs obtained by the processes "2" to "4" is supplied), the index to be supplied to the convolution encoder 10 is switched to the index A at the timing of the occurrence change A for the odd frame (LSB "0" of the upper five bits of the count of the CIF counter), or switched to the index B at the timing of the occurrence change B for the even frame (LSB "1" of the upper five bits of the count of the CIF counter).

The start address and sub channel size supplied to the multiplexer circuit 12 are switched to the start address A and sub channel size A at the timing of the occurrence change C for the odd frame, and switched to the start address B and size B at the timing of the occurrence change C for the even frame.

As described above, according to the digital signal multiplexing apparatus of this invention, service data having a plurality of difference bit rates can be multiplexed so as to meet the multiplex configuration information designated in advance by a user, and the bit rate can be made variable even during signal transmission.

Claims

1. A digital signal multiplexing apparatus for multiplexing, time divisionally on a baseband, a plurality of service data sets having different bit rates comprising:

information generating means for generating multiplex configuration information indicating how service data sets are multiplexed, in accordance with designated information, and generating a command whose contents match the multiplex configuration information;

a memory circuit for storing the multiplex configuration information generated by said information generating means;

means for controlling to write the multiplex configuration information into said memory circuit and converting the command generated by said information generating means into control signals for encoders;

a first encoder for encoding the multiplex configuration information read from said memory circuit in accordance with a predetermined format;

second encoders for encoding the plurality of service data sets in accordance with the con-

trol signals converted by said controlling and converting means and in accordance with predetermined formats;

a first multiplexer circuit for multiplexing the plurality of service data sets encoded by said second encoders; and

a second multiplexer circuit for multiplexing the data encoded by said first encoder and the data multiplexed by said first multiplexer circuit.

2. A digital signal multiplexing apparatus according to claim 1, further comprising an encoder control circuit for switching control signals of said second encoders at each designated frame in accordance with the plurality of multiplex configuration information data sets read from said memory circuit, wherein the multiplexing states are periodically changed while retaining a time sequential continuity.

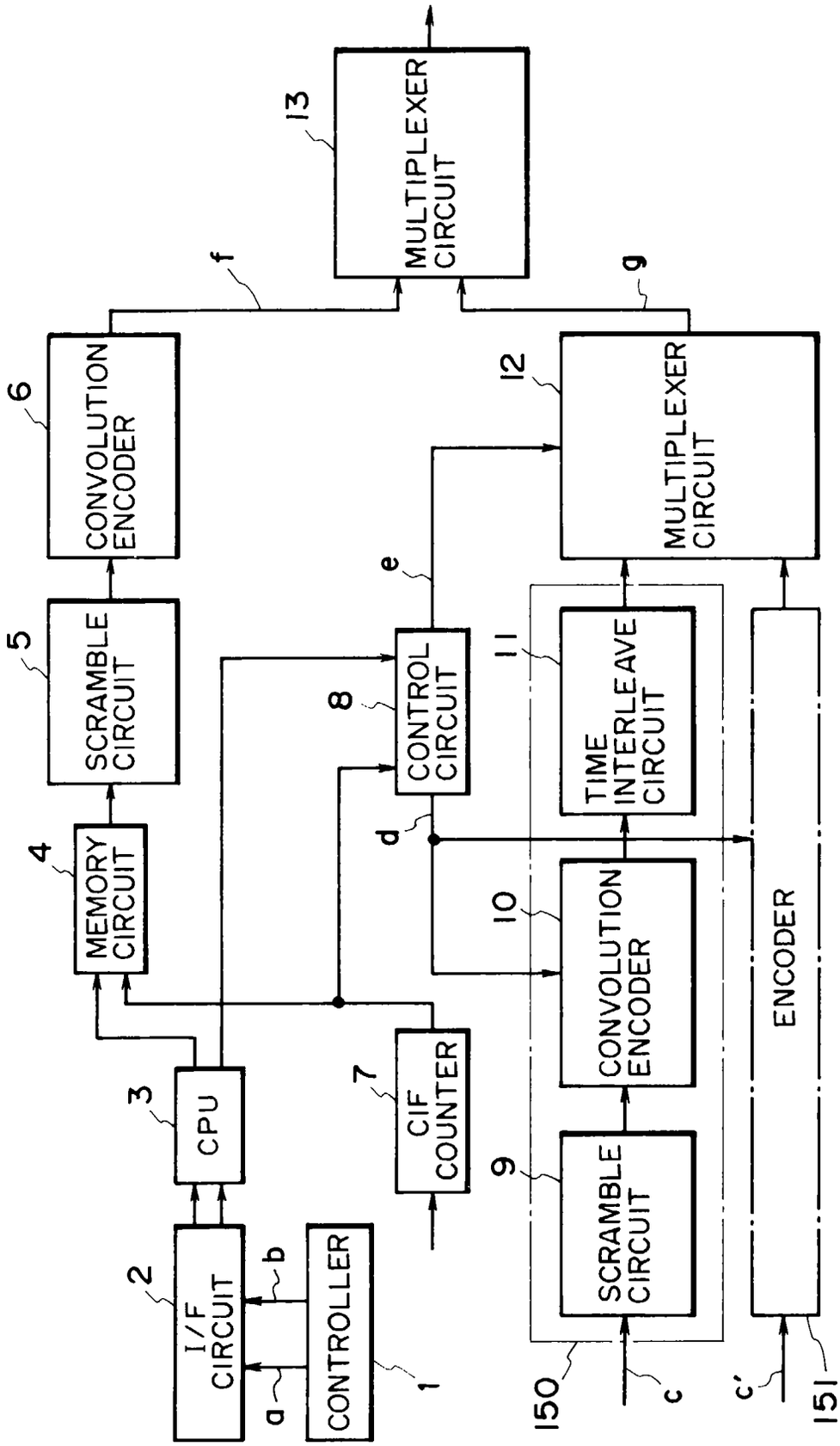
CONTROLLER
1
I/F CIRCUIT
2
CPU
3
MEMORY CIRCUIT
4
SCRAMBLE CIRCUIT
5
CONVOLUTION ENCODER
6
CIF COUNTER
7
CONTROL CIRCUIT
8
SCRAMBLE CIRCUIT
9
CONVOLUTION ENCODER
10
TIME INTERLEAVE CIRCUIT
11
MULTIPLEXER CIRCUIT
12
MULTIPLEXER CIRCUIT
13
ENCODER
151
a
b
c
c'
d
e
f
g
150

FIG. 1

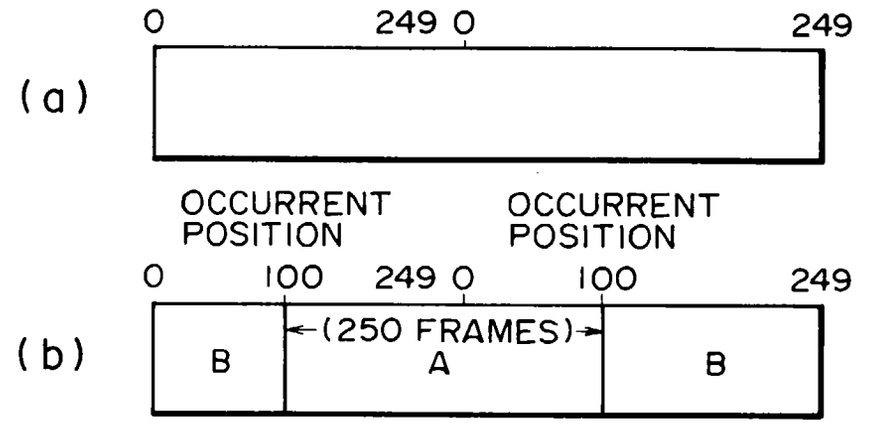
(a)
0
249 0
249
(b)
OCCURRENT POSITION
OCCURRENT POSITION
0
100
249 0
100
249
(250 FRAMES)
B
A
B

FIG. 2

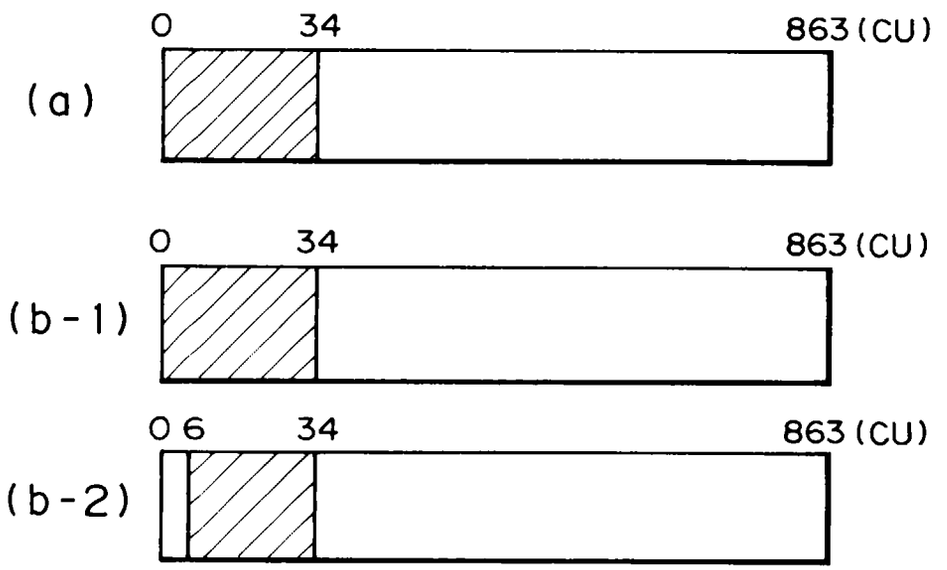
(a)
0
34
863 (CU)
(b-1)
0
34
863 (CU)
(b-2)
0 6
34
863 (CU)

FIG. 3

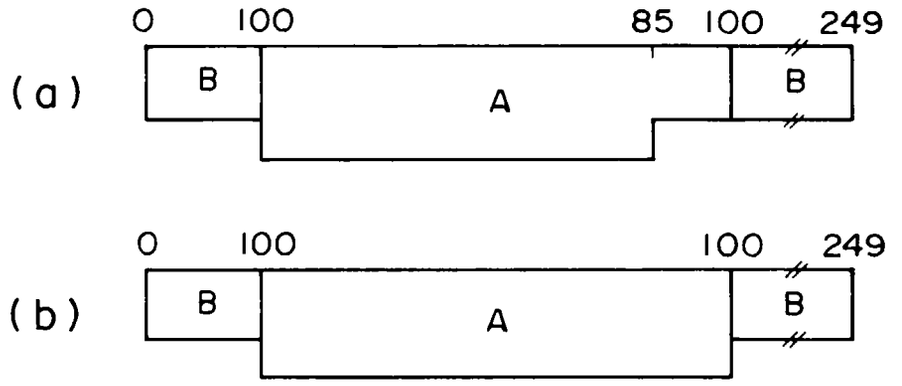
(a)
0
100
85
100
249
B
A
B
(b)
0
100
100
249
B
A
B

FIG. 4

(a)
0
100
249
0
85
100
249
(b)
(c)
B
A
B
(d)
B
A
B

FIG. 5

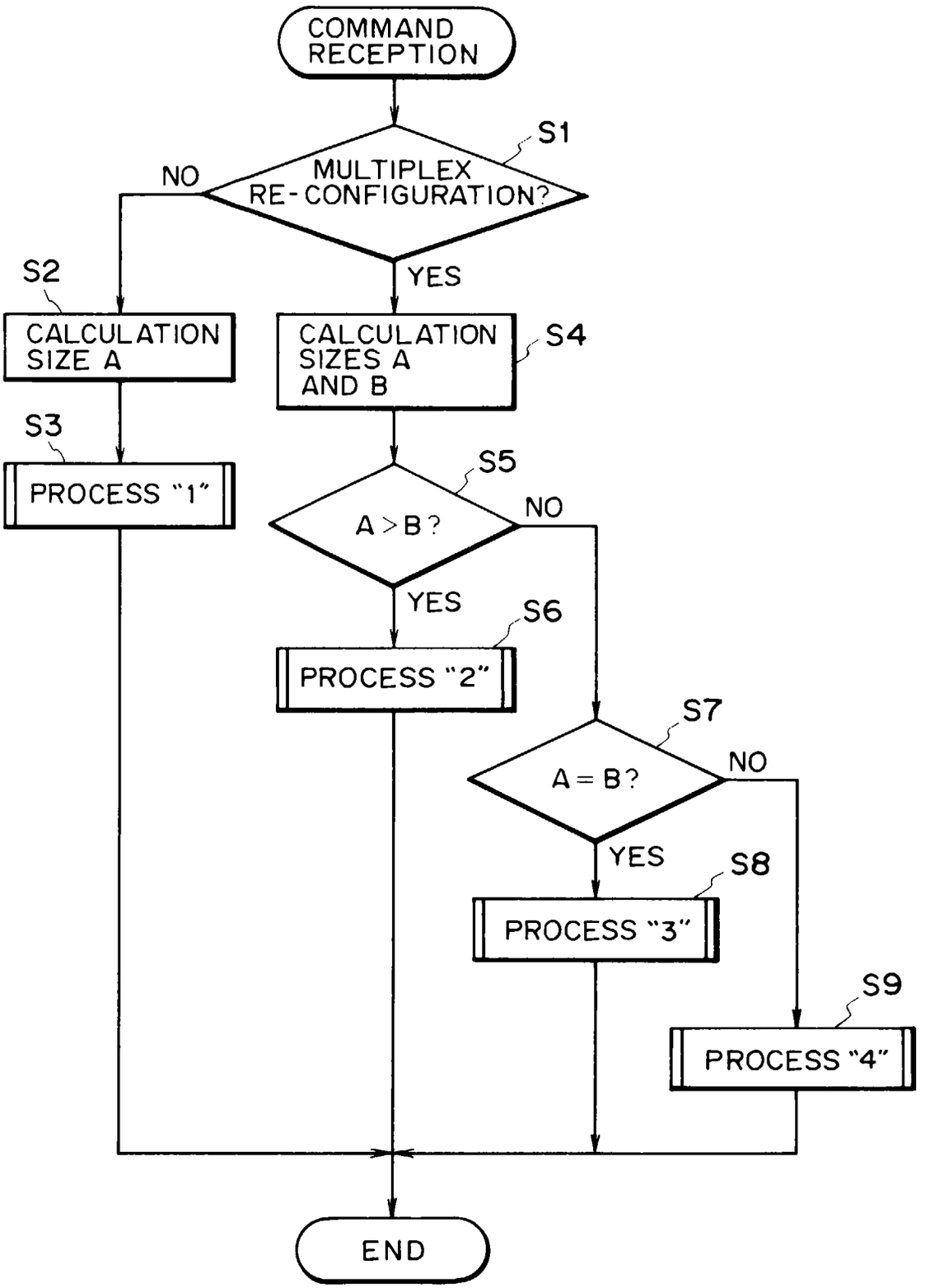
COMMAND RECEPTION
S1
MULTIPLEX RE-CONFIGURATION?
NO
YES
S2
CALCULATION SIZE A
S3
PROCESS "1"
CALCULATION SIZES A AND B
S4
S5
A > B ?
NO
YES
S6
PROCESS "2"
S7
A = B ?
NO
YES
S8
PROCESS "3"
S9
PROCESS "4"
END

FIG. 6

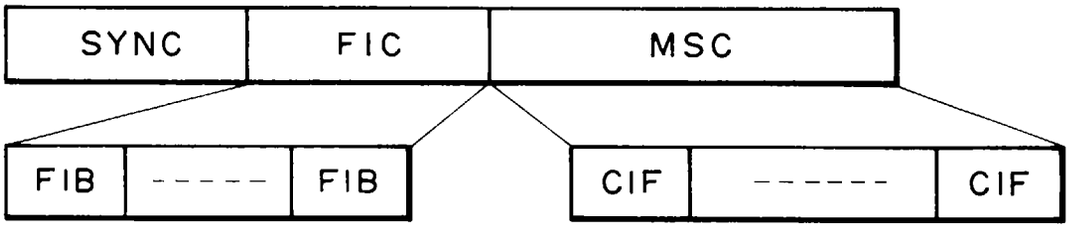

FIG. 7

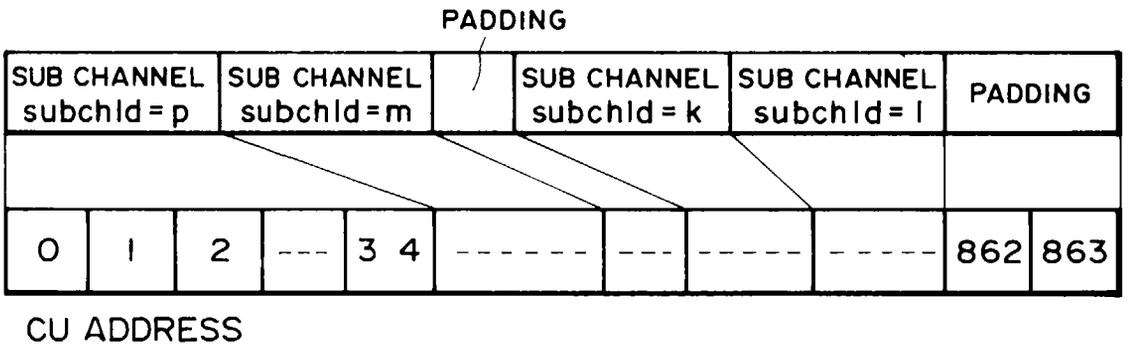

FIG. 8

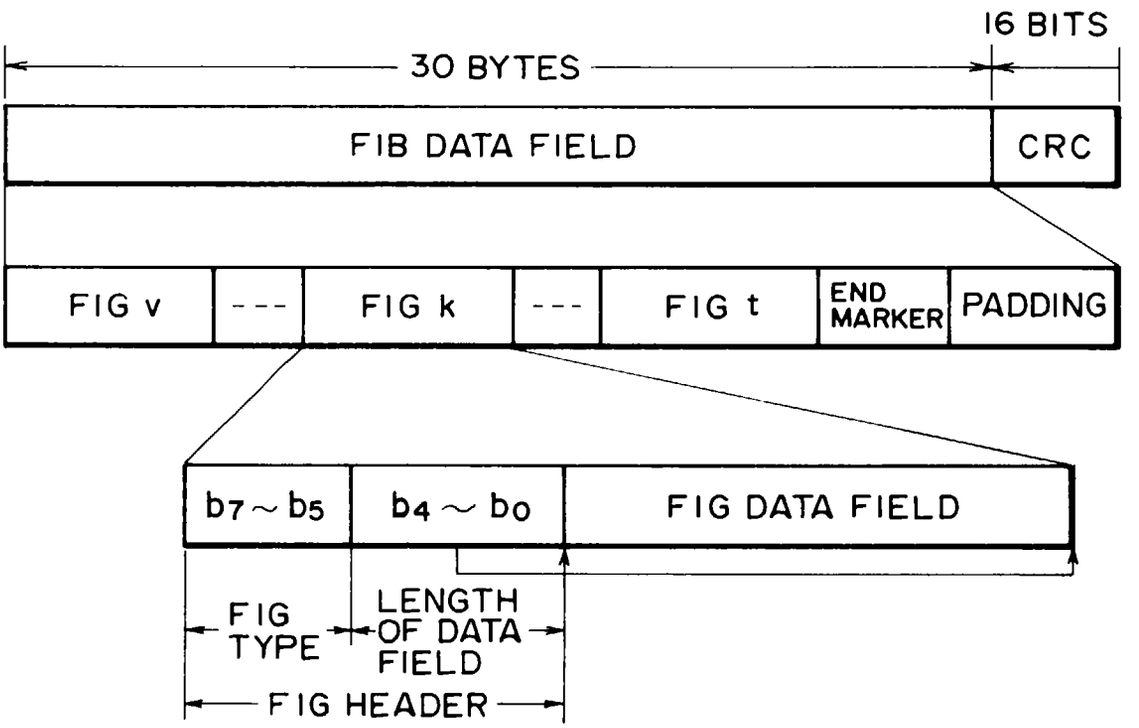

FIG. 9

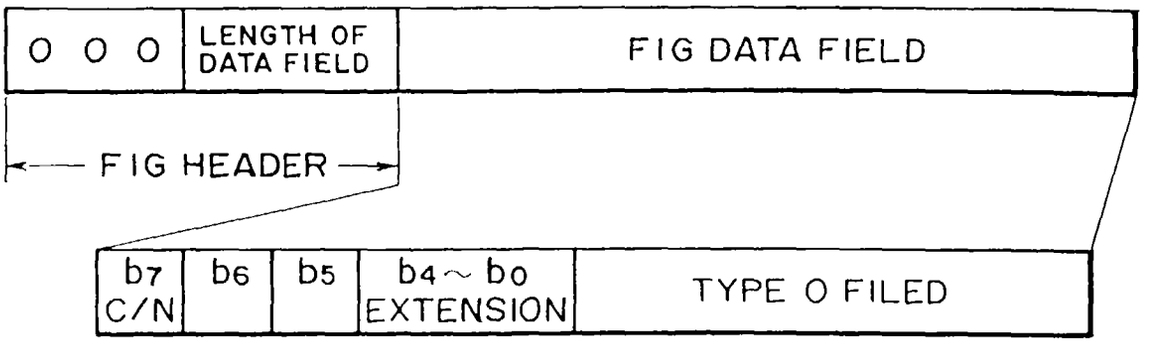

FIG. 10

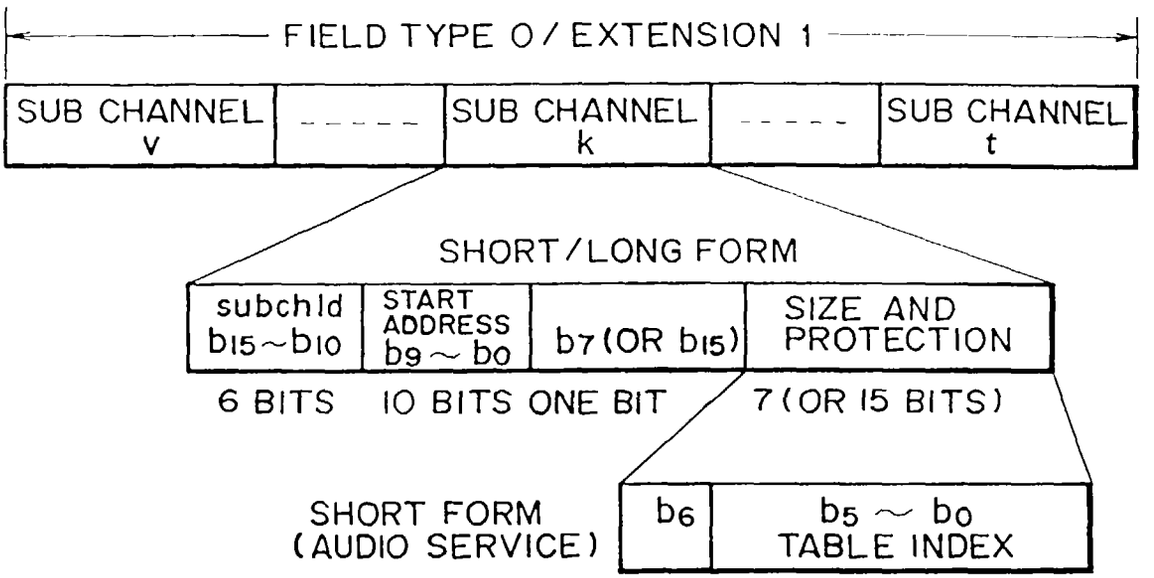

FIG. 11

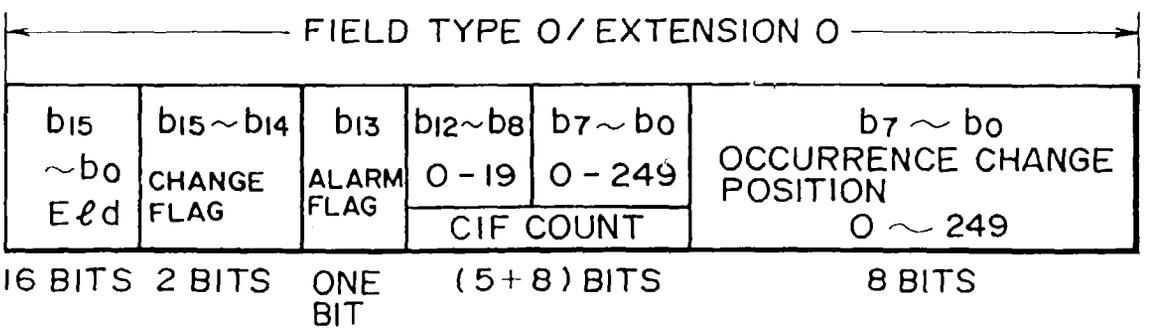

FIG. 12

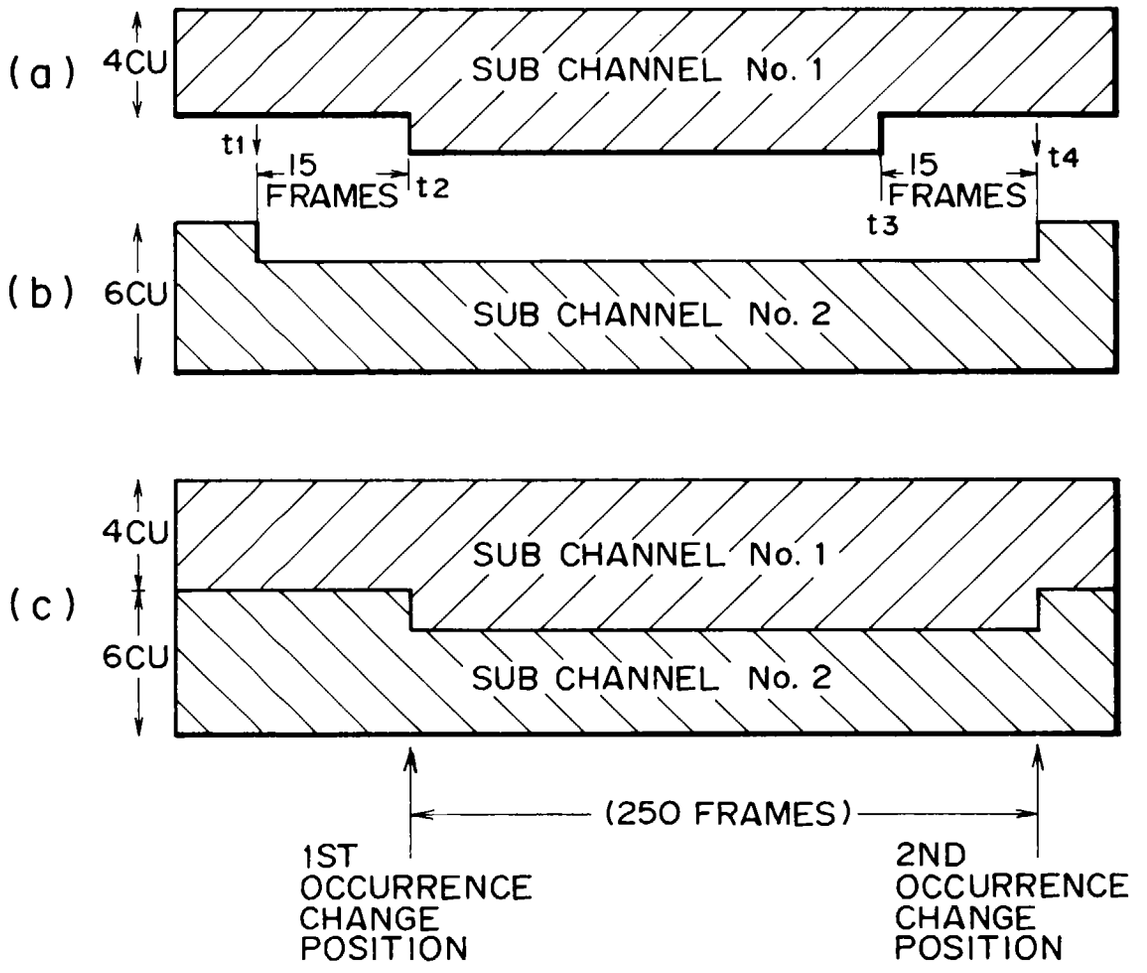
(a)
4CU
SUB CHANNEL No. 1
t1
15 FRAMES
t2
15 FRAMES
t3
t4
(b)
6CU
SUB CHANNEL No. 2
(c)
4CU
SUB CHANNEL No. 1
6CU
SUB CHANNEL No. 2
(250 FRAMES)
1ST OCCURRENCE CHANGE POSITION
2ND OCCURRENCE CHANGE POSITION

FIG. 13

INDEX	SUB CHANNEL SIZE(CU)	PROTECTION LEVEL	BIT RATE	INDEX	SUB CHANNEL SIZE(CU)	PROTECTION LEVEL	BIT RATE
0	16	5	32	33	64	5	128
1	21	4	32	34	84	4	128
2	24	3	32	35	96	3	128
3	29	2	32	36	116	2	128
4	35	1	32	37	140	1	128
5	24	5	48	38	80	5	160
6	29	4	48	39	104	4	160
7	35	3	48	40	116	3	160
8	42	2	48	41	140	2	160
9	52	1	48	42	168	1	160
10	29	5	56	43	96	5	192
11	35	4	56	44	116	4	192
12	42	3	56	45	140	3	192
13	52	2	56	46	168	2	192
	×			47	208	1	192
14	32	5	64	48	116	5	224
15	42	4	64	49	140	4	224
16	48	3	64	50	168	3	224
17	58	2	64	51	208	2	224
18	70	1	64	52	232	1	224
19	40	5	80	53	128	5	256
20	52	4	80	54	168	4	256
21	58	3	80	55	192	3	256
22	70	2	80	56	232	2	256
23	84	1	80	57	280	1	256
24	48	5	96	58	160	5	320
25	58	4	96	59	208	4	320
26	70	3	96		×		
27	84	2	96	60	280	2	320
28	104	1	96		×		
29	58	5	112	61	192	5	384
30	70	4	112		×		
31	84	3	112	62	280	3	384
32	104	2	112		×		
	×			63	416	1	384

FIG. 14

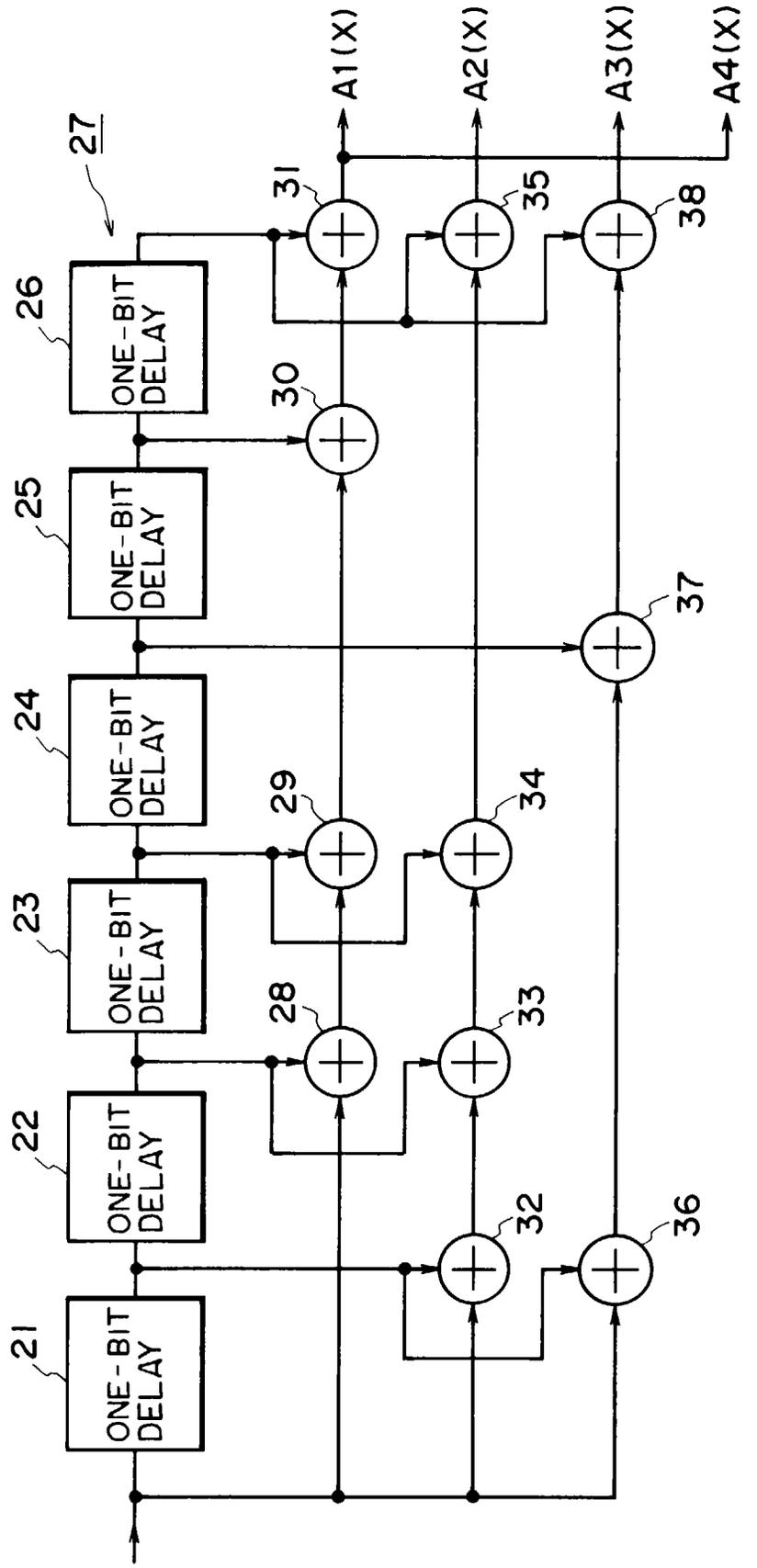
A1(X)
A2(X)
A3(X)
A4(X)
27
26
25
24
23
22
21
ONE-BIT DELAY
31
30
29
28
32
33
34
35
36
37
38

FIG. 15

INDEX	AUDIO BIT RATE (kbit/s)	P	L_1	L_2	L_3	L_4	PI_1	PI_2	PI_3	PI_4
0	32	5	3	4	17	0	5	3	2	—
1	32	4	3	3	18	0	11	6	5	—
2	32	3	3	4	14	3	15	9	6	8
3	32	2	3	4	14	3	22	13	8	13
4	32	1	3	5	13	3	24	17	12	17
5	48	5	4	3	26	3	5	4	2	3
6	48	4	3	4	26	3	9	6	4	6
7	48	3	3	4	26	3	15	10	6	9
8	48	2	3	4	26	3	24	14	8	15
9	48	1	3	5	25	3	24	18	13	18
10	56	5	6	10	23	3	5	4	2	3
11	56	4	6	10	23	3	9	6	4	5
12	56	3	6	12	21	3	16	7	6	9
13	56	2	6	10	23	3	23	13	8	13
14	64	5	6	9	31	2	5	3	2	3
15	64	4	6	9	33	0	11	6	5	—
16	64	3	6	12	27	3	16	8	6	9
17	64	2	6	10	29	3	23	13	8	13
18	64	1	6	11	28	3	24	18	12	18
19	80	5	6	10	41	3	6	3	2	3
20	80	4	6	10	41	3	11	6	5	6
21	80	3	6	11	40	3	16	8	6	7
22	80	2	6	10	41	3	23	13	8	13
23	80	1	6	10	41	3	24	17	12	18
24	96	5	7	9	53	3	5	4	2	4
25	96	4	7	10	52	3	9	6	4	6
26	96	3	6	12	51	3	16	9	6	10
27	96	2	6	10	53	3	22	12	9	12
28	96	1	6	13	50	3	24	18	13	19
29	112	5	14	17	50	3	5	4	2	5
30	112	4	11	21	49	3	9	6	4	8
31	112	3	11	23	47	3	16	8	6	9

FIG. 16

PI=1 : code rate:8/9	1100	1000	1000	1000	1000	1000	1000	1000
PI=2 : code rate:8/10	1100	1000	1000	1000	1100	1000	1000	1000
PI=3 : code rate:8/11	1100	1000	1100	1000	1100	1000	1000	1000
PI=4 : code rate:8/12	1100	1000	1100	1000	1100	1000	1100	1000
PI=5 : code rate:8/13	1100	1100	1100	1000	1100	1000	1100	1000
PI=6 : code rate:8/14	1100	1100	1100	1000	1100	1100	1100	1000
PI=7 : code rate:8/15	1100	1100	1100	1100	1100	1100	1100	1000
PI=8 : code rate:8/16	1100	1100	1100	1100	1100	1100	1100	1100
PI=9 : code rate:8/17	1110	1100	1100	1100	1100	1100	1100	1100
PI=10 : code rate:8/18	1110	1100	1100	1100	1110	1100	1100	1100
PI=11 : code rate:8/19	1110	1100	1110	1100	1110	1100	1100	1100
PI=12 : code rate:8/20	1110	1100	1110	1100	1110	1100	1110	1100
PI=13 : code rate:8/21	1110	1110	1110	1100	1110	1100	1110	1100
PI=14 : code rate:8/22	1110	1110	1110	1100	1110	1110	1110	1100
PI=15 : code rate:8/23	1110	1110	1110	1110	1110	1110	1110	1100
PI=16 : code rate:8/24	1110	1110	1110	1110	1110	1110	1110	1110
PI=17 : code rate:8/25	1111	1110	1110	1110	1110	1110	1110	1110
PI=18 : code rate:8/26	1111	1110	1110	1110	1111	1110	1110	1110
PI=19 : code rate:8/27	1111	1110	1111	1110	1111	1110	1110	1110
PI=20 : code rate:8/28	1111	1110	1111	1110	1111	1110	1111	1110
PI=21 : code rate:8/29	1111	1111	1111	1110	1111	1110	1111	1110
PI=22 : code rate:8/30	1111	1111	1111	1110	1111	1111	1111	1110
PI=23 : code rate:8/31	1111	1111	1111	1111	1111	1111	1111	1110
PI=24 : code rate:8/32	1111	1111	1111	1111	1111	1111	1111	1111

FIG. 17