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(71) Applicant: Hitachi, Ltd.  
Chiyoda-ku, Tokyo 101-0062 (JP)

(72) Inventors:  
• Furuhashi, Tsutomu  
Yokohama-shi, Kanagawa-ken (JP)  
• Nitta, Hiroyuki  
Fujisawa-shi, Kanagawa-ken (JP)

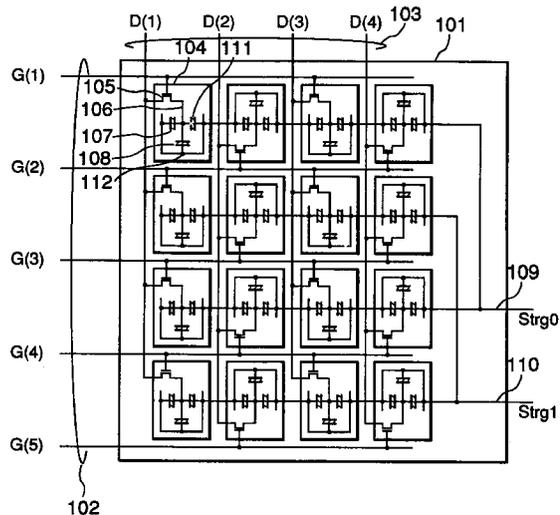
• Ooishi, Yoshihisa  
Yokohama-shi, Kanagawa-ken (JP)  
• Futami, Toshio  
Mobara-shi, Chiba-ken (JP)

(74) Representative:  
Altenburg, Udo, Dipl.-Phys. et al  
Patent- und Rechtsanwälte,  
Bardehle . Pagenberg . Dost . Altenburg .  
Frohwitter . Geissler & Partner,  
Galileiplatz 1  
81679 München (DE)

(54) Active matrix liquid crystal panel and liquid crystal display device with opposite electrodes divided in groups

(57) In driving the liquid crystal panel, the frequency of the base voltage applied to common electrodes is reduced without increasing flickering. Also, the deterioration of picture quality caused by concentration of current to the common electrodes is reduced. In a liquid crystal panel 101 having pixel portions 104, each including a thin film transistor, mounted thereon, a liquid crystal 107 and additional capacitors 108 as components of each pixel portion, have a common opposite electrode 112 on one side thereof opposite to the side where there is a pixel electrode 106. The opposite electrodes 112 of the pixel portions 104 connected to the same gate line 102 are divided in half and are respectively connected to two separate and opposite electrode lines 109, 110.

FIG.1



## Description

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The present invention relates to a liquid crystal display device having a liquid crystal panel of the active-matrix driving method type, and more particularly to a structure and a driving method of the liquid crystal panel.

#### Background Art

Among the liquid crystal panels for the liquid crystal display device, there is a liquid crystal panel of the active-matrix driving method type in which pixel portions, each formed of a TFT (Thin Film Transistor) and a pixel electrode, etc., are arranged on a transparent substrate having a liquid crystal sealed in (this panel is hereinafter referred to as the TFT crystal panel). JP-A-63-237095 discloses a liquid crystal display device for color display by applying gray-scale voltages corresponding to display data to the TFT liquid crystal panel.

Description will first be given of the conventional liquid crystal device using the TFT liquid crystal panel. Fig. 15 shows an equivalent circuit diagram of the TFT liquid crystal panel. In Fig. 15, a TFT crystal panel 201 comprises a plurality of gate lines 202 drawn extending horizontally, a plurality of drain lines 203 drawn extending vertically, pixel portions 204 each connected to a drain line 203 and a gate line 202, and a common electrode (Com) 209 and a common electrode (Strg) 210. Each pixel portion 204 includes a thin film transistor (TFT) 205, a pixel electrode 206, a liquid crystal 208, and an additional capacitor 207. The liquid crystal 208 is placed between the pixel electrode 206 and the common electrode (Com) 209, while the additional capacitor 207 is placed between the pixel electrode 206 and the common electrode (Strg) 210. The pixel portions 204 on the same row are driven by a voltage from one and the same gate line 202, while the pixel portions 204 on the same column are driven by a voltage from one and the same drain line 203.

Fig. 16 is a general block diagram of the liquid crystal display device. In Fig. 16, the liquid crystal display device comprises a liquid crystal panel 201 having the pixel portions arranged in an m-row n-column matrix, a liquid crystal controller 302 for outputting display data and various synchronizing signals, a drain driver 306 for applying data voltages according to display data to the drain lines 203, a gate driver 307 for applying a scanning voltage to the gate lines 202, AC voltage generating circuits 309, 310, and 313 for generating AC voltages to apply to the pixel portions 204, and a dividing resistance 311.

The liquid crystal controller 302, by means of a circuit shown in Fig. 7, sequentially latches and transfers

display data to the drain driver 306 in accordance with a data synchronizing signal 402. The liquid crystal controller 302, by means of a circuit shown in Fig. 8, generates an alternating signal 304 to specify the polarity of a base voltage derived from a vertical synchronizing signal 501 and a horizontal synchronizing signal 502, and outputs the alternating signal 304 to the AC voltage generating circuits 309, 310, 313. This alternating signal 304 fluctuates to invert the polarity of the voltage applied to the pixel portions 204 at each period of the horizontal synchronizing signal.

In the gate driver 307, as shown in the arrangement of Fig. 19, a shift register 603 shifts a synchronizing signal 601 which makes the selection of the first line effective in accordance with a synchronizing signal 602 of the same frequency as the horizontal synchronizing signal, and according to the logic level of an output 604, a level shifter 605 and a voltage selector circuit 607 cooperatively generate gate voltages G(1), G(2), G(3), ... for driving the liquid crystals, and apply the gate voltages to the gate lines 202. Thus, selective voltages to turn on TFT transistors 205 are applied to the gate lines 202 in the order of G(1), G(2), G(3).

In the drain driver 306, as shown in the arrangement in Fig. 20, a latch circuit 707 sequentially accepts display data and stores the data for one line in accordance with a sampling clock 706 generated by a shift register 705. Stored display data for one line is accepted all at once by a latch circuit 709 in accordance with a synchronizing signal 704 of the same frequency as in the horizontal synchronizing signal, then converted by a gray-scale voltages generating circuit 711 into drain voltages Vd according to a base voltage 312, and applied to the drain lines 203.

Meanwhile, if the polarity of the voltages applied to the liquid crystals 208 of the pixel portions 204 on the liquid crystal panel 201 remains the same during one frame period, flickering occurs on the screen. In this liquid crystal display device, to reduce the flickering, the AC voltage generating circuits 309, 310 and 313 are used to invert the polarity of the voltages applied to the pixel portions 204 at every line period.

The above-mentioned operation of the liquid crystal display device will be described with reference to Fig. 21.

In parallel with the gate driver 307 raising the voltage VG(2) of the gate line 202 for the second horizontal line to a selective voltage Vgon, the drain driver 306 applies the gray-scale voltages Vd according to the display data and the alternating signal for the second line to the drain lines 203. Accordingly, at the pixel portions 204 on the second line, the TFTs 205 turn on to apply gray-scale voltages Vd to the pixel electrodes 206, while a base voltage based on the alternating signal is applied to the common electrodes (Com, Strg) 209, 210. The potential difference between the gray-scale voltage and the base voltage controls the transmittance of each liquid crystal 208, and is maintained in the liquid crystal

208 and the additional capacitor 207 still after the voltage VG(2) becomes a non-selective voltage Vgoff and TFT 205 turns off.

When the gate driver 307 causes the voltage VG(2) to drop to the non-selective voltage Vgoff and causes the voltage VG(3) of the gate line 202 on the third line to rise to the selective voltage Vgon, the drain driver 306 outputs gray-scale voltages Vd according to display data and the alternating signal of the third line. The driving operation as mentioned above is performed for the pixel portions 204 on the third line.

In the above operation, when the base voltage level applied to the common electrodes (Com, Strg) 209, 210 is at a positive polarity level of VcomP, the gray-scale voltages Vd of negative polarity are applied to the pixel electrodes 206 of the pixel portions 204 on the line which is the driving object, so that the potential differences at the liquid crystals 208 and the additional capacitors 207 are of negative polarity with respect to the base voltage. Conversely, when the base voltage of the common electrodes (Com, Strg) 209, 210 is at a negative polarity level of VcomN, the potential differences at the liquid crystals 208 and the additional capacitors 207 are of positive polarity.

As has been described, in the conventional liquid crystal display device, the additional capacitors 207 of all pixel portions 204 are connected to the common electrode Strg 210, and the additional capacitors 207 of the respective pixel portions 204, each having a larger capacitance than the liquid crystals 208, maintain their potential difference of the same polarity in each row. Therefore, when voltages of different polarity are applied to the additional capacitors 207 when driving the pixel portions 204, currents flow in a concentrated manner between the additional capacitors 207 of pixel portions 204 driven simultaneously and the common electrode Strg 210, and due to the wiring resistance of the common electrode and the effects of the additional capacitors, distortion occurs in the voltage on the common electrode. Owing to this distortion, in the conventional liquid crystal display device, the applied voltages on the liquid crystals 208 deviate from the originally applied voltages corresponding to the display data, resulting in a deterioration of picture quality, which has been a problem.

In the conventional liquid crystal display device, to prevent the occurrence of flickering, the base voltage to be applied to the common electrodes is made an AC voltage whose polarity is inverted at every row. Therefore, it has been necessary to fluctuate the voltage applied to the common electrodes at a high frequency of 30 kHz to 60 kHz, which leads to unreasonable power consumption.

#### SUMMARY OF THE INVENTION

An object of the present invention is to reduce the frequency of the voltage applied to the common elec-

trodes without increasing flickering. Another object of the present invention is to reduce the deterioration of picture quality due to the concentrated flow of current into the common electrodes.

In order to achieve the above objects, in the present invention there is provided a liquid crystal panel having two substrates arranged facing each other and a liquid crystal filled in between the two substrates, the liquid crystal panel comprising:

M x N pixel portions arranged in an M-row N-column matrix on the substrate so as to correspond to pixels arranged in an M-row N-column matrix;

a plurality of drain lines;  
a plurality of gate lines; and  
two opposite electrode lines,

wherein each pixel portion comprises: a thin film transistor having a gate electrode coupled to one of the gate lines, a drain electrode coupled to one of the drain lines, and a source electrode, a pixel electrode coupled to the source electrode of the thin film transistor, and an opposite electrode for, in a pair with the pixel electrode, applying an electric field to the liquid crystal, to change the transmission of said liquid crystal of the corresponding pixel, wherein the opposite electrodes are divided into two groups, the two groups of the opposite electrodes being respectively connected to separate ones of the two opposite electrode lines.

In this liquid crystal panel, base voltages of different polarities can be applied to two groups of the opposite electrodes through the intermediary of the two opposite electrode lines. When the base voltages of different polarities are applied, among the liquid crystals of the pixel portions of the liquid crystal panel, some liquid crystals have a positive-polarity base voltage applied and others have a negative-polarity base voltage applied. For this reason, when the polarity of the base voltage is not varied, the same effects as in the prior art, in which the polarity of the base voltage is varied, can also be obtained. In other words, also when the polarity of the base voltage is also varied at a lower frequency than in the prior art, flickering can be suppressed sufficiently.

In the liquid crystal panel according to the present invention, capacitors for maintaining the electric field are formed by pairing the opposite electrodes and the pixel electrodes, and among the thin film transistors connected to one of the gate lines, those thin film transistors connected with the pixel electrodes paired with the opposite electrodes connected with the same electrode line are as many as substantially N/2.

In the case of this liquid crystal panel, for example, when N thin film transistors are driven at the same time, the currents flowing out from both the liquid crystals and the capacitors are distributed roughly equally into the two opposite electrode lines, which means that the currents do not flow in a concentrated manner into one

electrode line, and accordingly the deterioration of picture quality caused by the currents from the electrode lines is made less than in the prior art.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an equivalent circuit diagram of the liquid crystal panel according to a first embodiment of the present invention;

Fig. 2 is a block diagram of the liquid crystal display device according to the first embodiment;

Fig. 3 is a block diagram of the data processor in the liquid crystal controller;

Fig. 4 is a block diagram of the alternating signal generating circuit of the liquid crystal controller;

Fig. 5 is a timing chart showing the processing steps of the data processor;

Fig. 6 is a block diagram of the gate driver;

Fig. 7 is a block diagram of the drain driver;

Fig. 8 is a waveform diagram showing the operation of the liquid crystal display device according to the first embodiment;

Fig. 9 is an equivalent circuit diagram of the liquid crystal panel according to a second embodiment of the present invention;

Fig. 10 is a block diagram of the liquid crystal display device according to the second embodiment;

Fig. 11 is a waveform diagram showing the operation of the liquid crystal display device according to the second embodiment;

Fig. 12 is an equivalent circuit diagram of the liquid crystal panel according to a third embodiment of the present invention;

Fig. 13 is a block diagram of the liquid crystal display device according to the third embodiment;

Fig. 14 is a waveform diagram of the conventional liquid crystal panel;

Fig. 15 is an equivalent circuit diagram of the conventional liquid crystal panel;

Fig. 16 is a block diagram of the conventional liquid crystal display device;

Fig. 17 is a block diagram of the data processor of the conventional liquid crystal controller;

Fig. 18 is a block diagram of the alternating signal generating circuit of the conventional liquid crystal controller;

Fig. 19 is a block diagram of the conventional gate driver;

Fig. 20 is a block diagram of the conventional drain driver; and

Fig. 21 is a waveform diagram showing the operation of the conventional liquid crystal display device.

#### EMBODIMENTS OF THE INVENTION

Embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 1 is an equivalent circuit diagram of the liquid crystal panel according to a first embodiment of the present invention. Here, description will be given of an example in which four pixel portions are arranged in horizontal direction and four pixel portions are arranged in vertical direction.

A liquid crystal panel 101 shown in Fig. 1 includes five gate lines 102 drawn in the horizontal direction, four drain lines 103 drawn in the vertical direction, pixel portions 104 connected respectively to a drain line 103 and a gate line 102, and arranged in a four-row four-column matrix, a common electrode (Strg0) connected to the pixel portions 104 on odd rows (1st and 3rd rows), and a common electrode (Strg1) connected to the pixel portions 104 on even rows (2nd and 4th rows). If the pixel portions 104 are arranged in an m-row n-column matrix, it is necessary to draw m + 1 gate lines 102 and n drain lines 103.

A pixel portion 104 includes a thin film transistor (TFT) 105, a pixel electrode 106, liquid crystals 107, 111, an additional capacitor 108, and an opposite electrode 112. Three neighboring pixel portions 104 on each row are respectively provided with R(red), G(green) and B(blue) color filters (not shown). The liquid crystal 111 is a liquid crystal supplement to the liquid crystal 107.

As illustrated, the liquid crystals 107, 111 are placed between the pixel electrode 106 and the opposite electrode 112.

The opposite electrodes 112 on the odd rows are connected with a common electrode (Strg0) 109, while the opposite electrodes 112 on the even rows are connected with a common electrode (Strg1) 110.

The pixel portions 104 on the odd columns (1st and 3rd columns) and on the first row are driven by voltage G(1) on the gate line 102. The pixel portions 104 on the even columns (2nd and 4th columns) and on the first row and the pixel portions 104 on the odd columns and on the second row are driven by voltage G(2). The pixel portions 104 on the even columns and on the second row and the pixel portions 104 on the odd columns and on the third row are driven by voltage G(3). The pixel portions on the even columns and on the lowermost row, that is, the fourth row, are driven by voltage G(5).

The pixel portions 104 on the same columns are driven by the voltage on the same drain line 203.

When the pixel portions 104 are arranged in an m-row n-column matrix, the pixel portions 104 on the even columns and on the (a-1)-th row and the pixel portions 104 on the odd columns and on the a-th row are driven by voltage G(a) (where  $1 < a < m$ ). The pixel portions 104 on the b-th column are driven by voltage D(b).

Fig. 2 is a block diagram of the liquid crystal display device according to a first embodiment of the present invention.

The liquid crystal display device in Fig. 2 includes a liquid crystal panel 101, mentioned above, on which pixel portions 104 are arranged in an m-row n-column

matrix, a liquid crystal controller 902 for outputting display data and various synchronizing signals, a drain driver 907 for applying data voltages according to display data to the drain lines 103, a gate driver 908 for applying a scanning voltage to the gate lines 102, AC voltage generating circuits 910, 911 for applying base voltages to the opposite electrodes 112 through the common electrodes, and dividing resistances 912, 913 for applying gray-scale voltages to the pixel electrodes of the pixel portions 104.

Fig. 3 is a block diagram of a circuit portion for generating display data in the liquid crystal controller 902.

Fig. 4 is a block diagram of a circuit portion for generating alternating signals 904, 905 in the liquid crystal controller 902.

The circuit portion for generating display data includes a data delay circuit 1003 and a selector circuit 1005 as shown in Fig. 3. The data delay circuit 1003 receives display data 1001 included in a bus signal 901 supplied from a system (not shown), and a synchronizing signal 1002 representing the sending timing of display data. The supplied display data 1001 is delayed for a specified period of the synchronizing signal 1002 by the data delay circuit 1003, and is output as display data 1004. The selector circuit 1005, according to the method shown in the timing chart of Fig. 5, generates new display data 1006 from the display data 1001 and the delayed display data 1004, and outputs the display data 1006 to the drain driver 907. The above-mentioned circuit re-arranges display data received in the order of display data on the first row (R1-0, G1-0, B1-0), (R1-1, G1-1, B1-1), ... and display data on the second row (R2-1, G2-1, B2-1), ... into the order of (R2-0, G1-0, B2-0), (R1-1, G2-1, B1-1), ..., for example. Note that in parallel with this, the drain driver 907 and the gate driver 908 output synchronizing signals to enable display data 1006 to be displayed.

The circuit for generating alternating signals includes FF (flip-flop) circuits 1103, 1105, 1111, 1112, an exclusive-OR circuit 1107, and an inverter circuit 1109 as shown in Fig. 4. A vertical synchronizing signal 1101 included in the bus signal 901 is subjected to frequency division by 2 in the FF circuit 1103 to become a signal 1104, and is supplied to the FF circuit 1111. The FF circuit 1111 receives the supplied signal 1104 in accordance with a signal 1110 obtained by inverting a horizontal synchronizing signal 1102 in the bus signal 901, and outputs as an alternating signal 905 to the AC voltage generating circuits 910, 911. This alternating signal 905 inverts its polarity at every frame period. Meanwhile, the horizontal synchronizing signal 1102 in the bus signal 901 undergoes a frequency division by 2 in the FF circuit 1105, and is then XORed with the signal 1104 in the logic circuit 1107. The result of this logic operation is received by the FF circuit 1112 in step with the signal 1110, and output as an alternating signal 904 to the drain driver 907. This alternating signal 904 inverts its polarity at every line period.

Fig. 6 is a block diagram of the gate driver 908.

In Fig. 6, the gate driver 908 includes a m+1-step shift register 1303, a level shifter 1305, and a voltage selector circuit 1307. A synchronizing signal 906 supplied to the gate driver 908 from the liquid crystal controller 902 includes a synchronizing signal 1301 to make the selection of the first line effective, and a synchronizing signal 1302 to specify that the line to select be changed. The shift register 1303, on receiving a synchronizing signal 1301, causes the first one of output signals 1304 to go to the HIGH level, and sequentially shifts the output signals 1304, which are pulled to the HIGH level, according to the synchronizing signal 1302. The level shifter 1305 and the voltage selector circuit 1307 apply a selective voltage, which turns on TFT105, to a gate line 102 corresponding to a HIGH-level output signal 1304, but apply a non-selective voltage, which turns TFTs 205 off, to the other gate lines 102. By this arrangement, on the gate lines 102, voltages G(1), G(2), ..., G(m+1) are sequentially raised to a selective voltage, and this operation is repeated.

Fig. 7 is a block diagram of the drain driver 907.

In Fig. 7, the drain driver 907 includes a shift register 1405 for generating timing for accepting display data, line latch circuits 1407, 1409 for generating a timing signal for accepting and storing display data for one line, a positive-polarity gray-scale voltage generating circuit 1411 for generating positive-polarity gray-scale voltages according to the display data, a negative-polarity gray-scale voltage generating circuit 1413 for generating negative-polarity gray-scale voltages according to the display data, and a voltage selector 1415 for selecting and outputting either positive-polarity gray-scale voltages or negative-polarity gray-scale voltages.

The shift register 1405 generates a timing signal 1406 with which to make the latch circuit 1407 receive the amount for one horizontal line of display data 1401, which has been included in the bus signal 901, on the basis of synchronizing signals 1402, 1403, which are components of the bus signal supplied from the liquid crystal controller 902, and outputs the timing signal to the latch circuit 1407. The display data for one horizontal line received and stored in the latch circuit 1407 is then transferred all at once into the latch circuit 1409 in accordance with the synchronizing signal 1404 of the bus signal 901, and then supplied through data buses 1410 to the positive-polarity and negative-polarity gray-scale voltage generating circuits 1411, 1413. The gray-scale voltage generating circuits 1411, 1413 respectively generate drain voltages Vd+ 1412 of positive polarity and drain voltages Vd- 1414 of negative polarity according to supplied display data for one horizontal line, and output the drain voltages to the voltage selector circuit 1415. The voltage selector circuit 1415 selects either the drain voltages Vd+ 1412 or the drain voltages Vd- 1414 according to an alternating signal 904 supplied from the liquid crystal controller 902, and apply those voltages to the drain lines 103. Note that the

drain voltages  $V_d$  differ in polarity between the drain lines 103 on the odd columns and the drain lines 103 on the even columns. The drain voltages applied to the drain lines 103 alternate their polarity at every line period.

The operation of the liquid crystal display device according to this embodiment will be described with reference to Fig. 8.

The liquid crystal controller 902 outputs display data (R2-0, G1-0, B2-0), (R1-1, G2-1, B1-1) ..., obtained by re-arrangement as shown in Fig. 5, to the drain driver 907. When the gate driver 908 raises the voltage  $G(2)$  of the gate line 102 to a selective voltage  $V_{gon}$ , TFTs 105 turn on in the pixel portions 104 on the even columns and on the first row and on the odd columns and on the second row. In parallel with this, the gray-scale voltages according to: display data (R2-0, G1-0, B2-0, R1-1, G2-1, B2-1 ...) for the pixel portions on the even columns and on the first row and also on the odd columns and on the second row; and alternating signal 904 are output by the drain driver 907 to the drain lines 103. The gray-scale voltages are applied to the pixel electrodes 106 of the pixel portions 104 which are in the on state. The alternating signal is applied to the opposite electrodes through the common electrodes (Strg0, Strg1) 109, 110. By the potential differences of the voltages applied to the liquid crystals 107 and the additional capacities 108, the transmittance of the liquid crystals 107 is controlled for gray-level display. The potential differences at the liquid crystals 107 and the additional capacities 108 are still maintained after the voltage  $G(2)$  of the gate line 102 drops to the non-selective voltage  $V_{goff}$ .

After the passage of one line period, when the voltage  $G(2)$  falls to the non-selective voltage  $V_{goff}$  and the voltage  $G(3)$  rises to the selective voltage  $V_{gon}$ , TFTs 105 turn on in the pixel portions 104 on the even columns and on the second row and on the odd columns and on the third row. In parallel with this, the gray-scale voltages according to: display data for the pixel portions on the even columns and on the second row and on the odd columns and on the third row; and the alternating signal 904, are output on the drain lines 103. This operation is repeated in every line period until all the pixel portions 104 are driven in one frame period.

For example, in a period in which the voltage  $G(2)$  rises to the selective voltage  $V_{gon}$ , as shown in Fig. 8, at the pixel portions 104 on the even columns and on the first row, the base voltage  $V_{strg0}$  of the common electrode (Strg0) becomes  $V_{strgN}$  of negative polarity, resulting in a potential difference of positive polarity. At this time, at the pixel portions 104 on the odd columns and on the second row, the base voltage  $V_{strg1}$  on the common electrode (Strg1) 110 becomes the voltage  $V_{strgP}$  of positive polarity, thus giving rise to a potential difference of negative polarity. That is to say, the potential differences at the pixel portions 104 have their polarities inverted alternately from one row to another.

As has been described, in the liquid crystal display

device according to this embodiment, the currents produced by changes of the base voltage at  $n$  pixel portions 104 are divided in half and flow into the common electrodes (Strg0, Strg1) 109, 110. Because the currents do not flow in a concentrated manner into one common electrode, the deterioration of picture quality due to changes in the voltage applied to the common electrodes is made less than that in the prior art.

In the liquid crystal device according to this embodiment, even if it is arranged that the polarity of the base voltage applied to the common electrodes (Strg0, Strg1) 109, 110 is fixed for one frame period, a voltage of positive polarity and a voltage of negative polarity are applied evenly to the pixel portions of the liquid crystal panel, which contributes to the prevention of flickering. Consequently, it is possible to reduce the frequency of the base voltage applied to the common electrodes (Strg0, Strg1) 109, 110, by which power consumption can be decreased.

A second embodiment of the present invention will be described with reference to Figs. 9 to 11.

Fig. 9 is an equivalent circuit diagram of the liquid crystal panel according to a second embodiment of the present invention.

The liquid crystal panel 1601 shown in Fig. 9 includes four gate lines 1602, four drain lines 1603, pixel portions 1604 arranged in a four-row four-column matrix, a common electrode (Strg0) 1609, and a common electrode (Strg1) 1610. Each pixel portion 1604, as in the liquid crystal panel in Fig. 1, includes a TFT 1605, liquid crystals 1607, 1611, an additional capacitor 1608, a pixel electrode 1606, and an opposite electrode 1612.

In this liquid crystal panel 1601, the pixel portions 1604 are connected with gate lines 1602 of the rows along which they are arranged and also connected with drain lines 1603 of the columns along which they are arranged. Specifically, a pixel portion 1604 on the  $a$ -th row and on the  $b$ -th column is driven by voltages  $G(a)$  and  $D(b)$ .

In the pixel portions 1604 on odd rows, the opposite electrodes 1612 on odd columns are connected to the common electrode (Strg1) 1610, while the opposite electrodes 1612 on even columns are connected to the common electrode (Strg0) 1609. In the pixel portions 1604 on even rows, in contrast to the above case, the opposite electrodes 1612 on odd columns are connected to the common electrode (Strg0) 1609, while the opposite electrodes 1612 on even columns are connected to the common electrode (Strg1) 1610. In other words, a plurality of wires interconnecting the opposite electrodes 1612 are laid diagonally in the area where the pixel portions 1604 are arranged. That is, the pixel portions 1604 lying in diagonal directions are connected by the corresponding diagonal common electrode lines.

Fig. 10 is a block diagram of the liquid crystal display device according to this second embodiment.

The liquid crystal display device in Fig. 10 includes a liquid crystal panel 1601 mentioned above, which has

pixel portions arranged in a m-row n-column matrix, a liquid crystal controller 1701, a drain driver 907, a gate driver 908, AC voltage generating circuits 910, 911, and dividing resistances 912, 913. In the liquid crystal panel 1601, because the pixel portions 1604 are driven in row units, the liquid crystal controller 1701 transfers display data to the drain driver 907 using the conventional circuit shown in Fig. 17. Also, the conventional circuit in Fig. 19 may be used for the gate driver 908. The operation for varying the polarity of the base voltages on the common electrodes in this second embodiment is the same as in the liquid crystal display device in Fig. 2, and therefore, the alternating voltage generating circuits 910, 911, and the dividing resistances 912, 913 are used. Also, a circuit the same as the one shown in Fig. 7 is used for the drain driver 907. To generate alternating signals in the liquid crystal controller 1701, a circuit the same as the one in Fig. 4 is used.

The operation of the liquid crystal display device according to this second embodiment will be described with reference to Fig. 11.

In parallel with the gate driver 908 raising the voltage G(2) of the gate line 1602 to the selective voltage Vgon, the drain driver 907 outputs to the drain lines 1603 the drain voltages Vd+ and Vd- selected according to display data (R2-0, G2-0, B2-0, R2-1, G2-1, B2-1 ...) for the second row and the alternating signals 904. Therefore, the drain voltage Vd+ or Vd- as well as the base voltage are applied to the pixel portions 1604 on the second row. The transmittance of the liquid crystals 1607 is controlled and gray-level display is performed by the potential differences of the voltages applied to the liquid crystals 1607 and the additional capacitors 1608. These potential differences are maintained at the liquid crystals 1607 and the additional capacitors 1608 after the voltage G(2) on the gate lines 1602 fall to the non-selective voltage Vgoff.

After the passage of one line period, when the voltage G(2) decreases to the non-selective voltage Vgoff and the voltage G(3) rises to the selective voltage Vgon, TFTs 1605 of the pixel portions 104 on the third row turn on, and in parallel with this, the gray-scale voltages according to display data for the third row and the alternating signal 904 are output on the drain lines 1603. This operation is repeated in every line period until all the pixel portions 104 are driven in one frame period.

For example, in the period when the voltage G(2) rises to the selective voltage Vgon, at the pixel portions 1604 on odd columns and on the second row, the base voltage Vstrg0 on the common electrode (Strg0) 1609 becomes VstrgN of negative polarity as indicated in Fig. 11, thus producing a potential difference of positive polarity. At this time, in the pixel portions 1604 on even columns and on the second row, the base voltage Vstrg1 of the common electrode (Strg1) 110 becomes VstrgP of positive polarity, thus producing a potential difference of negative polarity. In other words, the potential differences at the pixel portions 104 on each row have

their polarities inverted alternately from one row to another. As for the current flowing into the common electrodes (Strg0, Strg1) 1609, 1610, a current from each pixel portion flows through its individual wire in the area with the pixel portions 1604, but on the other hand, a current produced at n/2 pixel portions flows in the wiring area other than the area with the pixel portions 1604. Meanwhile, in the wiring area other than the area with the pixel portions 1406, the resistance can be reduced by using thick wires, but in the area with the pixel portions 1604, it is difficult to reduce the resistance. For this reason, a very small current flow in each wire in the area with the pixel portions 1604, specifically, no more than a current for one pixel portion, greatly contributes to reduction of the distortion of the voltage applied to the liquid crystals.

As has been described, in the liquid crystal display device according to the second embodiment too, the currents caused by voltage changes in n pixel portions 1604 simultaneously driven on each row do not flow in a concentrated manner into one of the common electrodes (Strg0, Strg1) 1609, 1610, and therefore the deterioration of picture quality due to changes in voltage on the common electrodes can be made smaller than in the prior art. If the base voltage applied to each of the common electrodes (Strg0, Strg1) 109, 110 has its polarity fixed for one frame period, because a positive-polarity voltage and a negative-polarity voltage are applied in equal proportion to the liquid crystals of the pixel portions on the liquid crystal panel, flickering can be prevented when the frequency of the base voltage is reduced, thus making power consumption smaller than in the prior art.

A third embodiment of the present invention will be described with reference to Figs. 12 to 14.

Fig. 12 is an equivalent circuit diagram of the liquid crystal panel according to a third embodiment of the present invention. The liquid crystal panel 1901 in Fig. 12 differs from the liquid crystal panel 1601 only in the connection between the pixel portions and the common electrodes. More specifically, in the liquid crystal panel 1901 in the third embodiment, a plurality of wires are drawn vertically to connect to every other one of the vertically arranged opposite electrodes in the area with the pixel portions 1604. The pixel portions 1904 on odd rows and on odd columns and also the pixel portions 1904 on even rows and on even columns are connected to the common electrode (Strg0) 1909, while all the other pixel portions 1904 are connected to the common electrode (Strg1) 1910.

Fig. 13 is a block diagram of the liquid crystal display device according to the third embodiment of the present invention. The liquid crystal display device in Fig. 13 is identical in structure with the liquid crystal display device in Fig. 10 except that the above-mentioned liquid crystal panel 1901 is used.

The operation of the liquid crystal display device according to the third embodiment will now be

described with reference to Fig. 14.

In the liquid crystal display device according to the third embodiment, as in the second embodiment, in parallel with the voltage G(2) of the gate line 1902 rising to the selective voltage of Vgon, the drain voltages Vd+, Vd- selected according to display data for the pixel portions on the second row and the alternating signal 904 are output on the drain lines 1903. Therefore, the drain voltage Vd+ or Vd- and the base voltage are applied to the pixel portions 1904 on the second row. After the passage of one line period, the voltage G(2) falls to the non-selective voltage Vgoff and the voltage G(3) rises to the selective voltage Vgon, TFTs 1905 turn on in the pixel portions 1904 on the third row, and in parallel with this, the gray-scale voltages according to display data for the pixel portions on the third row and the alternating signal 904 are output on the drain lines 1903. This operation is repeated in every line period until all the pixel portions 104 are driven in one frame period.

For example, in the period when the voltage G(2) rises to the selective voltage Vgon, as shown in Fig. 14, potential differences of positive polarity are produced at the pixel portions 1904 on the second row and on odd columns, but potential differences of negative polarity are produced in the pixel portions 1904 on the second row and on even columns as shown in Fig. 14. In other words, the potential differences in the pixel portions 1904 have their polarities inverted alternately from one column to another. As for the current flowing into the common electrodes (Strg0, Strg1) 1909, 1010, a current from every one pixel portion flows through its individual wire in the area with the pixel portions 1904, while on the other hand currents produced at n/2 pixel portions flow in the wiring area other than the area with the pixel portions 1904. Therefore, in the third embodiment, as in the second embodiment, the voltages applied to the liquid crystals can be stabilized.

As a result of the foregoing arrangement, in the liquid crystal display device according to the third embodiment too, the deterioration of picture quality caused by changes of the voltage on the common electrodes can be made smaller than in the prior art. Moreover, flickering can be prevented even when the frequency of the base voltage is reduced, so that power consumption can be made smaller than in the prior art.

As has been described, according to the present invention, the frequency of the voltage applied to the common electrodes can be reduced without increasing flickering, which makes it possible to reduce power consumption of the liquid crystal display device. Moreover, a concentrated flow of currents into the common electrodes can be prevented, and the deterioration of picture quality can be reduced.

## Claims

1. A liquid crystal panel having two substrates arranged facing each other and a liquid crystal filled

between said two substrates, said liquid crystal panel comprising:

- M x N pixel portions arranged in an M-row N-column matrix on said substrate to correspond to pixels arranged in an M-row N-column matrix;
- a plurality of drain lines;
- a plurality of gate lines; and
- two opposite electrode lines,

wherein each pixel portion comprises: a thin film transistor having a gate electrode coupled to one of said gate lines, a drain electrode coupled to one of said drain lines, and a source electrode; a pixel electrode connected to said source electrode of said thin film transistor; and an opposite electrode for, in a pair with said pixel electrode, applying an electric field to said liquid crystal to change the transmission of said liquid crystal of the corresponding pixel, wherein said opposite electrodes are divided into two groups, said two groups of said opposite electrodes being respectively connected to separate ones of said two opposite electrode lines.

2. A liquid crystal panel according to Claim 1, wherein said opposite electrodes are each paired with said pixel electrodes to form capacitors for maintaining said electric field, and wherein among said thin film transistors connected to each one of said gate lines, the number of said thin film transistors connected to said pixel electrodes paired with said opposite electrodes connected to the same opposite electrode line is substantially N/2.
3. A liquid crystal panel according to Claim 1, wherein each one of said drain lines is connected to said drain electrodes of said thin film transistors on one column, wherein among said two opposite electrode lines, one of said electrode lines is connected to said opposite electrodes corresponding to said thin film transistors on odd rows, and the other electrode line is connected to said opposite electrodes corresponding to said thin film transistors on even rows, and wherein each one of said gate lines is connected to said thin film transistors on any one row and on even columns or on odd columns, or in addition to those thin film transistors, each one of said gate lines is also connected to said thin film transistors on an adjacent row and on odd columns or on even columns.
4. A liquid crystal panel according to Claim 2, wherein each one of said drain lines is connected to said drain electrodes of said thin film transistors on one column, wherein among said two opposite electrode lines, one of said electrode lines is connected

to said opposite electrodes corresponding to said thin film transistors on odd rows, and the other electrode line is connected to said opposite electrodes corresponding to said thin film transistors on even rows, and wherein each one of said gate lines is connected to said thin film transistors on any one row and on even columns or on odd columns, or in addition to those thin film transistors, each one of said gate lines is also connected to said thin film transistors on an adjacent row and on odd columns or on even columns.

5. A liquid crystal panel according to Claim 1, wherein each said drain line is connected to said drain electrodes of said thin film transistors on one column, wherein each said gate line is connected to said thin film transistors on one row, wherein one of said opposite electrode lines is connected as a common line to said opposite electrodes corresponding to said thin film transistors on odd rows and on odd columns or even columns, and said thin film transistors on even rows and on even columns or on odd columns and wherein the other electrode line is connected as a common line to said opposite electrodes corresponding to said thin film transistors on even rows and on even columns or on odd columns and said thin film transistors on odd rows and on even column or on odd columns.
6. A liquid crystal panel according to Claim 2, wherein each said drain line is connected to said drain electrodes of said thin film transistors on one column, wherein each said gate line is connected to said thin film transistors on one row, wherein one of said opposite electrode lines is connected as a common line to said opposite electrodes corresponding to said thin film transistors on odd rows and on odd columns or even columns, and said thin film transistors on even rows and on even columns or on odd columns and wherein the other electrode line is connected as a common line to said opposite electrodes corresponding to said thin film transistors on even rows and on even columns or on odd columns and said thin film transistors on odd rows and on even column or on odd columns.
7. A liquid crystal panel according to Claim 3, wherein said two opposite electrode lines comprise a plurality of wiring patterns drawn in the vertical direction or in the diagonal direction on said substrate, and wherein among said thin film transistors connected to each of said gate line, the number of said thin film transistors corresponding to said opposite electrodes connected to the same wiring pattern is one.
8. A liquid crystal panel according to Claim 4, wherein said two opposite electrode lines comprise a plurality of wiring patterns drawn in the vertical direction

or in the diagonal direction on said substrate, and wherein among said thin film transistors connected to each of said gate line, the number of said thin film transistors corresponding to said opposite electrodes connected to the same wiring pattern is one.

9. A liquid crystal panel according to Claim 5, wherein said two opposite electrode lines comprise a plurality of wiring patterns drawn in the vertical direction or in the diagonal direction on said substrate, and wherein among said thin film transistors connected to each of said gate line, the number of said thin film transistors corresponding to said opposite electrodes connected to the same wiring pattern is one.
10. A liquid crystal panel according to Claim 6, wherein said two opposite electrode lines comprise a plurality of wiring patterns drawn in the vertical direction or in the diagonal direction on said substrate, and wherein among said thin film transistors connected to each of said gate line, the number of said thin film transistors corresponding to said opposite electrodes connected to the same wiring pattern is one.
11. A liquid crystal display device comprising:
  - a liquid crystal panel according to Claim 1;
  - a liquid crystal controller for receiving display data and synchronizing signals, and based on the received display data and synchronizing signals, generating liquid crystal display data and a liquid crystal synchronizing signal to enable pictures according to said display data to be displayed on said liquid crystal panel;
  - scanning voltage generating means for applying a selective voltage or a non-selective voltage to said gate lines according to said liquid crystal synchronizing signal;
  - base voltage generating means for applying base voltages at a specified level and of mutually different polarities respectively to said two opposite electrode lines according to said liquid crystal synchronizing signal, and inverting the polarities of said two base voltages at specified periods; and
  - gray-scale voltage generating means for generating gray-scale voltages according to said liquid crystal display data and said base voltages, and applying said gray-scale voltages to said drain lines.
12. A liquid crystal display device comprising:
  - a liquid crystal panel according to Claim 2;
  - a liquid crystal controller for receiving display data and synchronizing signals, and based on the received display data and synchronizing signals, generating liquid crystal display data

and a liquid crystal synchronizing signal to enable pictures according to said display data to be displayed on said liquid crystal panel;

scanning voltage generating means for applying a selective voltage or a non-selective voltage to said gate lines according to said liquid crystal synchronizing signal;

base voltage generating means for applying a base voltage to said two opposite electrode lines according to said liquid crystal synchronizing signal; and

gray-scale voltage generating means for generating gray-scale voltages according to said liquid crystal display data and said base voltage, and applying said gray-scale voltages to said drain lines.

13. A crystal liquid display device according to Claim 11, wherein said base voltage generating means inverts the polarities of said base voltages at every display period of one frame of said liquid crystal display data, and wherein said gray-scale voltage generating means generates said gray-scale voltages according to the base voltages of different polarities at every display period of one line of said liquid crystal display data.

14. A liquid crystal display device according to Claim 11, wherein said liquid crystal controller generates said liquid crystal display data by re-arranging said received display data according to the connecting condition of said thin film transistors, gate lines and drain lines on said liquid crystal panel.

15. A liquid crystal display device according to Claim 12, wherein said liquid crystal controller generates said liquid crystal display data by re-arranging said received display data according to the connecting condition of said thin film transistors, gate lines and drain lines on said liquid crystal panel.

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FIG.1

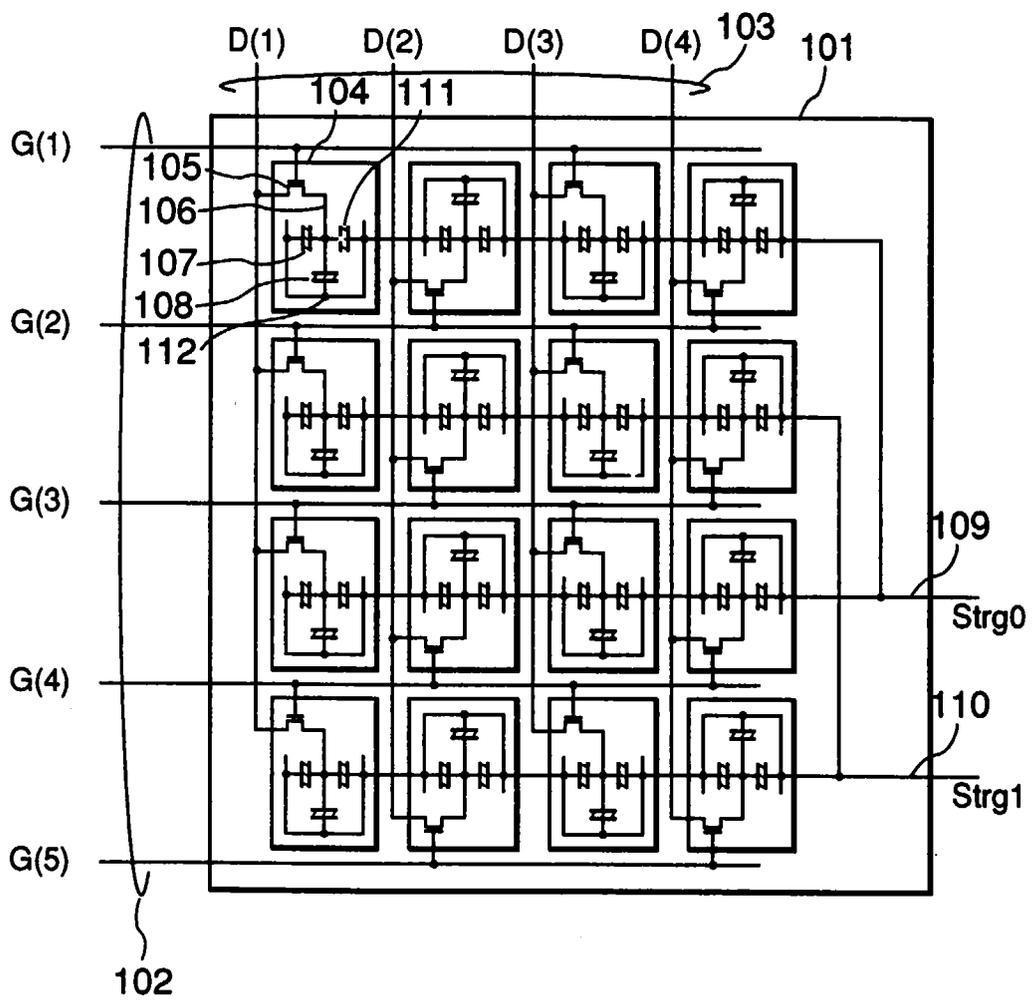


FIG.2

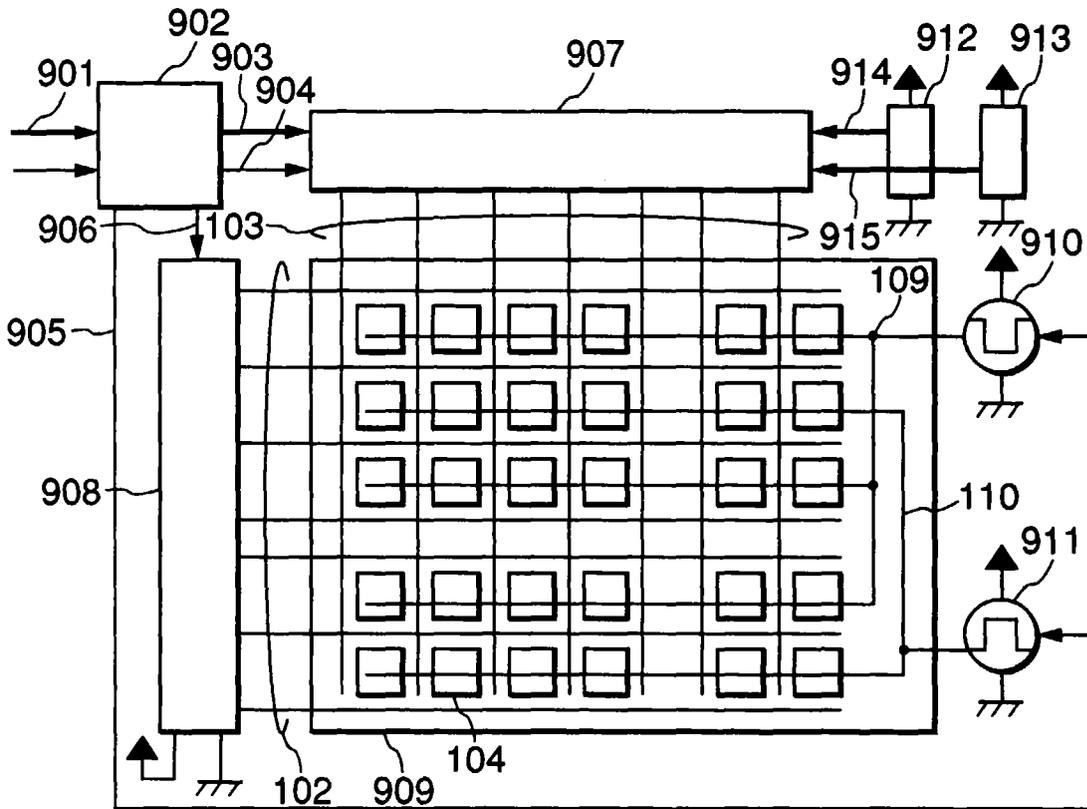


FIG.3

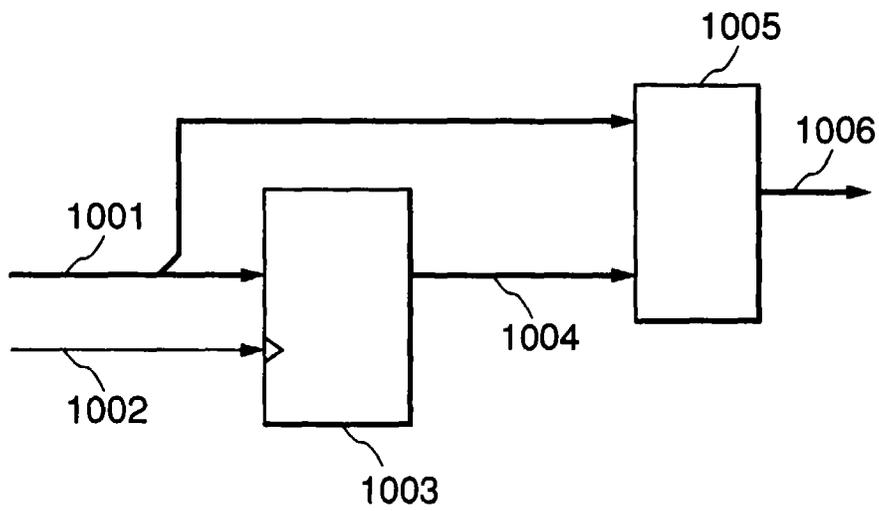


FIG.4

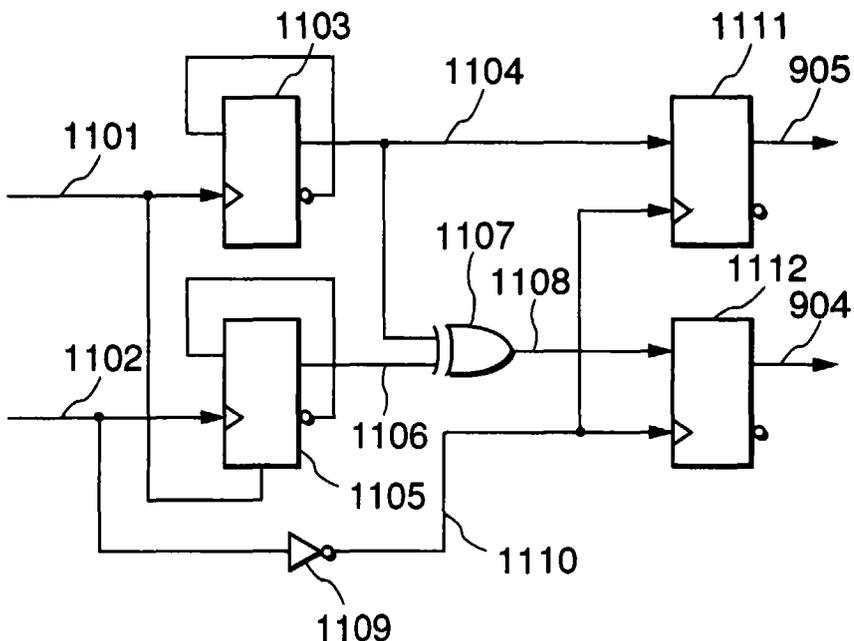


FIG.5

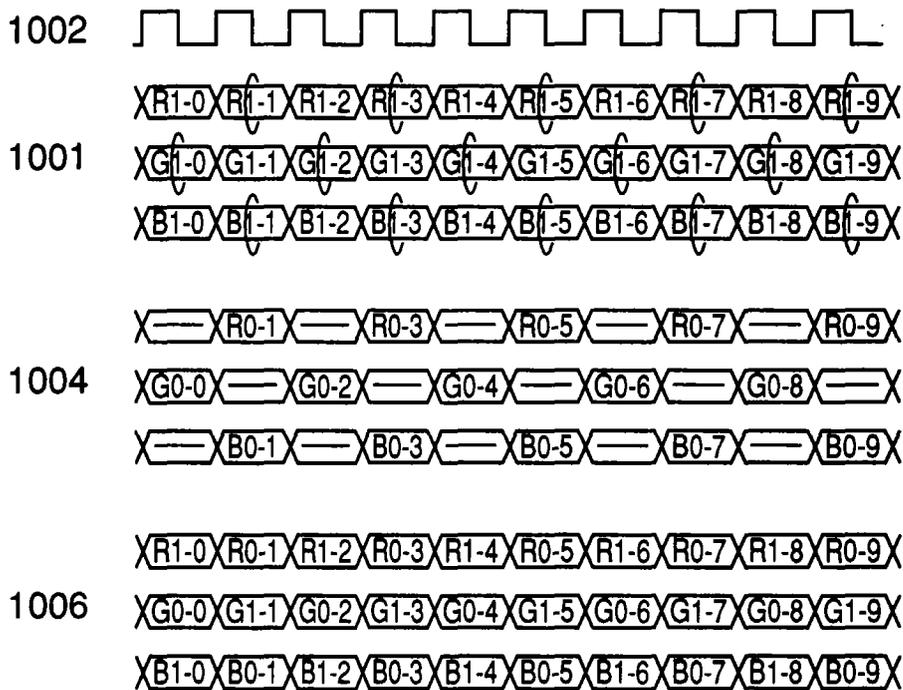


FIG.6

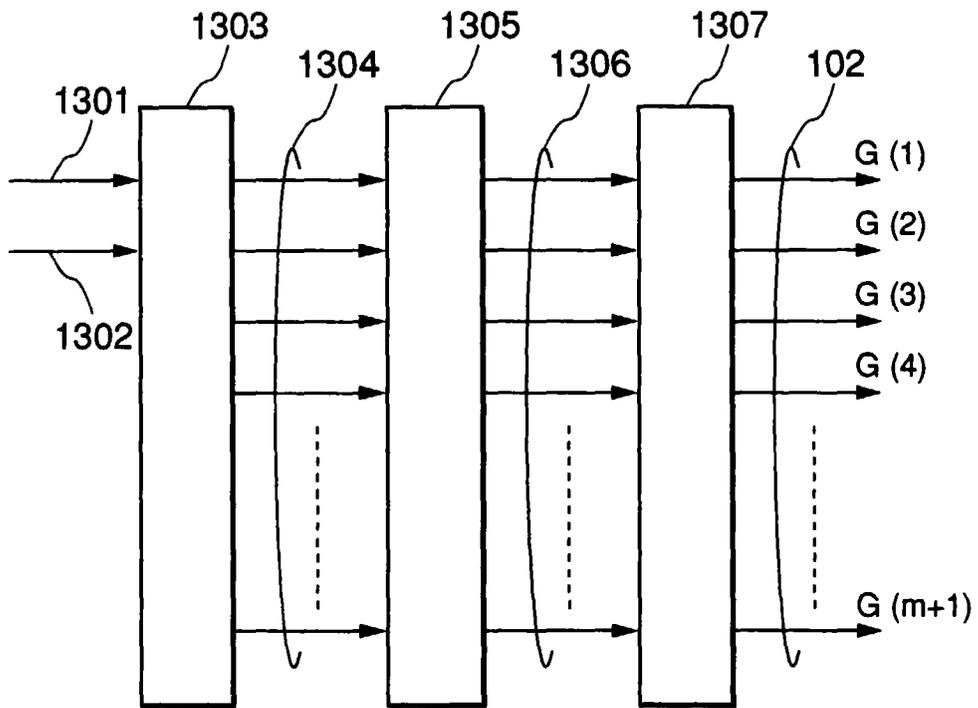


FIG.7

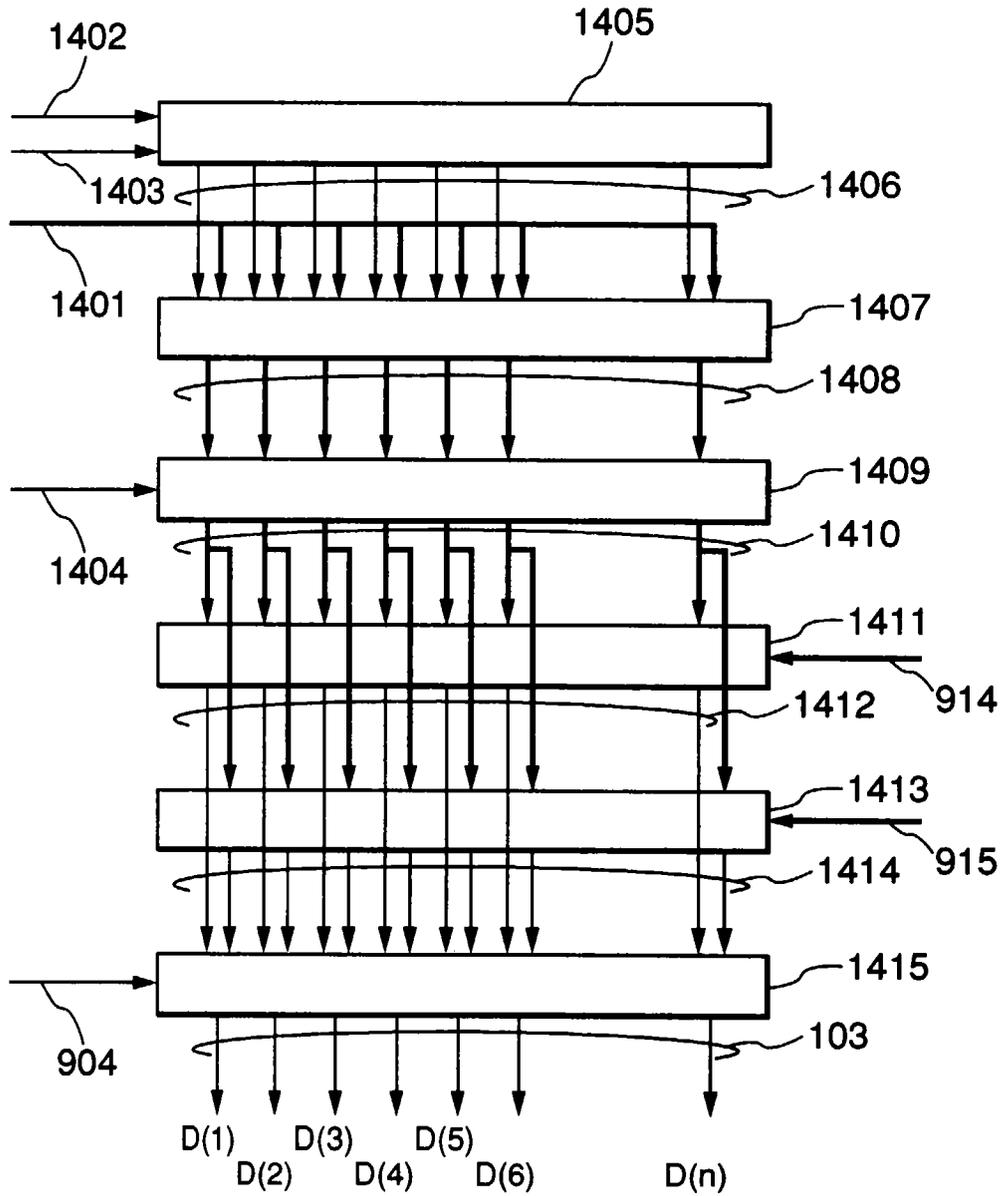


FIG.8

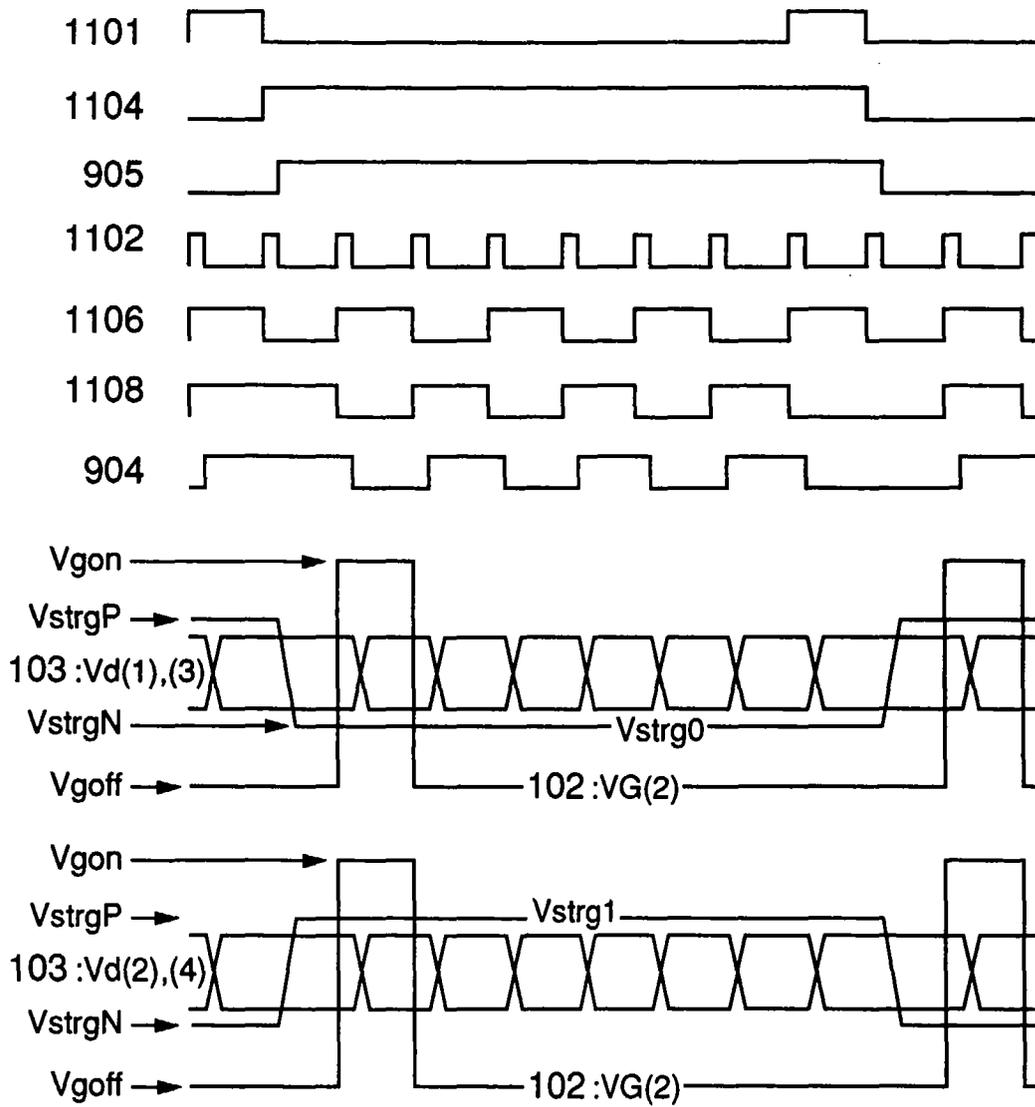




FIG.10

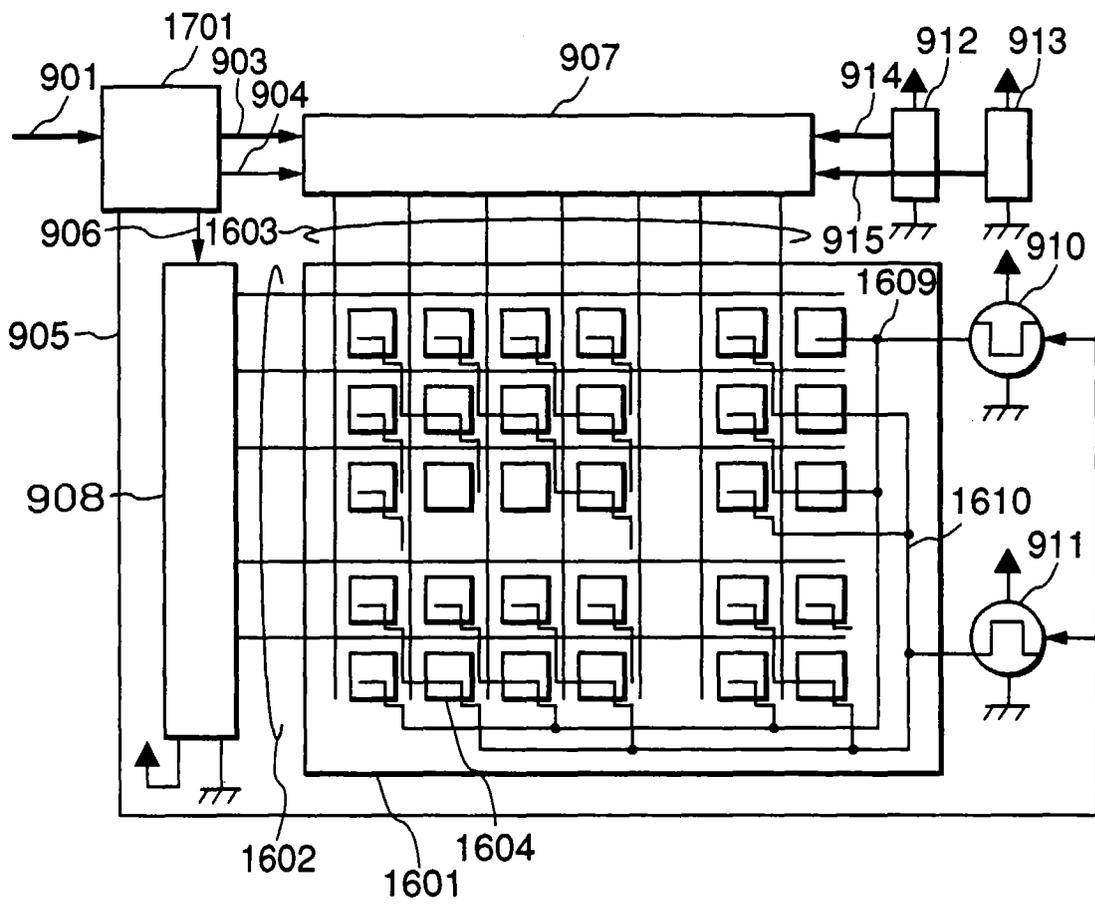


FIG.11

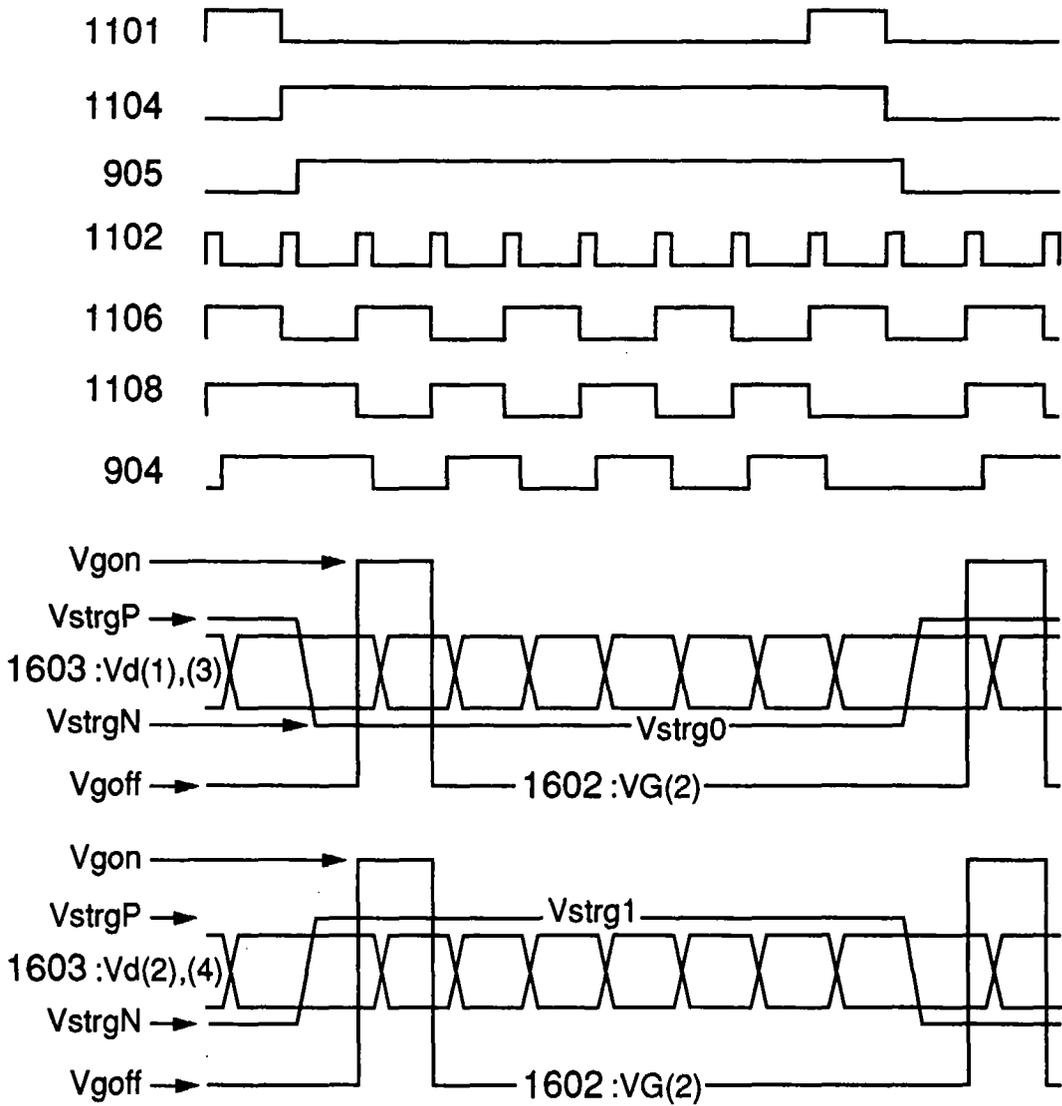


FIG.12

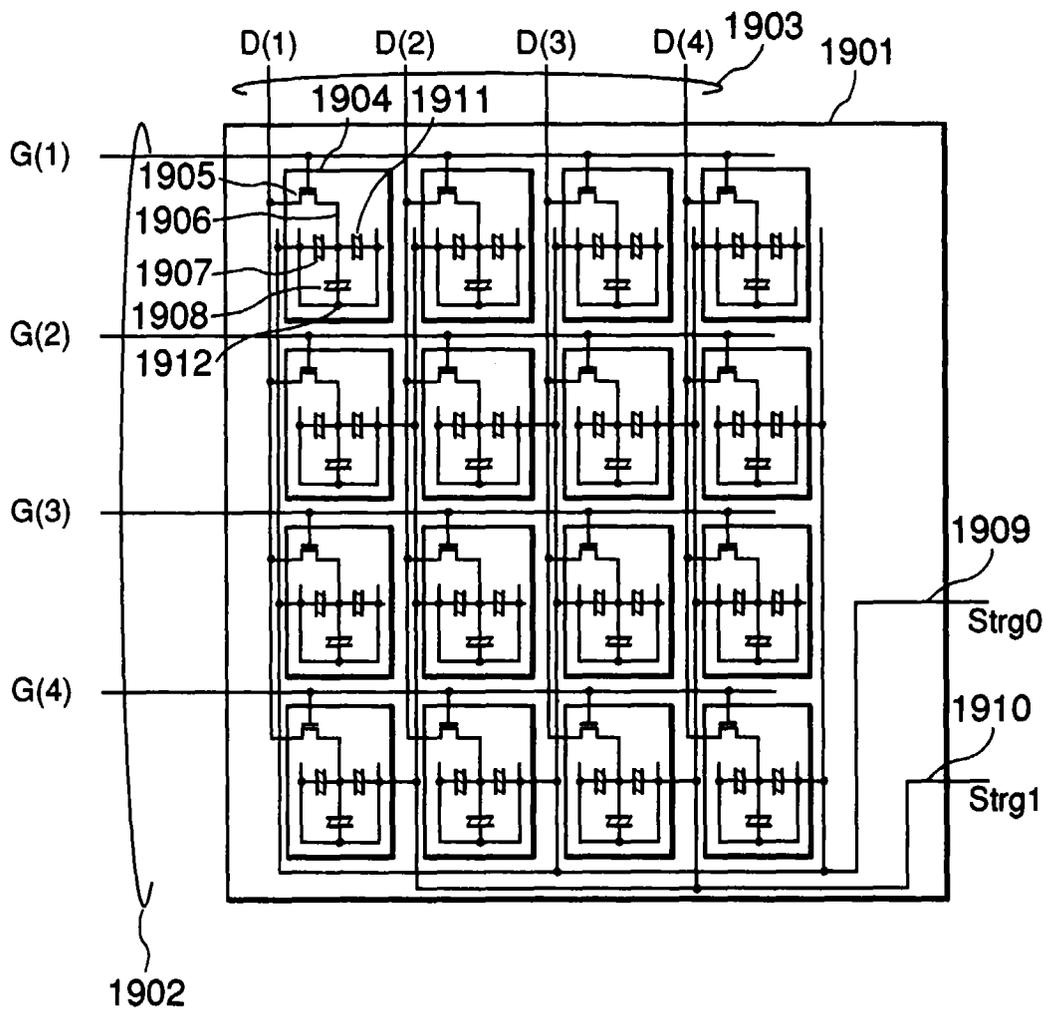


FIG.13

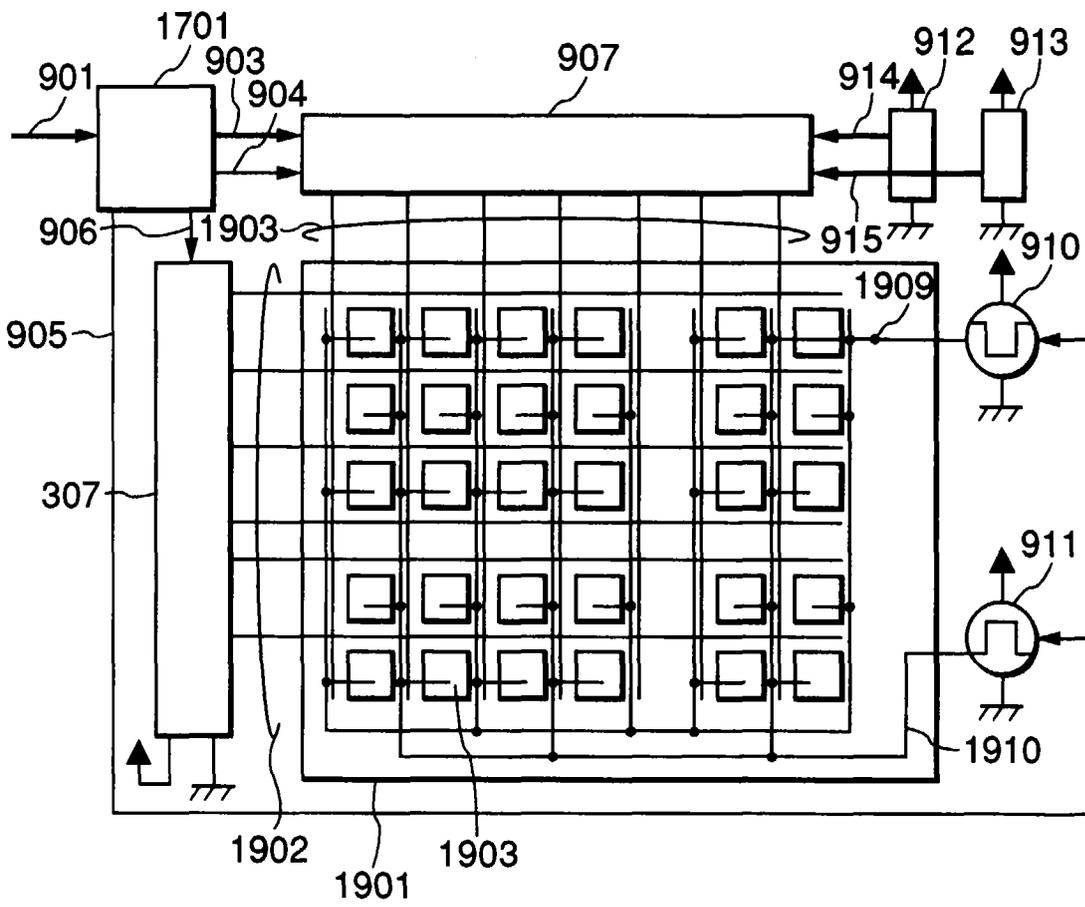


FIG.14

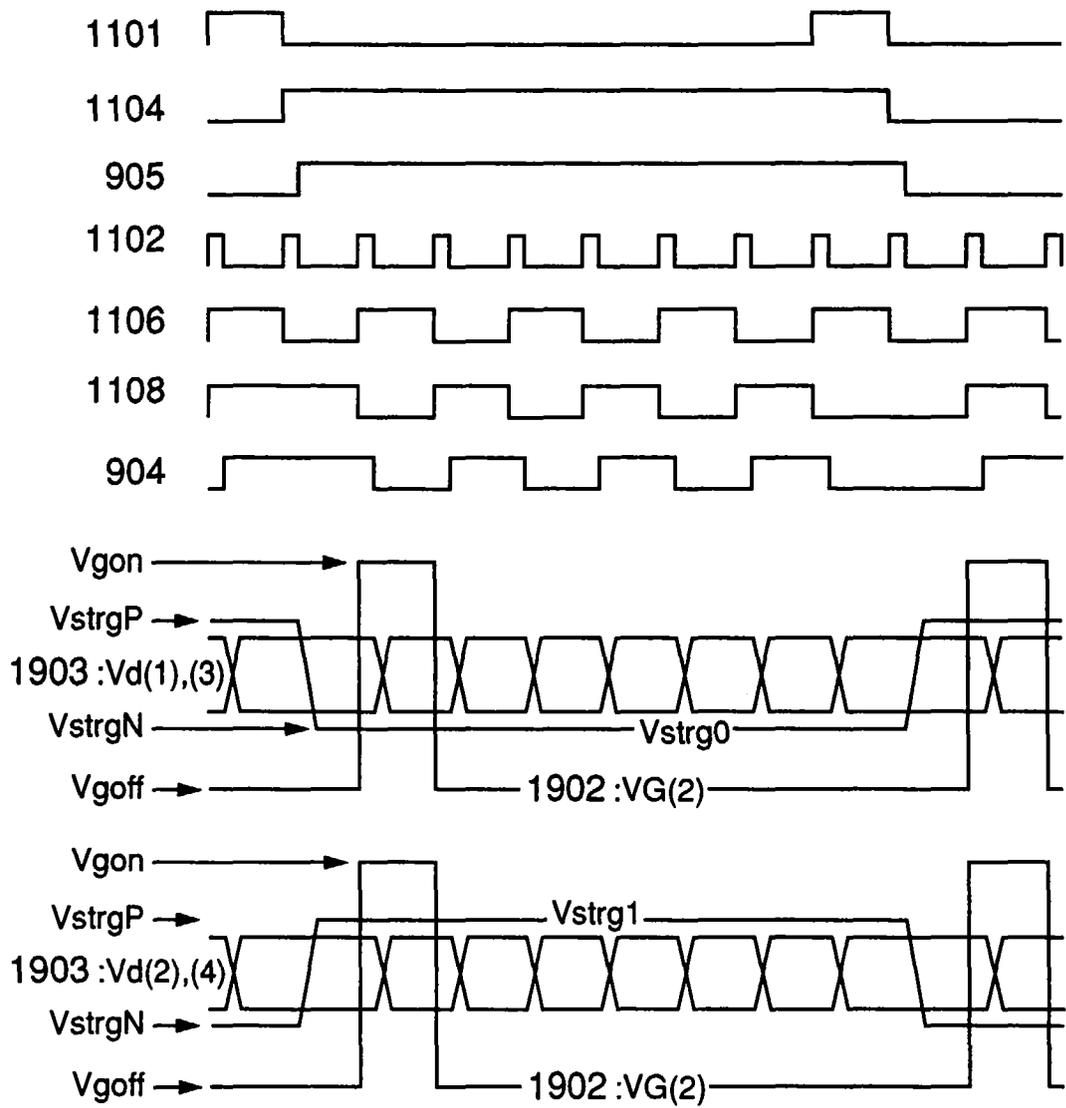


FIG.15

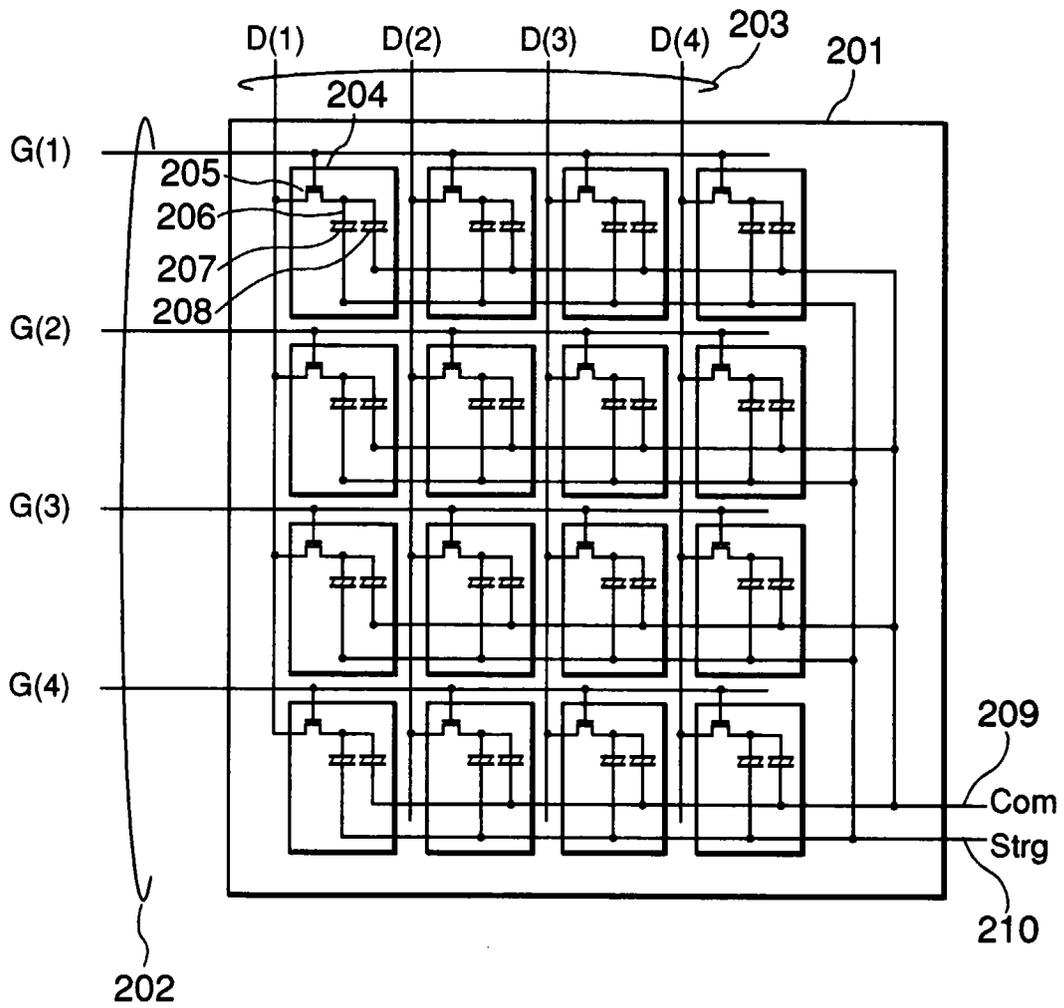


FIG.16

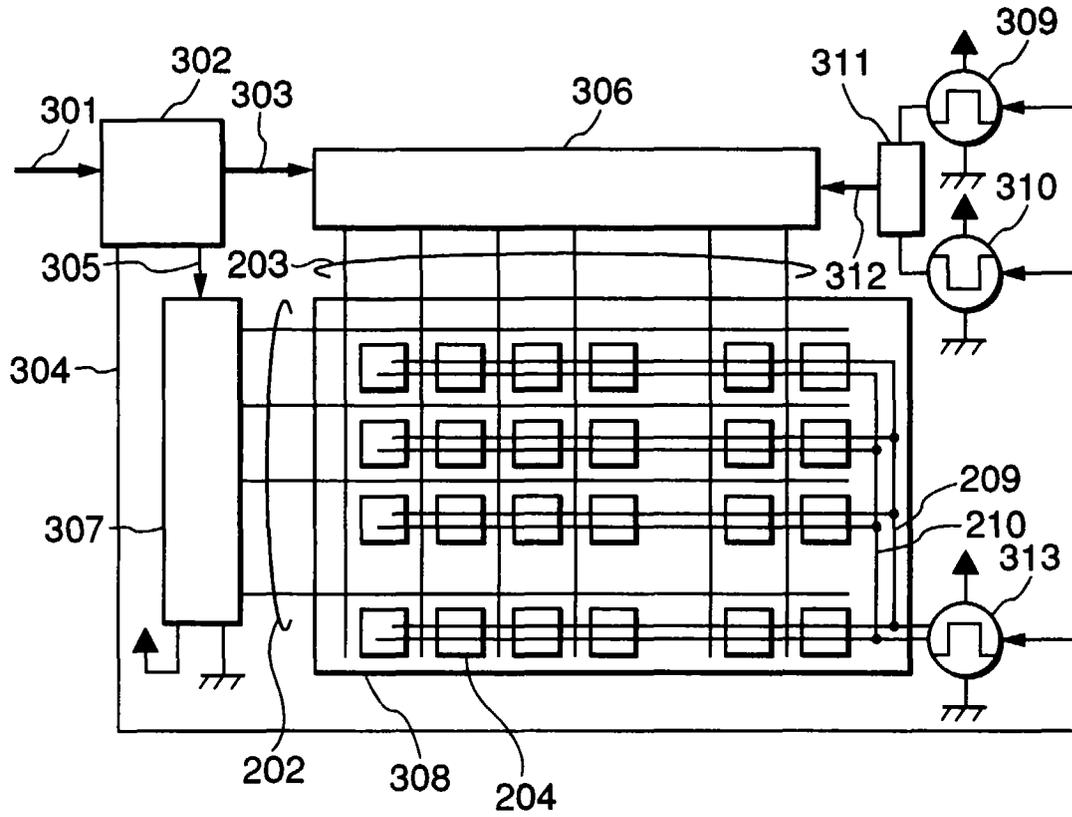


FIG.17

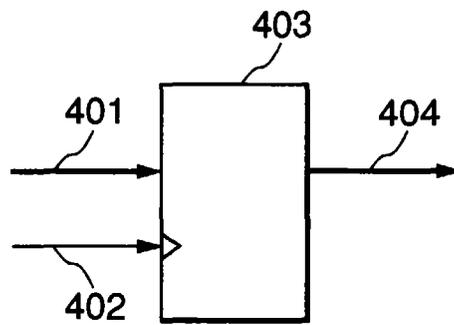


FIG.18

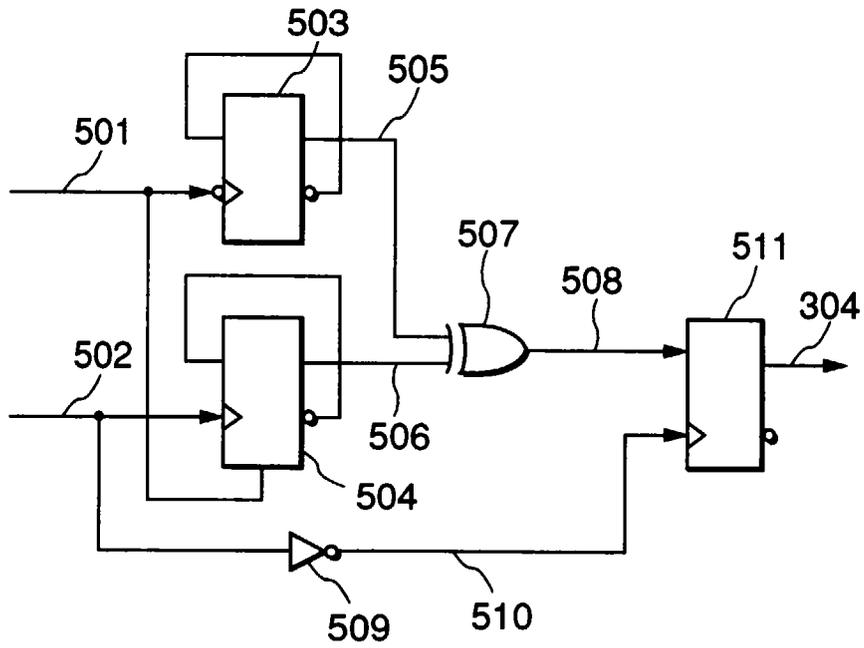


FIG.19

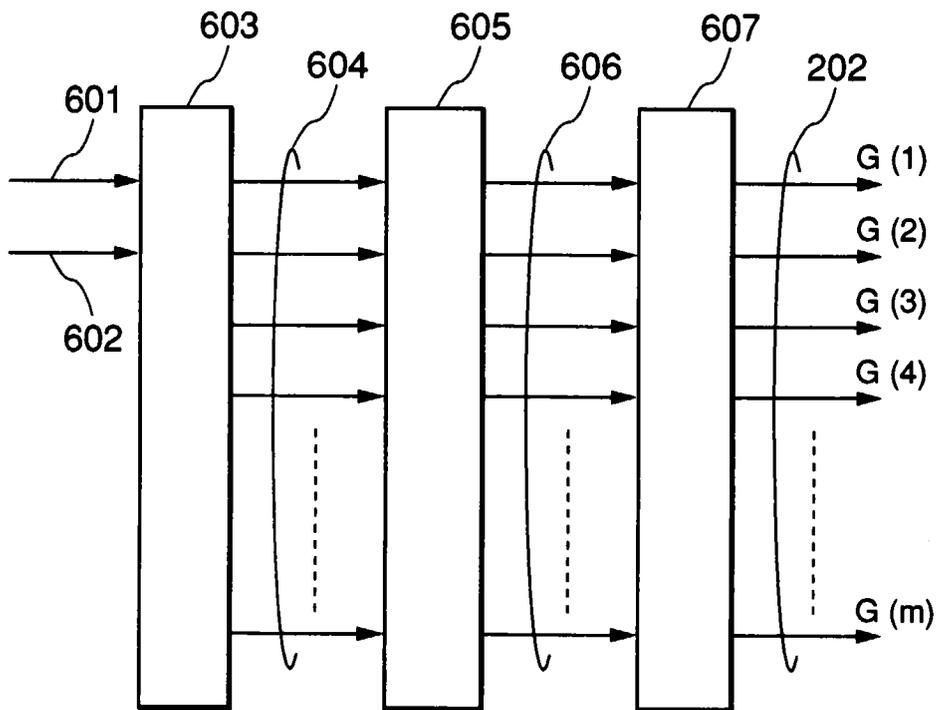


FIG.20

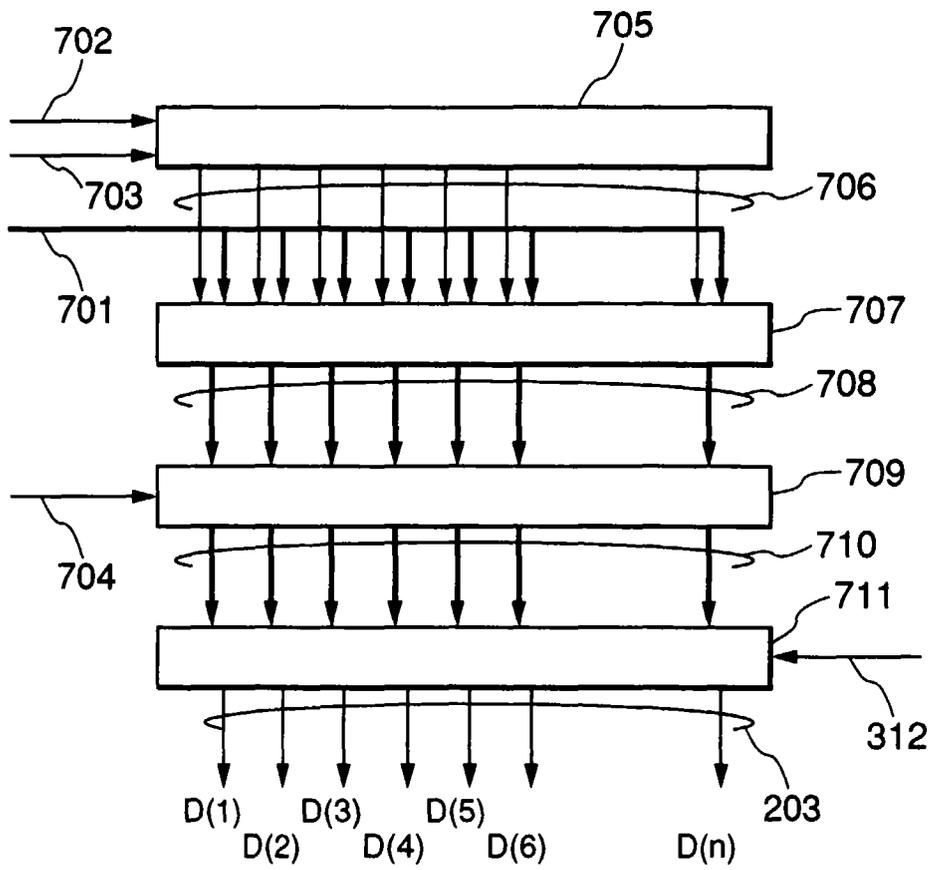
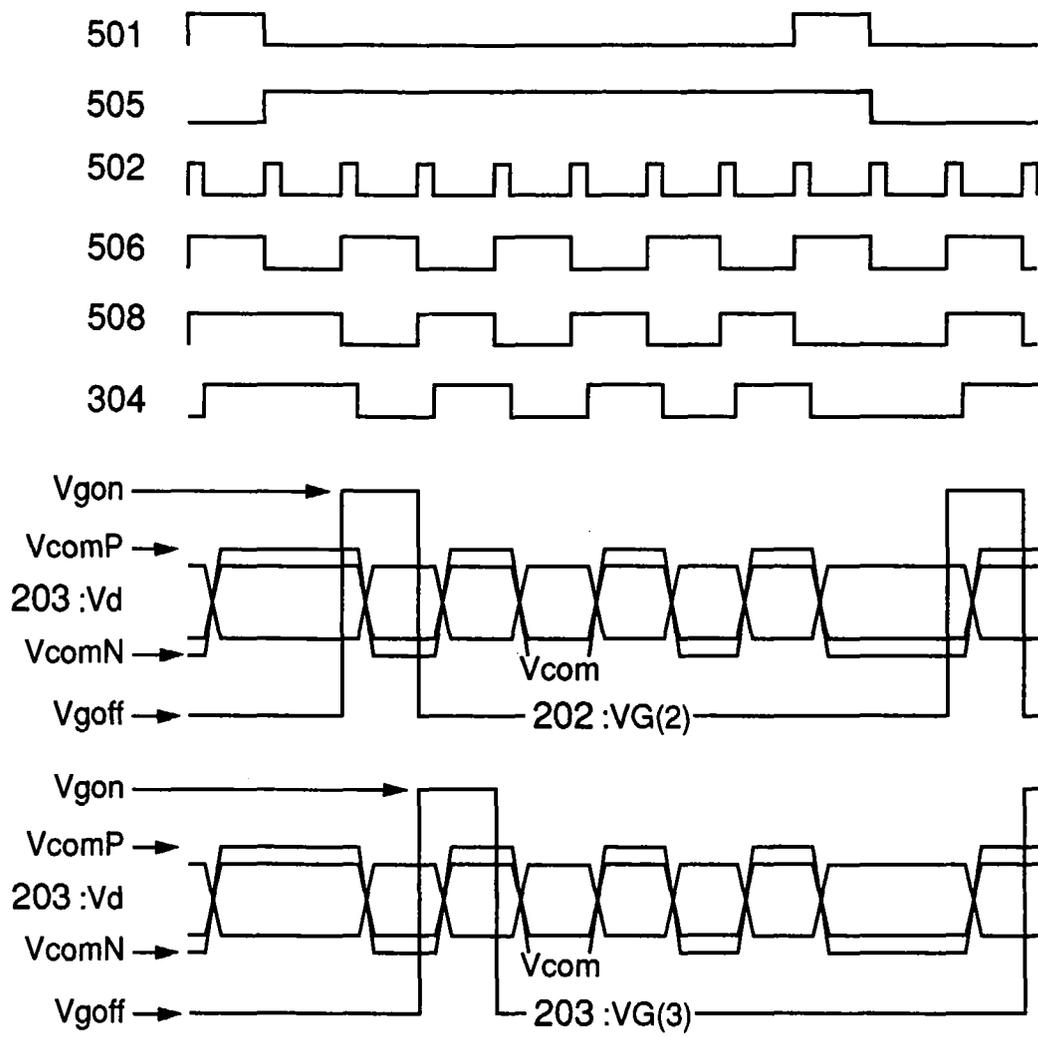


FIG.21





European Patent  
Office

EUROPEAN SEARCH REPORT

Application Number  
EP 97 11 8248

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 692 780 A (SAGEM S.A.)	1	G09G3/36
Y	* Abstract *	2	
	* page 4, line 26 - page 5, line 11; figure 2 *		
A	* claim 1 *	11,12	
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Y	PATENT ABSTRACTS OF JAPAN vol. 96, no. 4, 30 April 1996 & JP 07 318901 A (KYOCERA CO.), 8 December 1995,	2	
A	* abstract *	12,14,15	
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A	EP 0 466 378 A (I.B.M. CO.)	3-6, 11-15	
	* Abstract * * column 3, line 50 - column 5, line 3; figures 1-3,5 *		
	---		
A	US 5 151 689 A (KABUTO ET AL.)	3-6,14, 15	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
	* Abstract * * column 3, line 31 - column 4, line 61; figures 1A,2-4 * * column 6, line 4 - column 7, line 14 *		G09G
	---		
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 81 (E-719), 23 February 1989 & JP 63 260375 A (MITSUBISHI ELECTRIC CO.), 27 October 1988,	7-10	
	* abstract *		
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A	EP 0 554 129 A (SHARP K.K.)	11-15	
	* Abstract * * column 1, line 11 - line 47; figures 1,4 * * column 5, line 23 - line 43 *		
	-----		
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		21 January 1998	Corsi, F
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document	
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