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(71) Applicant: **SHARP KABUSHIKI KAISHA**
Osaka-shi Osaka 545 (JP)

(72) Inventors:
- **Gilmour, Sandra**
  Stow on the Wolt, GL54 1AL (GB)
- **Tillin, Martin David**
  Abingdon, Oxfordshire OX14 2PG (GB)
- **Towler, Michael John**
  Botley, Oxford OX2 9AL (GB)
- **Robinson, Michael Geraint**
  Newington Rd, Stadhampton, OX44 7UU (GB)
- **Tombling, Craig**
  Bear Lane, Stadhampton, OX44 7UR (GB)
- **Mayhew, Nicholas**
  Oxford OX2 0ED (GB)

(74) Representative: **Robinson, John Stuart et al**
Marks & Clerk
Nash Court
Oxford Business Park South
Oxford OX4 2RU (GB)

(54) Active matrix light modulators, use of an active matrix light modulator, and display

(57) An active matrix light modulator, such as a thresholdless antiferroelectric active matrix liquid crystal display, comprises an active matrix of control elements 18 disposed at intersections of data lines 22 and scan lines 20, and an array 10 of pixels which are selectively addressable by data and scan signals applied to the control elements 18 by a data driver 12 and a scan driver 14. Such addressing is controlled so that a voltage is applied to each pixel during a corresponding addressing frame by the application of data and scan signals to an associated one of the control elements 18 in order to select the optical level of the pixel for each frame, and bipolar switching is applied to control the voltage applied to the pixel during successive subframes such that, when one optical level is selected for the frame, a positive voltage is applied to the pixel during one subframe of the frame and a negative voltage of equal magnitude but opposite polarity is applied to the pixel during another subframe of the frame and, when another optical level is selected for the frame, an intermediate voltage (preferably zero voltage) is applied to the pixel during both of the subframes of the frame, so as to provide DC balancing within the frame. The required grey level within each frame is accurately reproduced and is substantially independent of the previous state of the pixel. The use of such modulators to reduce the effects of asymmetrical optical performance and colour-sequential displays are also disclosed.

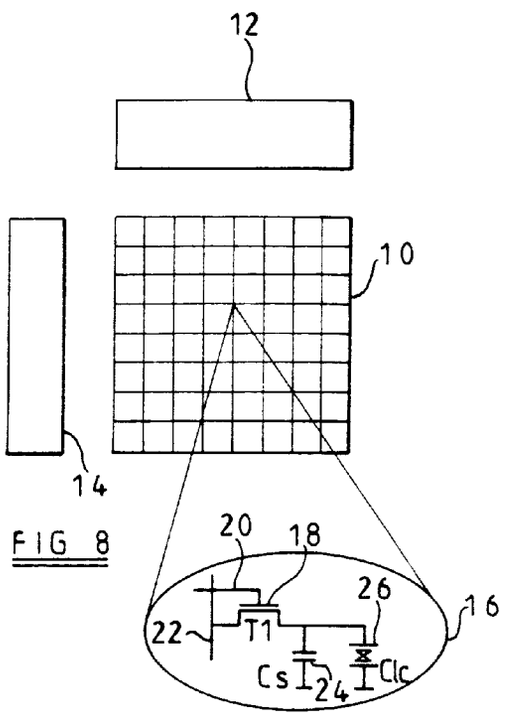

FIG 8

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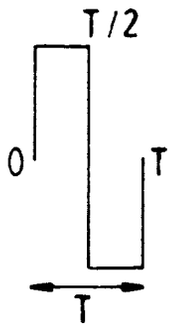
FIG 3a



Description

This invention relates to active matrix light modulators and is concerned more particularly, but not exclusively, with active matrix liquid crystal devices, such as antiferroelectric liquid crystal displays (AFLCD's), in which accurately reproducible grey levels can be obtained. The invention also relates to use of an active matrix light modulator and to a display.

It should be understood that the term "light modulators" is used in this specification to encompass both light transmissive modulators, such as diffractive spatial modulators, and light emissive modulators, such as conventional liquid crystal displays.

AFLCD's and related liquid crystal devices exhibit field tunable, in-plane switching behaviour which is capable of being exploited to provide greyscale and wide viewing angle in both passively driven and active matrix driven devices. Such liquid crystal devices have the property that, when the liquid crystal director switches to a different state in response to an applied transverse DC voltage, the director remains substantially parallel to the boundary plates for all applied switching voltages. Typically, in a transmissive device, the liquid crystal cell is disposed between crossed polarisers arranged such that the maximum dark state of the device is obtained at an applied voltage of zero volts. Such an arrangement typically corresponds to the case in which the alignment directions of the boundary surfaces are substantially parallel to one another and to the transmission axis of one of the two polarisers. On application of a DC voltage of either polarity to the cell, the optic axis of the liquid crystal material is rotated so that it is no longer parallel to the transmission axis of either polariser, and the light transmission of the device is increased.

Alternatively the liquid crystal cell may be arranged between two polarisers arranged with their axes parallel to one another such that the bright state is obtained when a voltage of zero volts is applied. On applying a DC voltage of either polarity to the cell, the device is switched to a darker state. However a switching angle of 45 degrees is required in order to obtain a maximum dark state. Accordingly it is possible for two such cells to be arranged in series between two polarisers having parallel axes such that the device as a whole is in the bright state when a voltage of zero volts is applied to each cell, and such that, when voltages of opposite polarities are applied to the cells, the optic axes of the cells are rotated in opposite directions such that the light transmission of the combined device decreases. When the angle between the two optic axes reaches 45 degrees, the device is in its maximum dark state, so that each cell is required to switch through an angle of only 22.5 degrees to reach the maximum dark state. An equivalent reflective device utilising a single polariser can be formed utilising a single liquid crystal cell and a quarter wave plate disposed between the cell and a reflective surface such that, in the zero voltage state, the optic axis of the cell is parallel to the polariser axis and the axis of the quarter wave plate, and the maximum dark state is reached when the cell is switched to +/- 22.5 degrees.

Such devices may be fabricated from antiferroelectric liquid crystal (AFLC) materials, or alternatively from materials exhibiting the deformed helix ferroelectric (DHF) effect, the short pitch bistable ferroelectric (SBF) effect or the electroclinic (EC) effect.

As disclosed by Y. Yamada, N. Yamamoto, M. Yamawaki, I. Kawamura and Y. Suzuki, Proc. Japan Display 1992, p. 57, in relation to a passive AFLCD driving scheme, it is possible to avoid ghosting due to ionic build up in idealised surface stabilised AFLC's by means of a passive addressing arrangement in which the pixels are switched between equal and opposite ferroelectric states +F or -F by the application of positive and negative voltages during successive addressing frames. A sharp voltage threshold must be overcome to switch the AFLC into either of these states, and voltages with magnitudes typically between 20 and 40 volts are required to fully switch the material into the required state. On removal of the applied voltage, the liquid crystal material relaxes to the more stable antiferroelectric (AF) state by way of the corresponding hysteresis curve, as shown in the graph of Figure 1a which shows ideal (symmetrical) voltage-transmission characteristics of an AFLC on switching to and from each of the ferroelectric states, where the transmission is denoted by τ and the applied voltage is denoted by V. Accordingly a holding voltage must be continuously applied to the AFLC in order to maintain the device in one of the ferroelectric states +F or -F. If a voltage less than that required to give full switching is applied, an intermediate grey level is obtained and, on removal of the voltage, the device relaxes to the AF state by way of the corresponding shallower hysteresis curve shown in broken lines in Figure 1a. As the F to AF relaxation can be quite slow, a reset period is usually required before the next frame is addressed in order to ensure that the transmission level in the next frame is not affected by the transmission level of the previous frame. Figure 1b shows typical (asymmetrical) voltage-transmission characteristics of an AFLC on switching to and from each of the ferroelectric states, from which it will be seen that the light transmission characteristics of the ferroelectric states are generally different in a typical AFLC.

As is well known, a passive addressing scheme for a liquid crystal display commonly uses row and column electrodes which intersect one another at the pixels of the display, and a data driver for supplying display data to the column electrodes in synchronism with scan pulses supplied to the row electrodes by a scan driver in a cyclically repeating sequence so that the rows of pixels are refreshed one at a time until all of the rows have been refreshed to complete refreshing of a frame of display data. The process is then repeated for the next frame of data. Figure 2a shows a suitable scan wave-

form for addressing the passively addressed AFLCD as described above in which the polarity of the applied voltage is reversed from frame to frame. Such a waveform comprises, during each addressing frame, a select (strobe) period 1, a non-select (holding voltage) period 2 and a reset period 3. The polarity of these periods is reversed from frame to frame in order to maintain the net DC balance of the pixels along the rows, and Figure 2a shows the waveforms of scan pulses applied during two successive frames of such a passive addressing scheme. Furthermore DC balanced data pulses are applied to the column electrodes which, when combined with the select (strobe) period 1 of the scan pulses applied to the row electrodes, determine the optical state (F, AF or intermediate) of the pixel during the non-select (holding voltage) period 2. Figure 2b shows typical DC balanced bipolar data pulses which may be applied to the column electrodes in such a passive addressing scheme corresponding respectively to an ON signal and an OFF signal for selection of the F state or the AF state in the select period 1 of the positive polarity pulse of Figure 2a, and an ON signal an OFF signal for selection of the F state or the AF state in the select period 1 of the negative polarity pulse of Figure 2a. Since the data pulses (but not the resultant pulses obtained by combination of the data and strobe pulses) are DC balanced during one line address time in such a passive addressing scheme, this results in application of a high frequency to the display at all times and leads to high power consumption.

M. Yamawaki, Y. Yamada, N. Yamamoto, K. Mori, H. Hayashi, Y. Suzuki, Y.S. Negi, T. Hagiwara, I. Kawamura, H. Orihara and Y. Ishibashi, Japan Display 1989, p. 26-9 discloses a passive addressing scheme for an AFLCD in which two addressing frames of opposite polarity are used for one display picture in order to effect DC balancing. As in the previously described passive addressing scheme, the scan waveform comprises, during each addressing frame, a select (strobe) period and a non-select (holding voltage) period. During the select period, an ON data signal or an OFF data signal selects the F state or the AF state of a pixel as the case may be, this state being maintained by the application of the holding voltage within the following non-select period. In the subsequent frame, the polarity of the periods is reversed in such a manner that the pixel is switched to the opposite F state where an ON signal is applied or is maintained in the AF state where an OFF signal is applied. In this manner, the transmission level is kept the same in the two addressing frames of opposite polarity used to display a single picture whilst providing DC balancing. However, as in the passive addressing scheme already described, a holding voltage must be applied in order to maintain the device in one of the ferroelectric states with consequent implications for power consumption. Furthermore, since conventional AFLC's with suitable switching thresholds require a voltage in the range of between 20 to 40 volts to switch, relatively high voltages are necessary in such a passive addressing scheme. There is no disclosure in this reference of grey-scale.

S. Quentel, C. Rodrigo, J.M. Oton, Journal of the SID, 4/1, 1996, p. 19 discloses an AFLCD passive addressing scheme using scan waveforms as shown in Figure 2a combined with unipolar data pulses. Since the polarity of the scan waveform is reversed from frame to frame, the polarity of the data pulses is also changed from frame to frame. However, since different data is applied in each frame, the device is only statistically DC balanced, and it is still possible for a net DC voltage to be applied to some pixels for long periods such that any ionic build-up in these periods results in certain grey levels being unobtainable. A further disadvantage of this addressing scheme is that the AFLCD must be arranged between crossed polarisers in order to optimise the symmetry of the switching so that positive and negative voltages of the same amplitude result in similar light transmission levels, and it is not possible to ensure that such symmetry is obtained for all voltages as asymmetry is a function of voltage. For example, if the device is set to give equivalent maximum bright states, the maximum dark state will not be obtained at zero volts.

European Patent Publication No. 0552045A1 discloses a thresholdless AFLC device in which grey levels within each frame are selected using a monopolar voltage. The polarity of the monopolar voltage changes from frame to frame. This addressing scheme only provides statistical DC balancing as described above. Also, the asymmetry described above is not averaged and leads to optical modulation at half the frame frequency when the device is viewed off-axis.

European Patent Publication No. 0586155A2 discloses an active matrix addressing circuit for a liquid crystal display in which each pixel includes a thin film transistor (TFT) switching element and a pixel capacitance. The gate terminal of the switching element is connected to the scan electrode such that, when an appropriate scan pulse is applied to the scan electrode, the switching element is turned on in order to transfer a data pulse applied to the data electrode to the pixel capacitance. In this way, an image is displayed based on the applied data and the image is maintained even after the switching element is turned off due to the maintenance of charge by the pixel capacitance under the effect of the applied electric field. However, such an active matrix addressing scheme is not capable of providing accurately reproducible grey levels when used with conventional ferroelectric liquid crystal materials. Furthermore, such an addressing scheme is not suitable for addressing a conventional AFLC material since such materials require 20-40 volts to switch and TFT switching elements can operate at only up to about 20 volts (and preferably operate at substantially less than 20 volts).

British Patent Publication No. 2 312 773 and European Patent Publication No. 0 807 918 disclose a polycrystalline silicon active matrix addressing circuit in

which each pixel includes: a TFT switching element having a data input for receiving data pulses from the data electrode and a scan input connected to the scan electrode; a storage capacitor connected to the output of the switching element; and a buffer amplifier connected between the output of the switching element and the pixel. Such a circuit allows substantially constant voltage addressing of the display so that, during each frame, a continuous voltage of one or other polarity is applied to each pixel, thus reducing the power requirement of the display. However, as with the previous reference, such an active matrix addressing scheme is not suitable for an AFLC material.

Direct view AFLC, SBF and DHF devices when viewed off-axis may produce flicker which is perceivable to some viewers. Even in the case of devices which appear symmetrical when viewed on-axis, there exist some off-axis positions for which the brightness is not symmetrical, i.e. the brightness is not equivalent for equal but oppositely switched states. In such viewing regions, an optical modulation at half the frame frequency may be perceived by some viewers.

It is an object of the invention to provide an active matrix light modulator, such as an AFLCD for example, which allows repeatable grey levels to be obtained and addressing asymmetry, where present, to be substantially eliminated.

The term "asymmetric optical performance" as used herein means a first optical performance (such as light emissivity, transmissivity or reflectivity) which occurs in response to an applied voltage of a predetermined value and a first polarity and which differs from a second optical property of the same type resulting from an applied voltage of the same predetermined value but of opposite polarity.

According to a first aspect of the invention, there is provided use of an active matrix light modulator for reducing the effects of asymmetrical optical performance, the active matrix light modulator comprising: a plurality of data lines; a plurality of scan lines; an active matrix of control elements disposed at intersections of the data lines and the scan lines; an array of pixels which are selectively addressable by data and scan signals applied to the control elements by way of the data and scan lines so as to be set to a first optical transmission state in response to a positive applied voltage of a particular magnitude, a second optical state in response to an intermediate applied voltage and a third optical state in response to a negative applied voltage of equal magnitude, but opposite polarity, to said positive applied voltage; addressing means for addressing each pixel during a corresponding addressing frame by the application of data and scan signals to an associated one of the control elements in order to select the optical level of the pixel for each frame; and voltage inversion means for controlling the voltage applied to each pixel during successive subframes of each frame such that, when one optical level is selected for the frame, said positive voltage is applied to the pixel during one subframe of the frame and said negative voltage is applied to the pixel during another subframe of the frame and, when another optical level is selected for the frame, said intermediate voltage is applied to the pixel during both of the subframes of the frame, so as to provide DC balancing within the frame.

According to a second aspect of the invention, there is provided use of an active matrix light modulator for reducing the effects of asymmetrical optical performance, the modulator comprising a plurality of pixels, an active matrix addressing arrangement for the pixels, and a pixel waveform generator for supplying each frame of image data as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe.

According to a third aspect of the present invention, there is provided an active matrix light modulator comprising: a plurality of data lines; a plurality of scan lines; an active matrix of control elements disposed at intersections of the data lines and scan lines; an array of pixels which are selectively addressable by data and scan signals applied to the control elements by way of the data and scan lines so as to be set to a first optical transmission state in response to a positive applied voltage of a particular magnitude, a second optical state in response to an intermediate applied voltage and a third optical state in response to a negative applied voltage of equal magnitude, but opposite polarity, to said positive applied voltage; and addressing means for addressing each pixel during a corresponding addressing frame by the application of data and scan signals to an associated one of the control elements in order to select the optical level of the pixel for each frame, characterised in that the pixels exhibit asymmetrical on-axis performance and in that the modulator comprises voltage inversion means for controlling the voltage applied to each pixel during successive subframes of each frame such that, when one optical level is selected for the frame, said positive voltage is applied to the pixel during one subframe of the frame and said negative voltage is applied to the pixel during another subframe of the frame and, when another optical level is selected for the frame, said intermediate voltage is applied to the pixel during both of the subframes of the frame, so as to provide DC balancing within the frame.

Such an active addressing arrangement makes the use of AFLCD's, for example, much more feasible since repeatable grey levels can be obtained due to the provision of DC balancing within a single addressing frame by virtue of the fact that the frame consists of the two sub-frames driven by voltages of opposite polarity. Such DC balancing avoids long term build up of ionic effects which would otherwise result in degradation of grey levels with time. Such an arrangement is also compatible with existing polysilicon active matrix drive circuitry providing low power addressing for materials with a high

spontaneous polarisation and ensuring that the state of each pixel is held during the frame time without requiring application of a constant holding voltage. Thus the use of AFLCD's with their inherent features of wide viewing angle, low power consumption and possible reflective use becomes feasible in a wide range of applications in association with the developing polycrystalline silicon technology, such as for very high quality desk top publishing displays.

Additionally such an arrangement can compensate for the asymmetrical voltage-transmission characteristics typically possessed by some AFLC materials by taking the temporal average of two subframes driven by voltages of opposite polarity so that any optical difference (intensity or chromaticity) between the positively and negatively driven subframes is averaged by the observer and is unimportant.

Preferably the intermediate applied voltage is zero voltage. However, it will be appreciated that, where the intermediate applied voltage is not zero, an opposite polarity voltage is required to provide DC balancing within the frame. Furthermore, although it is preferred that the positive and negative voltages are applied in the same order in each frame, it is also possible for the order of these voltages to be reversed in alternate frames.

In one embodiment, the first and third states are symmetrical in that they exhibit substantially the same optical level in response to said positive and negative applied voltages, and the voltage inversion means is arranged to apply said positive and negative voltages to the pixel during the two successive subframes when said one optical level is selected such that the same optical level is obtained during the two subframes.

In an alternative embodiment, the first and third optical states are asymmetrical in that they exhibit different optical levels in response to said positive and negative applied voltages, and the voltage inversion means is arranged to apply said positive and negative voltages to the pixel during the two successive subframes when said one optical level is selected such that different optical levels are obtained during the two subframes.

The voltage inversion means may be arranged to modulate addressing of each pixel by the addressing means by means of a voltage inversion switching waveform having 2N portions for addressing 2N subframes within the frame, where N is an integer greater than zero and consecutive portions have voltages of equal magnitude and duration but opposite polarity.

Furthermore, the voltage inversion means may be arranged to supply a voltage inversion switching waveform consisting of two portions having voltages of equal magnitude and duration but opposite polarity which follow one another substantially immediately. In an alternative embodiment, the voltage inversion means may be arranged to supply a voltage inversion switching waveform comprising portions having voltages of equal magnitude and duration but opposite polarity and a further portion of zero voltage.

In one embodiment, each of the pixels may be addressable so as to be set to one of a plurality of first optical states in response to a selected one of a plurality of different positive applied voltages or one of a plurality of third optical states in response to a selected one of a plurality of different negative applied voltages, and the voltage inversion means may be arranged to apply said selected positive voltage to the pixel during one subframe of the frame and said selected negative voltage to the pixel during another subframe of the frame in order to select one of a plurality of possible optical levels for the frame whilst maintaining DC balancing within the frame.

Preferably the active matrix incorporates a respective control element coupled to each pixel and having a data input for receiving data signals from a corresponding one of the data lines and a control input for receiving scan pulses from a corresponding one of the scan lines in order to switch the control element to supply a voltage to the pixel. Most preferably a storage capacitor is coupled to the output of the control element, and a buffer is connected between the output of the control element and the pixel.

Where the light modulator is a light transmissive liquid crystal device, the array may be disposed between polarisers arranged with their axes transverse to one another such that said first and third optical states are bright states and said second optical state is a dark state. Alternatively, the array may be disposed between polarisers arranged with their axes substantially parallel to one another such that said first and third optical states are dark states and said second optical state is a bright state. In a further alternative, the array may be disposed in series with a further array of similar form between polarisers arranged with their axes substantially parallel to one another, and the addressing means may be arranged to simultaneously apply addressing signals of opposite polarity to the arrays such that a dark level is obtained when one of the arrays is in said first optical state and the other array is in said third state and a bright level is obtained when both arrays are in said second optical state. In a further alternative, the array may be disposed between a polariser and a reflective surface with a quarter wave retarder being disposed between the array and the reflective surface such that a dark level is obtained when the array is in one of said first and third optical states and a bright level is obtained when the array is in said second optical state.

Where the light modulator is a diffractive spatial light modulator, the active matrix may incorporate a set of first elongate electrodes on one side of the array, a set of second elongate electrodes interdigitated with the set of first elongate electrodes on said one side of the array, and a set of pixel electrodes on the other side of the array each of which overlaps a plurality of first and second electrodes, the first and second electrodes being connected to respective supply lines for continuously applied voltages and each of the pixel electrodes being

addressable by the addressing means for switching between a diffractive mode and a non-diffractive mode, wherein the voltage inversion means is arranged to invert the voltages applied to the first and second electrodes about a predetermined voltage between the two subframes at the same time as inversion of the voltages applied to the pixel electrodes.

According to a fourth aspect of the invention, there is provided an active matrix spatial light modulator comprising a plurality of pixels, an active matrix addressing arrangement for the pixels, and a pixel waveform generator, characterised in that the pixels exhibit asymmetrical on-axis optical performance and in that the pixel waveform generator is arranged to supply each frame of image data as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe.

According to a fifth aspect of the invention, there is provided a display comprising: an active matrix spatial light modulator comprising plurality of pixels, an active matrix addressing arrangement for the pixels, and a pixel waveform generator; and an illumination system, characterised in that the pixel waveform generator is arranged to supply each frame of colour image data as a plurality of single colour frames of single colour image data and each single colour frame as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe, and in that the illumination system is arranged to illuminate the modulator with light of a colour corresponding to the colour of the colour image data currently being displayed by the modulator.

The first and second subframes of each single colour frame may be consecutive.

The pixels may exhibit symmetrical optical performance. The illumination system may be arranged to illuminate the modulator continuously during the first and second subframes of each single colour frame. The illumination system may be arranged to begin illuminating the modulator no earlier than completion of refreshing the modulator with each first subframe and to stop illuminating the modulator no later than commencement of refreshing the modulator with the subsequent first subframe.

The pixels may exhibit asymmetrical optical performance.

The first subframes of each subframe may be consecutive and the second subframes of each frame may be consecutive.

The illumination system may be arranged to be extinguished between consecutive subframes. The illumination system may be arranged to begin illuminating the modulator no earlier than completion of refreshing of the modulator with each subframe and to stop illuminating the modulator no later than commencement of refreshing the modulator with the subsequent subframe.

The single colour frames may comprise red, green and blue colour frames.

The modulator may comprise a liquid crystal device.

In order that the invention may be more fully understood, reference will now be made, by way of example, to the accompanying drawings, in which:

Figures 1a and 1b show ideal (symmetrical) voltage-transmission characteristics of an AFLC and typical (asymmetrical) voltage-transmission characteristics of an AFLC;

Figures 2a and 2b show the scan and the data waveforms used in a prior art AFLCD addressing scheme;

Figures 3a and 3b show a bipolar pulse and a bipolar pulse with gap for use in an addressing scheme of a device in accordance with the present invention;

Figures 4a and 4b show typical voltage-transmission characteristics of an AFLC for use in an AMLCD in accordance with the present invention.

Figures 5, 6 and 7 show measured waveforms used in accordance with the present invention for addressing a thresholdless AFLC, SBFLC and DHFLC respectively;

Figures 8 and 9 diagrammatically show two active matrix drive circuits which may be used in an AMLCD in accordance with the present invention;

Figures 10 and 11 show a portion of an AMLCD in accordance with the present invention and a voltage diagram showing the voltages applied to such a portion;

Figures 12a and 12b show liquid crystal transmission characteristics with respect to time on application of a bipolar pulse with gap at a high temperature and at a low temperature respectively;

Figure 13 diagrammatically illustrates an addressing scheme used in a diffractive light modulator in accordance with the present invention;

Figure 14 diagrammatically shows the electrode arrangement of such a diffractive light modulator;

Figures 15a, 15b and 15c show three addressing waveforms which may be used in devices in accordance with the present invention;

Figures 16, 17 and 18 show measured waveforms used in accordance with the present invention for addressing a thresholdless AFLC and SBFLC;

Figure 19 is a block schematic diagram of a colour sequential display constituting an embodiment of the invention;

Figures 20 to 22 shows addressing waveforms at (a) and (c), graphs of corresponding light transmission against time at (b) and (d), and a graph of emission against time of a multicoloured illumination system for three examples of the device of Figure 19;

Figure 23 shows measured waveforms using the addressing technique illustrated in Figure 22 for addressing an SBF material;

Figure 24 is a diagrammatic cross-sectional view of part of a transmissive AMLCD constituting an embodiment of the invention;

Figures 25 and 26 are diagrams illustrating operating of the AMLCD of Figure 24 during first and second subframes, respectively;

Figure 27 is a diagrammatic cross-sectional view of part of a transmissive double layer AMLCD constituting another embodiment of the invention;

Figures 28 and 29 are diagrams illustrating operation of the AMLCD of Figure 27 during first and second subframes, respectively;

Figure 30 is a diagrammatic cross-sectional view of part of a reflective AMLCD constituting a further embodiment of the invention; and

Figures 31 and 32 are diagrams illustrating operation of the AMLCD of Figure 30 during first and second subframes, respectively.

A preferred addressing scheme to be used in an active matrix liquid crystal display (AMLCD) in accordance with the present invention will now be described. Such an addressing scheme requires use of a liquid crystal material exhibiting voltage-transmission characteristics which are free or almost free from hysteresis. Such materials include thresholdless antiferroelectric liquid crystal (TAFLC) materials, deformed helix ferroelectric liquid crystal (DHFLC) materials and short-pitch bistable ferroelectric liquid crystal (SBFLC) materials. The addressing scheme also requires the use of an active matrix incorporating switching elements which are preferably in the form of thin film transistors (TFT) or thin film diodes (TFD), such as is disclosed, for example, in GB 2 312 773 and EP 0 807 918 which are referred to above and the contents of which are incorporated herein by reference.

Furthermore, the addressing scheme makes use of bipolar switching within each addressing frame so that the voltage applied across a pixel is of the form shown in either Figure 3a or Figure 3b, in order to provide voltage inversion between successive subframes within a single addressing frame and to thereby provide DC balancing within the addressing frame. A gap may be provided between the positive and negative parts of the switching waveform, as shown in Figure 3b.

In the case of the bipolar switching waveform of Figure 3a, the voltage V applied across the pixel as a function of time t ($0 \leq t < T$), during a frame of period T satisfies the requirement:

$$V(t + T/2) = - V(t) \text{ for } 0 \leq t < \frac{T}{2}$$

In the case of the bipolar switching waveform of Figure 3b having an intermediate gap of duration t_1, the voltage V applied across the pixel satisfies the requirements:

$$V=0 \text{ for } \frac{T-t_1}{2} \leq t < \frac{T+t_1}{2}$$

$$V(t+\frac{t_1+T}{2}) = -V(t) \text{ for } 0 \leq t < +\frac{T-t_1}{2}$$

In each case, each frame is made up of 2N consecutive subframes, where N is an integer, consisting of N subframes of one polarity alternating with N subframes of the opposite polarity with a voltage of the same magnitude but opposite sign to the voltage of the subframes of the one polarity.

Because such an addressing scheme makes use of two (or more) subframes within each addressing frame, the switching waveform being of opposite polarity in the two subframes and passing through zero between each pair of adjacent subframes, so that DC balancing is provided within each frame, the required grey level within each frame is accurately reproduced and is rendered substantially independent of the previous state, without requiring a reset period.

Figure 4a shows the on-axis light transmission of a TAFLC, which may be used in the AMLCD of the invention, as a function of the applied voltage, showing the antiferroelectric (AF) maximum dark state at zero volts and the ferroelectric (+F and -F) bright states symmetrically positioned relative to the AF state. On switching of such a device, a smooth transition is obtained between the AF and F states and only narrow hysteresis is observed on returning to the AF state by comparison with the case of AFLC's exhibiting appreciable hysteresis as shown in Figures 1a and 1b. A. Fukuda, Asia Display 1995, p. 61-64 describes such a TAFLC. Furthermore, full switching is obtained at much lower voltages, for example at voltages of the order of 5V as compared with such AFLC's. Such low voltages imply that TAFLC's

can be addressed by an active matrix, such as a TFT matrix for example. However TAFLC's possess a large spontaneous polarisation which makes the use of conventional amorphous silicon TFT's difficult. Nevertheless such difficulties can be overcome by making use of an active matrix circuit utilising polysilicon TFT's, such as that disclosed in GB 2 312 773 and EP 0 807 918 for example.

Figure 4b shows the corresponding on-axis voltage-transmission characteristics of a further TAFLC, which may be used in the AMLCD of the invention, in which the ferroelectric (+F and -F) bright states are asymmetrically positioned relative to the antiferroelectric (AF) state. Figure 4b also illustrates the asymmetric performance for off-axis viewing positions of liquid crystals which exhibit symmetrical on-axis performance as illustrated in Figure 4a.

Conventional AFLC materials with wide hysteresis and large voltage thresholds would not generally be suitable for the device of the invention in that they require larger voltages to switch which are incompatible with active matrix addressing, and they tend to have a hysteresis curve which rises sharply over a narrow voltage range up to maximum transmission, thus allowing for fewer grey levels. Also, since their hysteresis loop is wide, they take a long time to relax to the AF state and such relaxation may not occur within the available frame time, with the result that the subsequent grey level will be affected by the previous state. By contrast, TAFLC materials tend to have a narrow hysteresis loop and a less steep hysteresis curve up to maximum transmission, thus allowing faster driving and more grey levels to be accessible

Before describing in detail possible active matrix circuits which may be implemented for carrying out the addressing scheme used in the device in accordance with the present invention described above, three examples will be described with reference to Figures 5, 6 and 7 of experiments conducted with TAFLC, SBFLC and DHFLC materials utilising such an addressing scheme.

Example 1

Experiments were conducted in a 2micrometres thick antiparallel aligned cell filled with thresholdless AFLC material. The cell was rotated between crossed polarisers to give minimum transmission with zero volts applied (an embodiment of this type is described in more detail hereinafter). Because of the particular material-alignment combination chosen, the cell showed asymmetric on-axis transmission behaviour, that is the light transmission obtained from the application of voltages of the same magnitude but opposite polarity was not equivalent. The cell was addressed using a bipolar frame of 20 milliseconds duration, made up of two subframes of equal but opposite voltage, as shown in the upper part of Figure 5. The total light transmission for each frame, as shown in the lower part of Figure 5, was composed of two unequal contributions from each subframe, the total brightness being determined by the voltage applied. As each frame was DC balanced and the AF state was reached before addressing the next frame, there was no ion build up and therefore reproducible grey levels could be achieved without requiring an ionic reset pulse. Therefore the cell could be addressed by continually applying bipolar pulses of varying voltage (0-5V) and the level of grey was reproducible, being essentially independent of the previous state. A suitable TAFLC material which may be used in such an example is MLC0076 as disclosed by S.S. Seomun et al, "Electrooptic Property of a Binary Mixture of Ferroelectric and Antiferroelectric Chiral Compounds Showing Threshholdless V-shaped switching", Third International Display Workshops, Lcp 1-4 (1996), p. 61-64.

Example 2

Experiments were conducted in a 2 micrometres thick antiparallel aligned cell filled with a SBFLC material. The cell was rotated between crossed polarisers to give minimum transmission with zero volts applied. The cell showed substantially symmetric on-axis transmission behaviour, that is the light transmission obtained from the application of voltages of the same magnitude but opposite polarity was approximately equivalent. The cell was addressed using a bipolar frame of 20 milliseconds duration, made up of two subframes of equal but opposite voltage, as shown in the upper part of Figure 6. The total light transmission for each frame, as shown in the lower part of Figure 6, was composed of two equal contributions from each subframe, the total brightness being determined by the voltage applied. As each frame was DC balanced and the relaxed state was reached before addressing the next frame, there was no ion build up and therefore reproducible grey levels could be achieved without requiring an ionic reset pulse. Therefore the cell could be addressed by continually applying bipolar pulses of varying voltage (0-3V) and the level of grey was reproducible, being essentially independent of the previous state. A suitable SBFLC material which may be used in such an example is FLC6430 supplied by F. Hoffmann - La Roche and disclosed by J. Fünfschilling, Japanese Journal of Applied Physics, vol. 40, No. 4, p. 741-746 (1991).

Example 3

Experiments were conducted in a 2micrometres thick antiparallel aligned cell filled with a DHFLC material. The cell was rotated between crossed polarisers to give minimum transmission with zero volts applied. The cell showed asymmetric on-axis transmission behaviour, that is the light transmission obtained from the application of voltages of the same magnitude but opposite polarity was not equivalent. The cell was addressed using a bipolar frame of 20 milliseconds duration, made

up of two subframes of equal but opposite voltage, as shown in the upper part of Figure 7. The total light transmission, as shown in the lower part of Figure 7, for each frame was composed of two unequal contributions from each subframe, the total brightness being determined by the voltage applied. As each frame was DC balanced and the AF state was reached before addressing the next frame, there was no ion build up and therefore reproducible grey levels could be achieved without requiring an ionic reset pulse. Therefore the cell could be addressed by continually applying bipolar pulses of varying voltage (0-3V) and the level of grey was reproducible, being essentially independent of the previous state. A suitable DHFLC material which may be used in such an example is FLC10150 supplied by ROLIC and disclosed by G. Cnossen et al, SID 96 Digest, p. 695-698 (1996).

In order to implement the addressing scheme in an AMLCD utilising TAFLC, SBFLC or DHFLC material in accordance with the present invention described above, it is necessary to apply a substantially constant voltage across the liquid crystal material during each of the subframes of the bipolar switching waveform shown in Figure 3a or 3b, and the application of such a voltage can be achieved in two different ways. In a first embodiment shown in Figure 8, a regular rectangular active matrix array 10 of pixels comprises column electrodes addressed by a data driver 12 and row electrodes addressed by a scan driver 14, the active circuit 16 associated with each pixel comprising a polysilicon thin film field effect transistor 18 connected by its gate to the scan electrode 20 and by its drain to the data electrode 22, and a fixed storage capacitor 24 connected to the source of the transistor 18 in parallel with the pixel capacitance 26. When the electrode 20 receives a scan pulse from the scan driver 14, the transistor 18 is turned on in order to cause the voltage on the data electrode 22 applied by the data driver 12 to charge up the storage capacitor 24. When the scan pulse is removed from the scan electrode 20, the transistor 18 is turned off in order to isolate the storage capacitor 24 from the data electrode 22 so that the light transmission of the pixel corresponds to the voltage across the storage capacitor 24 until it is refreshed during the next frame. Since the spontaneous polarisation of the liquid crystal modes used is high, it is necessary to apply a large amount of charge to the pixel, and accordingly a large storage capacitor 24 is required to effect the charge transfer at substantially constant voltage. However the charge must be transferred within a scan line period and this requires considerable peak currents to flow, thereby dissipating considerable power. Furthermore a large storage capacitor would have a deleterious impact on the aperture ratio of the display.

An alternative active circuit 16' for use in the AMLCD of the present invention is shown in Figure 9 and includes, in addition to the components already referred to, a buffer amplifier 28 having unity voltage gain connected between the storage capacitor 24 and the pixel capacitance 26. The buffer amplifier 28 has a very high input impedance and a relatively low output impedance so that, when the transistor 18 is turned off, the output of the amplifier 28 follows the voltage across the storage capacitor 24 whereas the current supplied to the input of the amplifier 28 is negligible so that discharge of the storage capacitor 24 is much slower than in the previous circuit arrangement. Accordingly the storage capacitor 24 can be a relatively small capacitor which can be easily charged up to the desired voltage on turning on of the transistor 18. The pixel connected to the output of the amplifier 28 receives a constant voltage equal to the voltage on the storage capacitor 24, and, since the charge is supplied at the rate at which the liquid crystal material switches, the circuit consumes less dynamic power than the previously described active circuit. The buffer amplifier can also implement the subframe inversion required in the addressing scheme of the invention in order to achieve repeatable grey levels as described above.

In order that the operation of such a circuit can be fully understood, reference will now be made to Figure 10 which shows four pixels A, B, C and D disposed at the intersections of two scan electrodes 20a, 20b and two data electrodes 22a, 22b, . A corresponding voltage diagram is provided in Figure 11 showing the scan voltages applied to the scan electrodes 20a and 20b, the data voltage applied to the data electrode 22a, and the voltages V_{S1} and V_{LC1} applied to the storage capacitor 24 and the pixel capacitance 26 of the pixel A during two subframes of the addressing frame.

Referring to Figure 11, beginning at t = 0, a scan voltage of say, 12V is applied to the scan electrode 20a in order to turn on the transistor 18 of pixel A, the voltage being maintained for the duration of the line time after which the voltage on the scan electrode 20a is 0V for the rest of the half-frame. The turning on of the transistor 18 causes the voltage + V_{dat} on the data electrode 22a to charge up the storage capacitor 24 as well as the pixel capacitance 26. The pixel voltage is thereby changed from $V_{previous}$, the voltage level of the previous address line, to the applied data voltage V_{dat} which will vary in magnitude depending on the state selected for the pixel. The same voltage is then held on the storage capacitor 24 (V_{S1}) and the pixel capacitance (V_{LC1}) for the rest of the half-frame. At the start of the second half-frame, the same scan voltage is applied to the scan electrode 20a, but a negative data voltage -V_{dat} is applied to the data electrode 22a with the result that the voltages held on the storage capacitor 24 and the pixel capacitance 26 are changed to - V_{dat} and are held for the rest of the second half-frame. It will accordingly be appreciated that the voltage applied to the pixel A will be inverted between successive half-frames within the addressing frame in order to provide DC balancing within the frame.

The data voltages applied to the data electrodes such as 22a and 22b are continuously applied during

each half-frame, and a scan voltage is applied to the scan electrode 20b during the line time following the line time in which the scan voltage was previously applied to the scan electrode 20a in order to turn on the transistor 18 of the next pixel C to be addressed in the half-frame. This sequence is repeated for all the pixels of the display, and, following voltage inversion, addressing of the pixels is then effected in similar manner during the second half-frame except that the data voltages are inverted. In an alternative drive scheme, the voltage on the storage capacitor is the same in the two half-frames, but the buffer amplifier 28 of each pixel is caused to invert the polarity of the signal applied to the pixel during the second half-frame.

It will be appreciated that the above described addressing scheme produces a bipolar switching waveform without gap as shown in Figure 3a. However a bipolar switching waveform with gap as shown in Figure 3b can be produced in a similar manner except that, instead of each frame being divided into two half-frames with a positive data voltage + V_{dot} being applied to the data electrode 22a in the first half-frame and a negative data voltage - V_{dot} being applied to the data electrode 22a in the second half-frame, each frame is divided into three part-frames with a positive data voltage being applied to the data electrode 22a in one part-frame, a negative data voltage being applied to the data electrode 22a in another part-frame, and zero voltage being applied to the data electrode 22a in a further part-frame which may be intermediate the other two part-frames or at the beginning or end of the frame. The duration of the positive and negative voltage part-frames should be equal (x/3 of frame period), whereas the duration of the zero voltage part-frame will typically be substantially less (y/3 of frame time, where $2x/3 + y/3 = 3/3 = 1$ and $y << x$). Similar scan voltages are applied to the scan electrodes 20a and 20b at the start of the positive and negative part-frames (but not at the start of the zero voltage part-frame) as are applied at the start of the two half-frames in the bipolar switching waveform without gap addressing scheme already described. Thus, a bipolar switching waveform is produced comprising portions having voltages of equal magnitude and duration but opposite polarity and a further portion of zero voltage.

Whilst the above described circuit arrangements can be implemented with an addressing scheme based on a bipolar switching waveform without gap as shown in Figure 3a or a bipolar switching waveform with gap as shown in Figure 3b, a potential advantage of using a bipolar switching waveform with gap is that it will tend to average the light transmission obtained if the material viscosity changes with temperature. As shown in Figure 12a, the lower viscosity of the material which is typically obtained at higher temperatures allows the material to respond more quickly to an electric field, and this is reflected in the form of the corresponding transmission characteristic against time. On the other hand, the viscosity of the material typically increases with decreasing temperature, thus leading to a decrease in the response of the material. However, by increasing the length of the gap of the bipolar switching waveform as shown in Figure 12b, the transmission characteristic can be altered so as to compensate for changes in temperature.

Such an addressing scheme can also be applied to an AFLCD comprising two AFLC cells arranged in series between a pair of polarisers having parallel axes and set such that the display as a whole is in the bright state at zero volts and the application of voltages of opposite polarities to the cells causes the respective optic axes of the cells to rotate in opposite directions so that the light transmission of the display becomes darker. In this case, each of the two cells is addressed by a similar bipolar addressing scheme. Furthermore, the bipolar addressing scheme may be applied to a single polariser reflection AFLCD incorporating a quarter wave plate with its axis parallel to the polariser axis so that the bright state is obtained at zero volts and the transmission becomes darker when a voltage of either polarity is applied to the display. Embodiments of both of these types are described in more detail hereinafter.

Such an addressing scheme is also applicable to an active matrix liquid crystal grating panel constituting a diffractive spatial light modulator (SLM) such as is disclosed in GB 2 313 920 and EP 0 811 872, the contents of which are incorporated herein by reference. Such a diffractive SLM, which may have a transmission geometry or a reflection geometry, comprises top and bottom substrates made of glass and ferroelectric liquid crystal material disposed between the substrates. The top substrate carries two sets of interdigitated transparent electrodes 20 and 21, as shown in broken lines in Figure 14, with the electrodes of each set being connected together and interdigitated with the electrodes of the other set so that only two connections are required to opposite sides of the top substrate. The bottom substrate 2 carries a rectangular array of pixel electrodes 23, as shown in solid lines in Figure 14, each pixel electrode 23 facing a plurality of interdigitated electrodes 20 and 21.

By applying suitable voltages to the various electrodes, each pixel can be switched between a non-diffractive mode in which light is transmitted or reflected in the zeroth order of diffraction, and a diffractive mode in which the pixel forms a phase-only diffraction grating and light is diffracted in non-zeroth orders of diffraction. In the diffractive mode, each pixel comprises a plurality of strip regions of liquid crystal material in which adjacent regions are in different states such that light beams passing through adjacent strip regions undergo a relative phase shift of 180 degrees. In the non-diffractive mode, all light passing through the pixel is subject to substantially the same phase change. By collecting light diffracted in the first order of diffraction for example for display, each pixel will appear dark in the non-diffractive mode and light in the diffractive mode.

Furthermore, each pixel may be addressable by

way of an active circuit 16 associated with each pixel electrode 17 and shown diagrammatically on an enlarged scale in Figure 14. In the arrangement illustrated, each pixel electrode 17 is connected to the source of a polysilicon thin film field effect transistor, and the drains of the transistors of each column of pixels are connected to a respective column or data electrode 22, whereas the gates of the transistors of each row are connected to a respective row or scan electrode 20. The pixels are thus enabled one row at a time so that data for a complete row are written simultaneously.

British Patent Application No. 9702076.2 and European Patent Application No. 98300627.1 (the contents of which are incorporated herein by reference) disclose an addressing scheme for switching between the diffractive and non-diffractive modes of the pixels in which, in order to provide a net voltage across each strip region when averaged over time which is equal to zero, all the electrode voltages are reversed about an arbitrary voltage Varb during alternate addressing frames. Thus, during a first frame (FRAME 1), the pixel ON mode (the diffractive mode) is defined by continuous voltages V1 and V2 applied to the interdigitated electrodes 19 and 21 via supply lines 19' and 21', respectively, and a write voltage V_{write} applied to the pixel electrode 17 such that V_{write} is between V1 and V2. This causes adjacent strips of liquid crystal material to be switched oppositely such that the pixel acts as a phase-only diffraction grating. The pixel OFF mode (the non-diffractive mode) is defined by the same continuous voltages V1 and V2 applied to the interdigitated electrodes 19 and 21 and an erase voltage V_{erase} applied to the pixel electrode 17 such that V_{erase} is below V1 and V2. This causes adjacent strip regions to be switched to the same state and means that light passing through the strip regions is subjected to the same phase shift so that the pixel does not diffract light. In a second frame (FRAME 2), the ON and OFF modes of the pixel are similarly defined except that the continuous voltages applied to the interdigitated electrodes 19 and 21 are (Varb - V1) and (Varb - V2), the write voltage applied to the pixel electrode 17 is (Varb - V_{write}) and the erase voltage applied to the pixel electrode 17 is (Varb - V_{erase}) so that the electric field directions are reversed for the ON and OFF modes of the pixel as compared with FRAME 1 in order to provide DC balancing over a large number of frames. Because the image data generally changes with time, such DC balancing relies on statistical averaging over a period of time, and perfect DC balancing over short periods of time is not of course possible with such an addressing scheme.

By contrast, the addressing scheme applied to the SLM in accordance with the invention, which is illustrated diagrammatically in Figure 13, provides DC balancing within each addressing frame, rather than relying on statistical averaging over a period of time. In this case, all the electrode voltages are inverted about an arbitrary voltage Varb, which may be for example 5 volts, during successive subframes within a single addressing frame. Thus, in the example given in Figure 13, the ON mode of the pixel in a first subframe, SUBFRAME Ia, is defined by continuous voltages V1 and V2, of 15 volts and 5 volts for example, applied to the interdigitated electrodes 19 and 21 and a write voltage V_{write}, of 10 volts for example, applied to the pixel electrode 17 such that V_{write} is between V1 and V2, whereas the OFF mode of the pixel is defined by the same voltages V1 and V2 applied to the interdigitated electrodes 19 and 21 and an erase voltage V_{erase}, of 0 volts for example, applied to the pixel electrode 17 such that V_{erase} is below V1 and V2. In a second subframe of the same frame, SUBFRAME 1b, the ON mode of the pixel is defined by continuous voltages (Varb - V1) and (Varb - V2) applied to the interdigitated electrodes 19 and 21 and a write voltage V'_{write} equal to (Varb - V_{write}) applied to the pixel electrode 17, whereas the OFF mode of the pixel is defined by the same voltages (Varb - V1) and (Varb - V2) applied to the interdigitated electrodes 19 and 21 and an erase voltage V'_{erase} equal to (Varb - V_{erase}) applied to the pixel electrode 17.

Such an addressing scheme provides DC balancing within a single addressing frame whilst simultaneously ensuring that the optical properties of the phase grating remain identical during the two subframes. The grating is written by applying a write voltage V_{write} to the pixel electrode 17 which overlaps a plurality of the interdigitated electrodes 19 and 21 to which continuous voltages are globally applied which are reversed between successive subframes as described above, whereas erasing is achieved by applying a voltage V_{erase} to the pixel electrode 17 which lies sufficiently below both V1 and V2 as to ensure full switching of the pixel into the non-diffractive mode. In each, case both the write voltage and the erase voltage are alternated between successive subframes as described above.

Such an addressing scheme relies on driving the device using two subframes and performing a voltage inversion at the mid point of the frame between the two subframes. The addressing scheme may be implemented using a standard SRAM pixel architecture since the globally applied voltages on the interdigitated electrodes and the voltages applied to the pixel electrodes can then be inverted simultaneously (which is not possible with DRAM pixel architecture). In practice, all the voltages might be inverted about the mean of the voltage range accessible by the SRAM (as shown in the example of Figure 11). It is to be noted that there is no theoretical difference in the optical appearance of a phase diffraction grating and its inverse in such a device so that true intra-frame DC balancing is provided whilst maintaining the optical appearance. Furthermore, where the device is to be used to obtain analogue greyscale, such an addressing scheme enables analogue grey levels to be obtained whilst avoiding any significant historical dependence of such grey levels caused by ionic memory.

Figures 15a, 15b and 15c show three bipolar switching waveforms which may be applied to a TAFLC or SBFLC material in an addressing scheme in accordance with the invention. In the case of Figure 15a, voltage inversion occurs between successive subframes as described above with reference to Figures 3a and 3b, and there is a polarity change between successive frames A and B so that the voltage passes through zero between each successive frame. In the case of Figure 15b and 15c, however, whilst voltage inversion is still provided between successive subframes in each frame, the first subframe is not of the same polarity in each frame so that the second subframe of the frame A is of the same polarity as the first subframe of the following frame B and the voltage does not pass through zero between successive frames. In each case, the voltage magnitudes of the pulses in the frames A and B are given as 0.5V and 1.0V by way of example only.

Figures 16, 17 and 18 show examples of the addressing of thresholdless AFLC material with switching waveforms of the general type shown in Figure 15a (in the case of Figure 16) and of a general type shown in Figures 15b and 15c (in the case of Figures 17 and 18). The total on-axis light transmission for each frame, as shown in the upper part of each figure, was composed of two unequal contributions from each subframe, the total brightness being determined by the voltage applied as in the case of the earlier examples described. The same level of reproducibility of grey levels was obtained utilising the waveforms of Figures 15b and 15c as with the waveform of Figure 15a, but the additional advantage was obtained with the waveforms of Figures 15b and 15c that the transmission level for a particular voltage was increased. This was around a 20% increase for the thresholdless AFLC material, and would probably somewhat lower in the case of a SBFLC material due to the faster switching.

Figure 19 illustrates a colour sequential direct view liquid crystal display comprising an LCD panel 30 which may be embodied using any of the addressing schemes described hereinbefore and using any of the display arrangements described hereinbefore and suitable for use in direct view displays. The panel 30 has an input 31 for receiving a serial video signal of analogue or digital type. The panel 30 also has an input 32 for receiving timing signals for synchronising the refreshing of rows and frames with the video signal at the input 31.

The display further comprises a multi-coloured illumination system 33 arranged as a backlight for the panel 30. The system 33 is connected to a colour switching circuit 34 having an input connected to the input 32 for synchronising operation of the system 33. In particular, the illumination system 33 is controlled by the circuit 34 so as to provide red, green and blue illumination of the panel 30 in sequence. For instance, the system 33 may comprise individually controllable red, green and blue light sources, each of which may comprise a coloured light emitter or a white light source and a fixed colour filter. As an alternative, the system 33 may comprise a switchable white light source and a switchable colour filter arrangement whose passband is switchable to pass red, green and blue light.

Figure 20 illustrates an addressing scheme which is suitable for use with a panel 30 having a substantially symmetrical optical response throughout the desired viewing region. In particular, the optical transmission of each pixel of the panel 30 is the same for addressing signals of the same magnitude but of opposite polarities for on-axis viewing and for off-axis viewing throughout a sufficient range of viewing angles for the intended application of the display.

Figure 20 shows at (a) a typical or arbitrary pixel waveform for one complete frame of colour video data. In particular, the waveform shown at (a) is that which is applied to a pixel in a first row to be addressed of a typical frame. Similarly, Figure 20 shows at (c) the same waveform used for addressing the same pixel colour of a pixel in the last row to be addressed in the same frame. The waveforms are shown against the same time axis and illustrate the time delay between refreshing the first and last rows to be addressed of a complete frame of colour video data.

The frame is divided into three individual colour subframes, each of which is divided into first and second subframes. During the first of these subframes, the pixels of the panel 30 are refreshed with red image data by positive addressing pulses as illustrated by Vr for the pixels whose waveforms are shown at (a) and (c). The responses of these pixels are illustrated at (b) and (d), respectively, which illustrate the transmission against time of the pixels.

During the next subframe, the pixel voltages are inverted as illustrated by the pixel voltages -Vr for the pixel waveforms at (a) and (c). As shown at (b) and (d), the transmission performances of the pixels are substantially the same irrespective of whether the pixel voltage is positive or negative.

During the next two subframes, positive and negative pixel voltages are supplied corresponding to the desired green level to be displayed by the pixels. This is followed by two subframes in which positive and negative blue pixel voltages such as Vb and - Vb are applied to the pixels of the panel 30. This sequence is then repeated for subsequent frames of video data.

Figure 20 illustrates at (e) the operation of the multi-coloured illumination system 33 controlled by the colour switching circuit 34. Red, green and blue illumination is provided during the time periods when the panel 30 displays red, green and blue image data, respectively. In order to avoid crosstalk between the colour images, the illumination system 33 is switched off during the transitions between the red, green and blue image data. The relative timings are illustrated for the green image data at (e) in Figure 20. The colour switching circuit 34 is controlled by the timing signals at the input 32 to extinguish the illumination system 33 until time T1 when all of the

pixels of the panel 30 have been refreshed with the first green image subframe. Thus, the green illumination provided by the system 33 is switched on when the last row of pixels have been refreshed and have responded fully so as to achieve the desired transmission as illustrated at (d) in Figure 20. This ensures that even illumination of the pixels across the whole panel 30 is achieved.

The next subframe also contains green image data and it is not therefore necessary to extinguish the illumination system 33 during refreshing of the next subframe. However, in order to ensure even illumination of the whole panel 30 and to avoid crosstalk between the green and blue image data, the circuit 34 extinguishes the illumination system 33 at the start of refreshing the pixels with the following subframe of blue image data. As shown in Figure 20, this occurs at time T2 when the first row of pixels to be addressed is refreshed with the first subframe of blue image data.

In order to achieve the brightest possible display, green illumination is provided throughout the period between the times T1 and T2 as shown in Figure 20. However, the actual times of switching on and off the illumination systems 33 may vary so as to take into account any delays in emitting light and ceasing to emit light following the switching signals from the circuit 34. Thus, the illumination system may be switched on for green illumination slightly before the time T1 to ensure maximum illumination and may need to be switched off slightly before the time T2 to avoid crosstalk between the green and blue colour data. Also, the green illumination may be provided during a shorter time interval between these limit points if necessary or desirable, for instance to achieve a different compromise between display brightness and colour crosstalk.

Figure 21 is similar to Figure 20 but illustrates a different addressing scheme in which the illumination system 33 is switched on and off during each of the six subframes making up the full colour frame. The waveforms shown at (a) and (c) in Figure 21 are substantially identical to those shown at (a) and (c), respectively, in Figure 20. As shown at (e) in Figure 21, for instance for the two red subframes of opposite pixel voltage polarity, the illumination system 33 is switched by the circuit 34 to produce red light when the pixels of the panel 30 have been refreshed with the first subframe of red image data. The red illumination is then switched off when the next subframe of red image data begins i.e. with refreshing of the first row to be addressed by the negative pixel voltages. The red illumination is then switched on and off in the same way during the next subframe. Similarly, green illumination is switched on and off during each of the subframes of green image data and the blue illumination is switched on and off during each of the subframes of blue image data.

Figure 21 also illustrates an asymmetric pixel response to equal magnitude but opposite polarity pixel voltages. In this case, each pixel has a higher transmission as a result of a positive pixel voltage than as a result as a negative pixel voltage of the same magnitude. However, because the individual colour images are refreshed twice for each complete frame of colour video data, the "flicker frequency" resulting from the asymmetric response occurs at the frame frequency and is less perceptible or imperceptible to a viewer. This in turn allows the use of liquid crystal arrangements which have asymmetric optical responses on-axis and extends the viewing region of liquid crystal arrangements having symmetrical on-axis optical performance but asymmetrical off-axis optical response.

Figure 22 illustrates an addressing scheme which differs from those shown in Figures 20 and 21 in that the two subframes of each colour component are no longer consecutive. As illustrated at (a) and (c) in Figure 22, a complete colour frame comprises six subframes which represent "positive" red image data, "negative" green image data, "positive" blue image data, "negative" red image data, "positive" green image data and "negative" blue image data. Although consecutive subframes are of opposite polarity, the sequence of colour image data is now "red, green, blue, red, green, blue" for the complete colour frame. The switching of the illumination system 33 corresponds to this and is illustrated at (e) in Figure 22. Thus, the illumination system 33 is "flashed" for each subframe and is switched on from when pixels in the last line of a subframe reach equilibrium and off when pixels in the first line leave equilibrium.

The optical responses of the pixels shown at (b) and (d) in Figure 22 are for the symmetrical optical response case but the addressing scheme may equally well be used for the asymmetrical optical response case.

The addressing scheme illustrated in Figure 22 has the advantage that each individual colour is "flashed" at a high frequency than the frequency for the scheme illustrated in Figure 20 and the effective frequency for the scheme illustrated in Figure 21, where each colour is flashed twice in succession. This reduces or suppresses the known artifact of "colour break-up" and thus improves image quality.

Figure 23 illustrates measured results obtained using the addressing scheme illustrated in Figure 22 for an SBF material. In this case, each substantially constant voltage period of the pixel waveform is approximately 2.78 milliseconds. The details of the cell are as described hereinbefore with reference to Example 2.

Figure 24 illustrates part of a pixelated AMLCD using an AFLC and being of the type described hereinbefore as Example 1. The device comprises a glass substrate 40 on which are formed pixel electrodes 41, for example made of indium tin oxide (ITO). An alignment layer 42, for instance comprising a rubbed polyimide layer, is formed on the substrate 40 and the electrodes 41. Similarly, a glass substrate 43 carries a common electrode 44 of ITO, on which is formed an alignment layer 45, for instance also of rubbed polyimide. The substrates 40 and 43 are spaced apart to define a cell containing a layer 46 of AFLC.

As illustrated in Figures 25 and 26, the device also comprises polarisers 47 and 48 having vertical and horizontal polarisation transmission directions, respectively. The device operates in the transmissive mode and is "normally black" ie. provides maximum attenuation of light in the absence of an applied field across the layer 46.

Figures 25 and 26 illustrate operation of four pixels 49 to 52 of the device displaying arbitrary image data in first and second subframes of a frame. In the first subframe as illustrated in Figure 25, the pixels 49 and 50 have no applied field. The optic axes of the pixels 49 and 50 are oriented vertically so that the liquid crystal of these pixels has no effect on the direction of polarisation of light entering the layer 46 via the polariser 47. Vertically polarised light passing through the pixels 49 and 50 is extinguished by the polariser 48 so that these pixels appear dark.

In the first subframe, a positive electric field is applied across the pixels 51 and 52 so that the optic axes of the liquid crystal of these pixels are rotated from the vertical as illustrated in Figure 25. The dielectric anisotropy and the thickness of the layer 46 are such that the pixels 51 and 52 act as half waveplates so that the polarisation of light passing through the pixels 51 and 52 from the polariser 47 is rotated by twice the angle between the optic axes of the pixels 51 and 52 and the vertical. Light from the pixels 51 and 52 is thus at least partly transmitted by the polariser 48 so that these pixels appear bright.

Figure 26 illustrates operation of the pixels 49 to 52 during the second subframe. The zero applied field across the liquid crystal of the pixels 49 and 50 remains unchanged so that these pixels continue to appear dark. However, the applied field across the liquid crystal of the pixels 51 and 52 is of the same magnitude but of opposite polarity so that the optic axes of these pixels are rotated in the opposite direction. Accordingly, these pixels appear bright.

Figure 27 illustrates a double layer embodiment of a transmissive display. The display comprises the components 40 to 48 as illustrated in Figures 24 to 26. In addition, the display of Figure 27 comprises a further device comprising a glass substrate 40 , ITO pixel electrodes 41', an alignment layer 42 , an ITO common electrode 44 , an alignment layer 45' and a layer 46' of AFLC. The glass substrate 43 acts as a substrate also for the electrode 44' alignment 45'. The pixel electrodes 41 and 41' are optically aligned with each other so that the pixels formed in the layers 46 and 46' are optically in series with each other and are addressed so as to be controlled together.

As illustrated in Figure 28 for a first subframe, the pixels 49, 50, 49' and 50', have a zero applied field so that their optic axes are vertical and parallel to the polarisation transmission direction of the polariser 47. These pixels therefore have no substantial effect on the polarisation of light from the polariser 47. The polarisation transmission direction of the polariser 48 is, in this embodiment, parallel to that of the polariser 47 so that these pixels appear bright.

The pixels 51 and 52 of the layer 46 have a positive applied field whereas the pixels 51' and 52'of the layer 46' have a negative applied field of the same magnitude. Thus, the optic axes of the pixels 51 and 52 are rotated by α in a clockwise direction from the vertical whereas the optic axes of the pixels 51' and 52' are rotated by the same angle but in an anti-clockwise direction from the vertical. The layers 46 and 46' act as half waveplates so that the polarisation vector of light from the polariser 47 is rotated so as to be substantially perpendicular to the polarisation transmission direction of the polariser 48. These pixels therefore appear dark.

Operation during the second subframe is illustrated in Figure 29 and, as described with reference to Figures 25 and 26, the applied fields across the pixels 51 and 52 of the layer 46 and 51' and 52' of the layer 46' are rotated in the opposite directions. These pixels therefore again appear dark.

Figure 30 illustrates a single layer reflective device which differs from that shown in Figure 24 in that the common electrode 44 is made of metal, such as silver or aluminum, and is reflective to light. Also, a quarter wave retarder 53 is disposed between the electrode and reflector 44 and the alignment layer 45.

Figure 31 illustrates operation of the device of Figure 30 during a first subframe. The state of the pixels 49 to 52 are as described for Figure 25. Thus, the polarisation of light from the polariser 47 passing through the pixels 49 and 50 and through the retarder 54 is unchanged and such light is reflected by the electrode and reflector 44 back through the retarder 53, the pixels 49 and 50 and the polariser 47. These pixels therefore appear bright.

Light from the polariser 47 passing through the pixels 51 and 52 has its polarisation vector rotated such that the retarder 53 converts the polarisation from linear polarisation to circular or elliptical polarisation. The polarisation of such light reflected by the electrode and reflector 44 is reversed and converted to linear polarisation by the retarder 53. The linear polarisation of light passing back through the pixels 51 and 52 is rotated so as to be substantially perpendicular to the polarisation transmission direction of the polariser 47. These pixels therefore appear dark.

As illustrated in Figure 32, during the second subframe, the optic axes of the pixels 51 and 52 are rotated in the opposite direction from the vertical compared with the first subframe. Otherwise, operation is substantially the same so that the pixels 49 and 50 appear bright whereas the pixels 51 and 52 appear dark.

Various modifications may be made within the scope of the invention. For instance, in the devices shown in Figures 24 to 26, the polarisation transmission directions of the polarisers 47 and 48 may be parallel, in which case the device is of the normally white type.

Similarly, the polarisation transmission directions of the polarisers 47 and 48 in the embodiment illustrated in Figures 27 to 29 may be orthogonal, in which case the device is of the normally black type.

Claims

1. Use of an active matrix light modulator for reducing the effects of asymmetrical optical performance, the active matrix light modulator comprising: a plurality of data lines (22); a plurality of scan lines (20); an active matrix of control elements (18) disposed at intersections of the data lines (22) and scan lines (20); an array (10) of pixels which are selectively addressable by data and scan signals applied to the control elements (18) by way of the data and scan lines (20,22) so as to be set to a first optical transmission state in response to a positive applied voltage of a particular magnitude, a second optical state in response to an intermediate applied voltage and a third optical state in response to a negative applied voltage of equal magnitude, but opposite polarity, to said positive applied voltage; addressing means (12,14) for addressing each pixel during a corresponding addressing frame by the application of data and scan signals to an associated one of the control elements (18) in order to select the optical level of the pixel for each frame; and voltage inversion means (12,14,28) for controlling the voltage applied to each pixel during successive subframes of each frame such that, when one optical level is selected for the frame, said positive voltage is applied to the pixel during one subframe of the frame and said negative voltage is applied to the pixel during another subframe of the frame and, when another optical level is selected for the frame, said intermediate voltage is applied to the pixel during both of the subframes of the frame, so as to provide DC balancing within the frame.

2. Use according to claim 1, characterised in that said intermediate applied voltage is zero voltage.

3. Use according to claim 1 or 2, characterised in that the first and third optical states are symmetrical in that they exhibit substantially the same optical level in response to said positive and negative applied voltages, and the voltage inversion means (12,14,28) is arranged to apply said positive and negative voltages to the pixel during the two successive subframes when said one optical level is selected such that the same optical level is obtained during the two subframes.

4. Use according to claim 1 or 2, characterised in that the first and third optical states are asymmetrical in that they exhibit different optical levels in response to said positive and negative applied voltages, and the voltage inversion means (12,14,28) is arranged to apply said positive and negative voltages to the pixel during the two successive subframes when said one optical level is selected such that different optical levels are obtained during the two subframes.

5. Use according to any preceding claim, characterised in that the voltage inversion means (12,14,28) is arranged to modulate addressing of each pixel by the addressing means by means (12,14) of a voltage inversion switching waveform having 2N portions for addressing 2N subframes within the frame, where N is an integer greater than zero and consecutive portions have voltages of equal magnitude and duration but opposite polarity.

6. Use according to claim 5, characterised in that the voltage inversion means (12,14,28) is arranged to supply a voltage inversion switching waveform consisting of two portions having voltages of equal magnitude and duration but opposite polarity which follow one another substantially immediately.

7. Use according to claim 5, characterised in that the voltage inversion means (12,14,28) is arranged to supply a voltage inversion switching waveform comprising portions having voltages of equal magnitude and duration but opposite polarity and a further portion of zero voltage.

8. Use according to claim 5, 6 or 7, characterised in that the voltage inversion means (12,14,28) is arranged to supply voltage inversion switching waveforms in successive frames such that the polarity of the last subframe of a first of the frames is the same as the polarity of the first subframe of a second of the frames following the first frame.

9. Use according to any preceding claim, characterised in that each of the pixels is addressable so as to be set to one of a plurality of first optical states in response to a selected one of a plurality of different positive applied voltages or one of a plurality of third optical states in response to a selected one of a plurality of different negative applied voltages, and the voltage inversion means (12,14,28) is arranged to apply said selected positive voltage to the pixel during one subframe of the frame and said selected negative voltage to the pixel during another subframe of the frame in order to select one of a plurality of possible optical levels for the frame whilst maintaining DC balancing within the frame.

10. Use according to any preceding claim, characterised in that the control elements (18) are polysilicon switching elements.

11. Use according to claim 10, characterised in that the polysilicon switching elements (18) are polysilicon thin film transistors or diodes.

12. Use according to any preceding claim, characterised in that the active matrix incorporates a respective control element (18) coupled to each pixel and having a data input for receiving data signals from a corresponding one of the data lines (22) and a control input for receiving scan pulses from a corresponding one of the scan lines (20) in order to switch the control element (18) to supply a voltage to the pixel.

13. Use according to claim 12, characterised in that a storage capacitor (24) is coupled to the output of the control element (18), and a buffer (28) is connected between the output of the control element (18) and the pixel.

14. Use according to any preceding claim, characterised in that the light modulator is a light transmissive liquid crystal device.

15. Use according to claim 14, characterised in that the array (10,44-46) is disposed between polarisers (47,48) arranged with their axes transverse to one another such that said first and third optical states are bright states and said second optical state is a dark state.

16. Use according to claim 14, characterised in that the array (10, 40-46) is disposed between polarisers (47,48) arranged with their axes substantially parallel to one another such that said first and third optical states are dark states and said second optical state is a bright state.

17. Use according to claim 14, characterised in that the array (10, 40-46) is disposed in series with a further array(10, 40'-45') of similar form between polarisers (47,48) arranged with their axes substantially parallel to one another, and the addressing means (12,14) is arranged to simultaneously apply addressing signals of opposite polarity to the arrays (10,40-46, 40'-45')) such that a dark level is obtained when one of the arrays (10,40-46) is in said first optical state and the other array (10,40'-45') is in said third optical state and a bright level is obtained when both arrays (10,40-46, 40'-45') are in said second optical state.

18. Use according to claim 14, characterised in that the array (10,40-42, 45,46)) is disposed between a polariser (47) and a reflective surface (44) with a quarter wave retarder (53) being disposed between the array (10,40-42,45,46) and the reflective surface (44) such that a dark level is obtained when the array (10,40-42,45,46) is in one of said first and third optical states and a bright level is obtained when the array (10,40-42,45,46) is in said second optical state.

19. Use according to any preceding claim, characterised in that the light modulator is a diffractive spatial light modulator.

20. Use according to claim 19, characterised in that the active matrix incorporates a set of first elongate electrodes (19) on one side of the array (10), a set of second elongate electrodes (21) interdigitated with the set of first elongate electrodes (19) on said one side of the array (10), and a set of pixel electrodes (17) on the other side of the array (10) each of which overlaps a plurality of first and second electrodes (19,21), the first and second electrodes (19,21) being connected to respective supply lines (19',21') for continuously applied voltages and each of the pixel electrodes (17) being addressable by the addressing means (12,14) for switching between a diffractive mode and a non-diffractive mode, wherein the voltage inversion means (12,14) is arranged to invert the voltages applied to the first and second electrodes (19,21) about a predetermined voltage between the two subframes at the same time as inversion of the voltages applied to the pixel electrodes (17).

21. Use according to any one of claims 1 to 20, characterised in that the light modulator is an antiferroelectric liquid crystal device.

22. Use according to claim 21, characterised in that the light modulator is a thresholdless antiferroelectric liquid crystal device.

23. Use according to any one of claims 1 to 20, characterised in that the light modulator is a deformed helix ferroelectric liquid crystal device.

24. Use according to any one of claims 1 to 20, characterised in that the light modulator is a short pitch bistable ferroelectric liquid crystal device.

25. Use of an active matrix light modulator for reducing the effects of asymmetrical optical performance, the modulator comprising a plurality of pixels, an active matrix addressing arrangement (16-28) for the pixels, and a pixel waveform generator (12,14) for supplying each frame of image data as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe.

26. An active light modulator comprising: a plurality of

data lines (22); a plurality of scan lines (20); an active matrix of control elements (18) disposed at intersections of the data lines (22) and scan lines (20); an array (10) of pixels which are selectively addressable by data and scan signals applied to the control elements (18) by way of the data and scan lines (20,22) so as to be set to a first optical transmission state in response to a positive applied voltage of a particular magnitude, a second optical state in response to an intermediate applied voltage and a third optical state in response to a negative applied voltage of equal magnitude, but opposite polarity, to said positive applied voltage; and addressing means (12,14) for addressing each pixel during a corresponding addressing frame by the application of data and scan signals to an associated one of the control elements (18) in order to select the optical level of the pixel for each frame, characterised in that the pixels exhibit asymmetrical on-axis optical performance and in that the modulator comprises voltage inversion means (12,14,28) for controlling the voltage applied to each pixel during successive subframes of each frame such that, when one optical level is selected for the frame, said positive voltage is applied to the pixel during one subframe of the frame and said negative voltage is applied to the pixel during another subframe of the frame and, when another optical level is selected from the frame, said intermediate voltage is applied to the pixel during both of the subframes of the frame, so as to provide DC balancing within the frame.

27. A light modulator according to claim 26, characterised in that said intermediate applied voltage is zero voltage.

28. A light modulator according to claim 26 or 27, characterised in that the first and third optical states are asymmetrical in that they exhibit different optical levels in response to said positive and negative applied voltages, and the voltage inversion means (12,14,28) is arranged to apply said positive and negative voltages to the pixel during the two successive subframes when said one optical level is selected such that different optical levels are obtained during the two subframes.

29. A light modulator according to 26, 27 or 28, characterised in that the voltage inversion means (12,14,28) is arranged to modulate addressing of each pixel by the addressing means (12,14) by means of a voltage inversion switching waveform having 2N portions for addressing 2N subframes within the frame, where N is an integer greater than zero and consecutive portions have voltages of equal magnitude and duration but opposite polarity.

30. A light modulator according to claim 29, characterised in that the voltage inversion means (12,14,28) is arranged to supply a voltage inversion switching waveform consisting of two portions having voltages of equal magnitude and duration but opposite polarity which follow one another substantially immediately.

31. A light modulator according to claim 29, characterised in that the voltage inversion means (12,14,28) is arranged to supply a voltage inversion switching waveform comprising portions having voltages of equal magnitude and duration but opposite polarity and a further portion of zero voltage.

32. A light modulator according to claim 29, 30 or 31, characterised in that the voltage inversion means (12,14,28) is arranged to supply voltage inversion switching waveforms in successive frames such that the polarity of the last subframe of a first of the frames is the same as the polarity of the first subframe of a second of the frames following the first frame.

33. A light modulator according to any one of claims 26 to 32, characterised in that each of the pixels is addressable so as to be set to one of a plurality of first optical states in response to a selected one of plurality of a different positive applied voltages or one of a plurality of third optical states in response to a selected one of a plurality of different negative applied voltages, and the voltage inversion means (12,14,28) is arranged to apply said selected positive voltage to the pixel during one subframe of the frame and said selected negative voltage to the pixel during another subframe of the frame in order to select one of plurality of possible optical levels for the frame whilst maintaining DC balancing within the frame.

34. A light modulator according to any one of claims 26 to 33, characterised in that the control elements (18) are polysilicon switching elements.

35. A light modulator according to claim 34, characterised in that the polysilicon switching elements (18) are polysilicon thin film transistors or diodes.

36. A light modulator according to any one of claims 26 to 35, characterised in that the active matrix incorporates a respective control element (18) coupled to each pixel and having a data input for receiving data signals from a corresponding one of the data lines (22) and a control input for receiving scan pulses from a corresponding one of the scan lines (20) in order to switch the control element (18) to supply a voltage to the pixel.

37. A light modulator according to claim 36, characterised in that a storage capacitor (24) is coupled to the output of the control element (18) and a buffer (28) is connected between the output of the control element (18) and the pixel.

38. A light modulator according to any one of claim 26 to 37, characterised in that the modulator is a light transmissive liquid crystal device.

39. A light modulator according to claim 38, characterised in that the array (10,40-46) is disposed between polarisers (47,48)arranged with their axes transverse to one another such that said first and third optical states are bright states and said second optical state is a dark state.

40. A light modulator according to claim 38, characterised in that the array (10,40-46) is disposed between polarisers (47,48) arranged with their axes substantially parallel to one another such that said first and third optical states are dark states and said second optical state is a bright state.

41. A light modulator according to claim 38, characterised in that the array (10,40-46) is disposed in series with a further array (20,40'-45') of similar form between polarisers (47,48)arranged with their axes substantially parallel to one another, and the addressing means (12,14) is arranged to simultaneously apply addressing signals of opposite polarity to the arrays (10,40-46,40'-45') such that a dark level is obtained when one of the arrays (10,40-46) is in said first optical state and the other array (10,40'-45') is in said third optical state and a bright level is obtained when both arrays (10,40-46,40'-45') are in said second optical state.

42. A light modulator according to claim 38, characterised in that the array (10,40-46) is disposed between a polariser (47) and a reflective surface (44) with a quarter wave retarder (53) being disposed between the array (10,40-46) and the reflective surface (44) such that a dark level is obtained when the array (10,40-46) is in one of said first and third optical states and a bright level is obtained when the array (10,40-46) is in said second optical state.

43. A light modulator according to any one of claims 26 to 42, characterised in that the modulator is a diffractive spatial light modulator.

44. A light modulator according to claim 43, characterised in that the active matrix incorporates a set of first elongate electrodes (19) on one side of the array (10), a set of second elongate electrodes (21) interdigitated with the set of first elongate electrodes (19) on said one side of the array (10), and a set of pixel electrodes (17) on the other side of the array (10), each of which overlaps a plurality of first and second electrodes (19,21); the first and second electrodes (19,21) being connected to respective supply lines (19',21') for continuously applied voltages and each of the pixel electrodes (17) being addressable by the addressing means (12,14) for switching between a diffractive mode and a non-diffractive mode, wherein the voltage inversion means (12,14) is arranged to invert the voltages applied to the first and second electrodes (19,21) about a predetermined voltage between the two subframes at the same time as inversion of the voltages applied to the pixel electrodes (17).

45. A light modulator according to any one of claims 26 to 44, characterised in that the modulator is an antiferroelectric liquid crystal device.

46. A light modulator according to claim 45, characterised in that the modulator is a thresholdless antiferroelectric liquid crystal device.

47. A light modulator according to any one of claims 26 to 44, characterised in that the modulator is a deformed helix ferroelectric liquid crystal device.

48. A light modulator according to any one of claims 26 to 44, characterised in that the modulator is a short pitch bistable ferroelectric liquid crystal device.

49. An active matrix spatial light modulator comprising a plurality of pixels, an active matrix addressing arrangement (16-28) for the pixels, and a pixel waveform generator (12,14), characterised in that the pixels exhibit asymmetrical on-axis optical performance and in that the pixel waveform generator (12,14) is arranged to supply each frame of image data as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe.

50. A display comprising: an active matrix spatial light modulator (30) comprising a plurality of pixels, an active matrix addressing arrangement (16-28) for the pixels, and a pixel waveform generator (12,14); and an illumination system (33,34), characterised in that the pixel waveform generator (12,14) is arranged to supply each frame of colour image data as a plurality of single colour frames of single colour image data and each single colour frame as first and second subframes such that the waveform across each pixel during the second subframe is substantially the inverse of the waveform across the pixel during the first subframe, and in that the illumination system (33,34) is arranged to illuminate the modulator (30) with light of a colour corresponding to the

colour of the colour image data currently being displayed by the modulator (30).

51. A display as claimed in claim 50, characterised in that the first and second subframes of each single colour frame are consecutive.

52. A display as claimed in claim 51, characterised in that the pixels exhibit symmetrical optical performance.

53. A display as claimed in claim 52, characterised in that the illumination system (33,34) is arranged to illuminate the modulator (30) continuously during the first and second subframes of each single colour frame.

54. A display as claimed in claim 53, characterised in that the illumination system (33,34) is arranged to begin illuminating the modulator (30) no earlier than completion of refreshing the modulator (30) with each first subframe and to stop illuminating the modulator (30) no later than commencement of refreshing the modulator (30) with the subsequent first subframe.

55. A display as claimed in claim 51, characterised in that the pixels exhibit asymmetrical optical performance.

56. A display as claimed in claim 50, characterised in that the first subframes of each frame are consecutive and the second subframes of each frame are consecutive.

57. A display as claimed in claim 55 or 56, characterised in that the illumination system (33,34) is arranged to be extinguished between consecutive subframes.

58. A display as claimed in claim 57, characterised in that the illumination system (33,34) is arranged to begin illuminating the modulator (30) no earlier than completion of refreshing the modulator (30) with each subframe and to stop illuminating the modulator (30) no later than commencement of refreshing the modulator (30) with the subsequent subframe.

59. A display as claimed in any one of claims 50 to 58, characterised in that the single colour frames comprise red, green and blue colour frames.

60. A display as claimed in any one of claims 50 to 59, characterised in that the modulator (30) comprises a liquid crystal device.

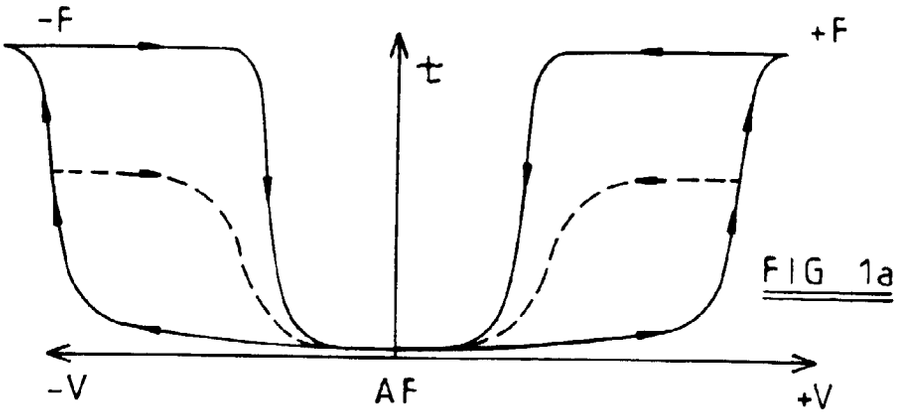


FIG 1a

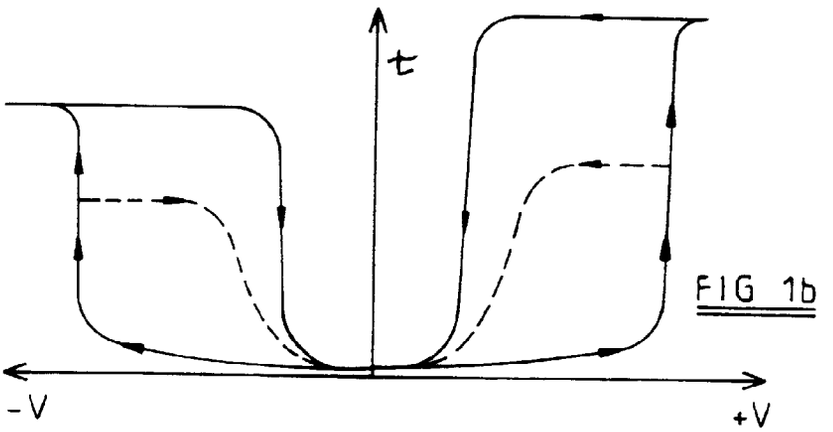


FIG 1b

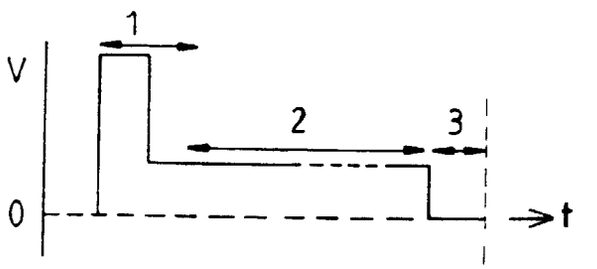


FIG 2a

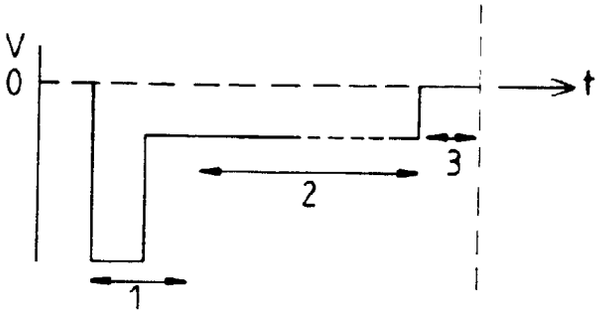


FIG 2b

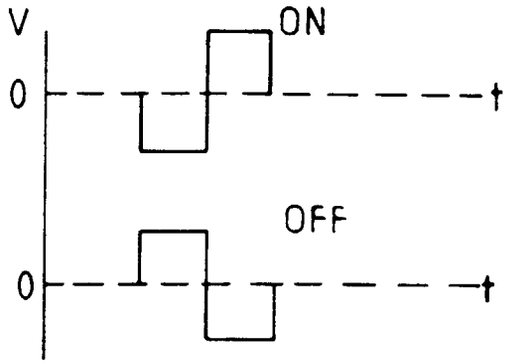


FIG 3a

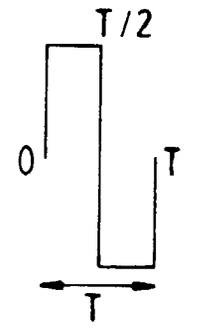
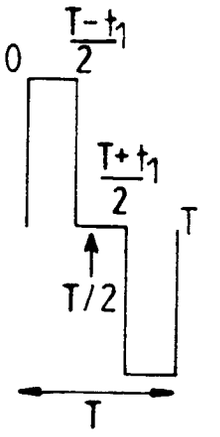


FIG 3b



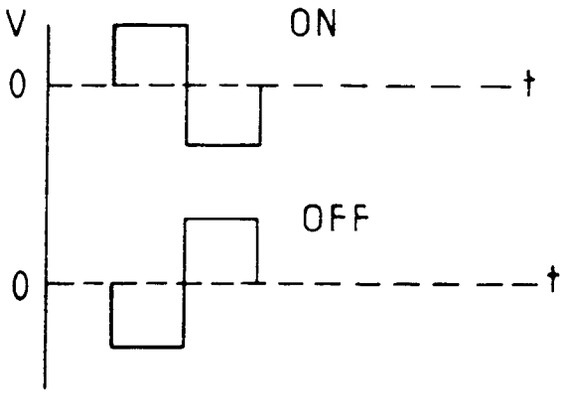


FIG 4a

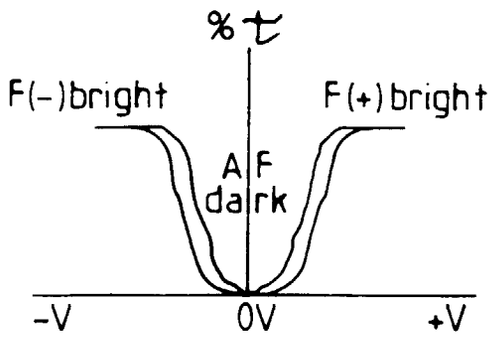


FIG 4b

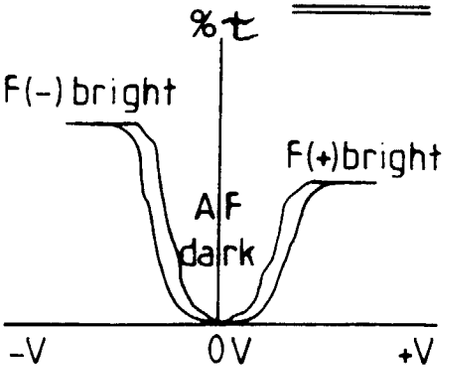


FIG 5

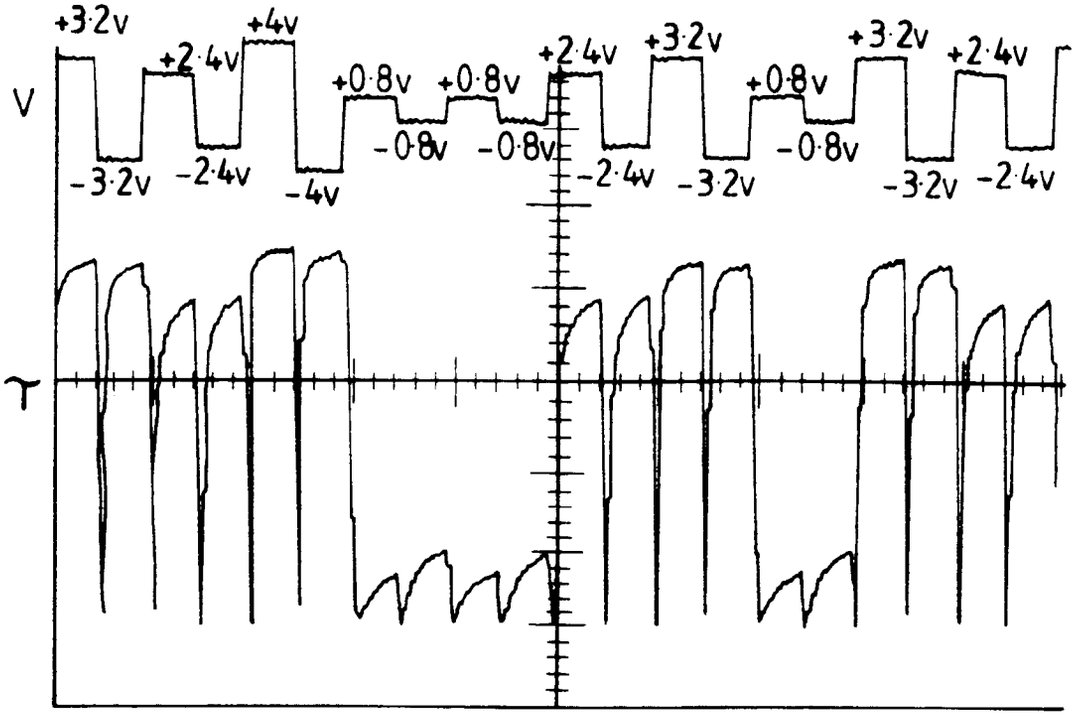
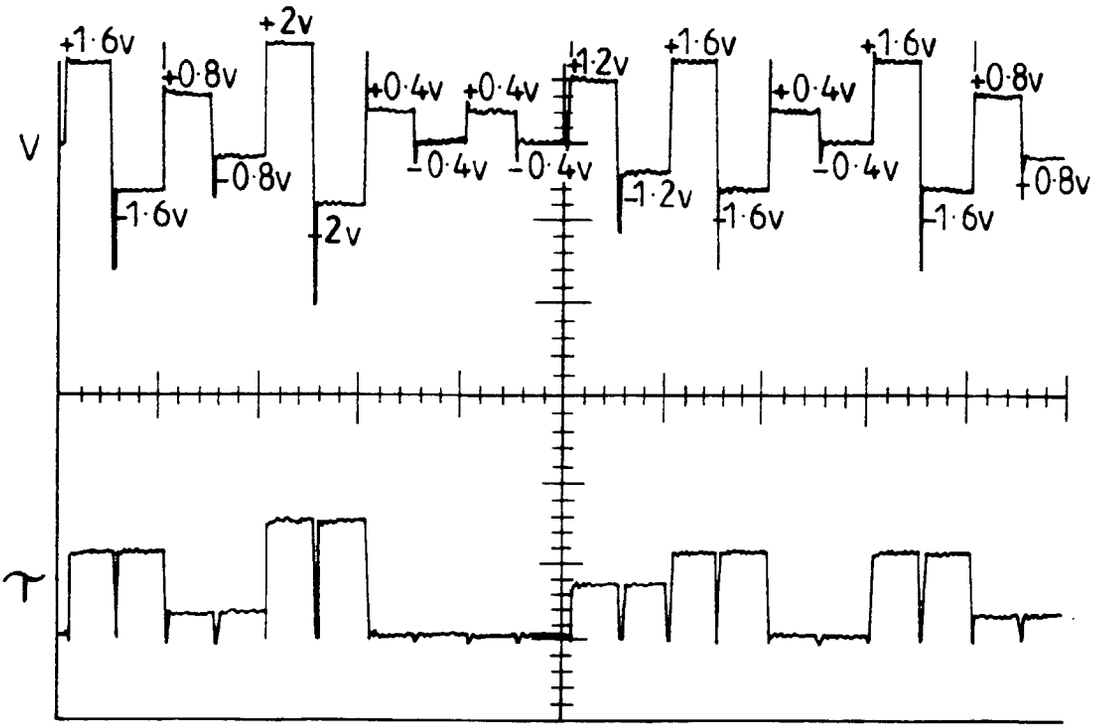

+3·2v
+2·4v
+4v
+0·8v
+0·8v
+2·4v
+3·2v
+0·8v
+3·2v
+2·4v
-3·2v
-2·4v
-4v
-0·8v
-0·8v
-2·4v
-3·2v
-0·8v
-3·2v
-2·4v
V
T

FIG 6


+1·6v
+0·8v
+2v
+0·4v
+0·4v
+1·2v
+1·6v
+0·4v
+1·6v
+0·8v
-1·6v
-0·8v
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-0·4v
-1·6v
-0·8v
V
T

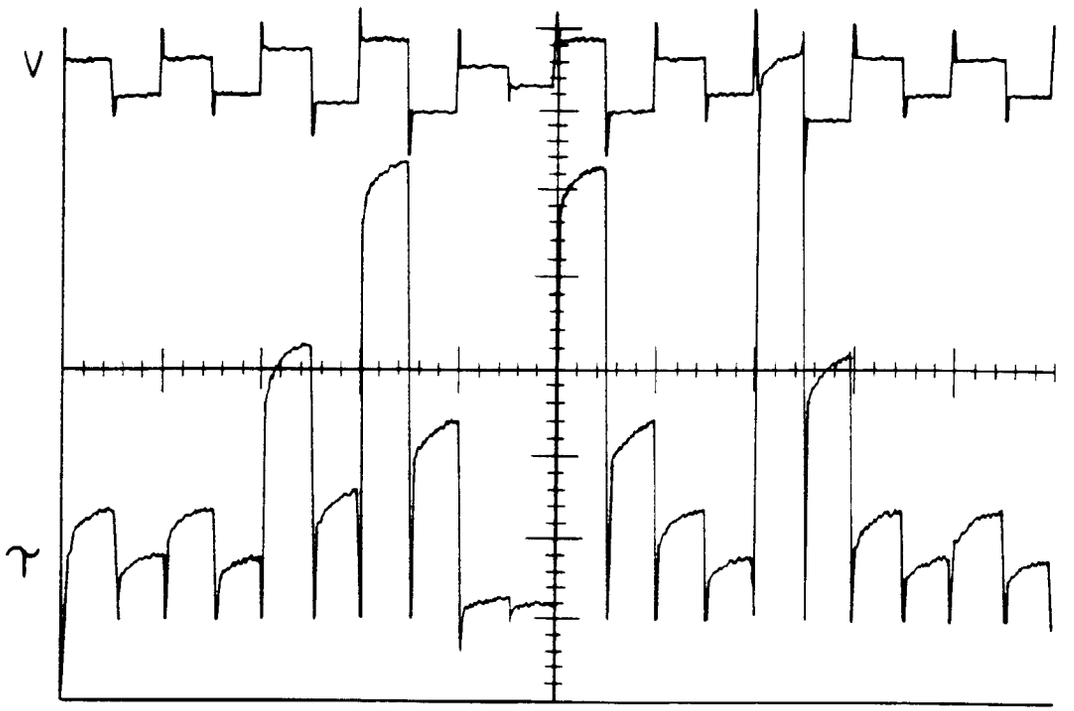


FIG 7

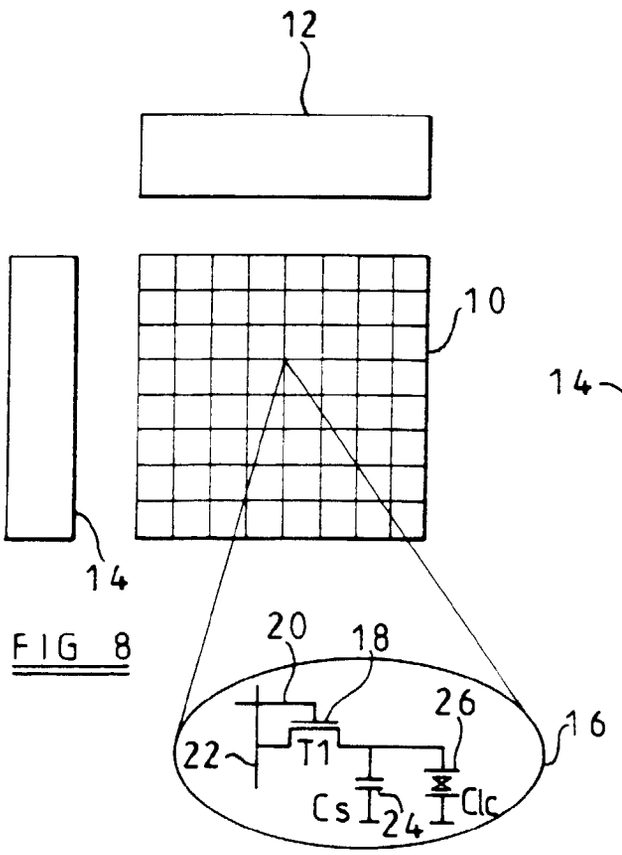


FIG 8

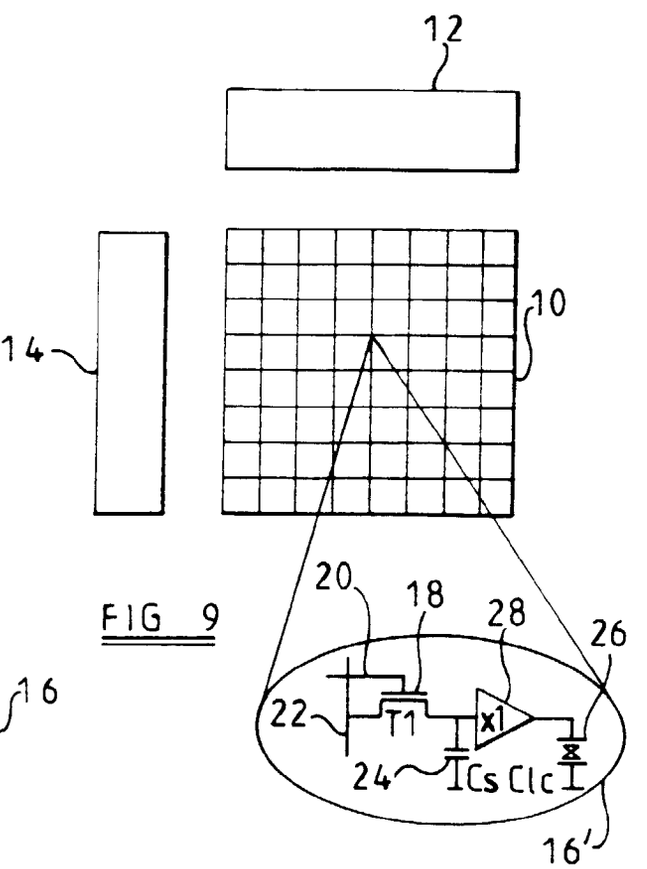


FIG 9

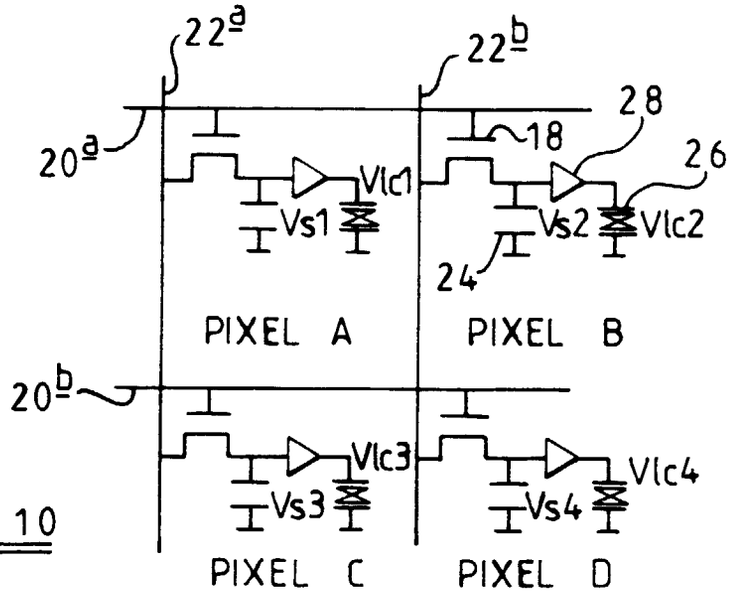
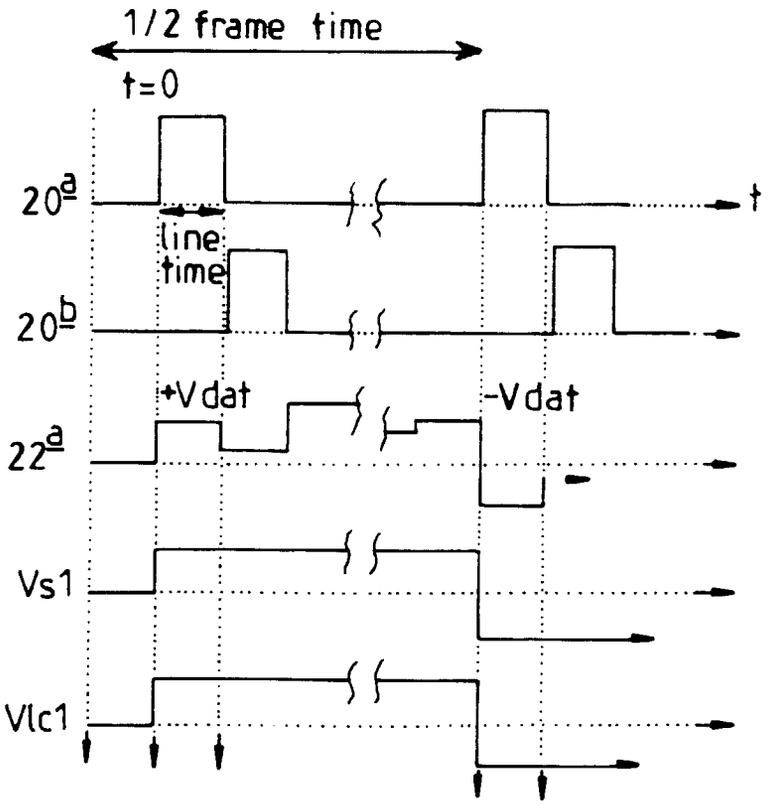

22a
22b
28
18
20a
Vlc1
26
Vs1
Vs2
Vlc2
24
PIXEL A
PIXEL B
20b
Vlc3
Vlc4
Vs3
Vs4
PIXEL C
PIXEL D

FIG 10

FIG 11


1/2 frame time
t=0
20a
t
line time
20b
+Vdat
-Vdat
22a
Vs1
Vlc1

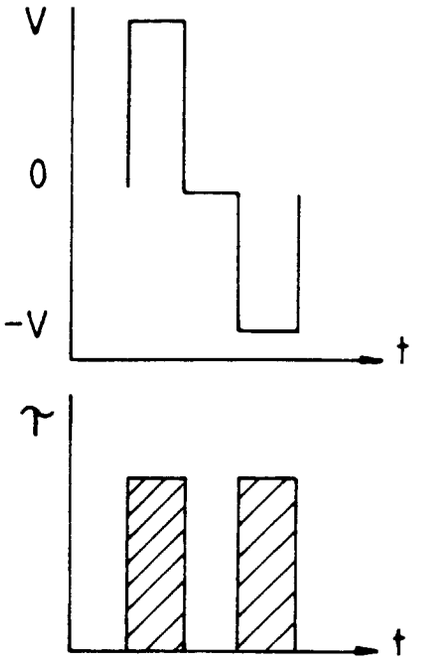


FIG 12a

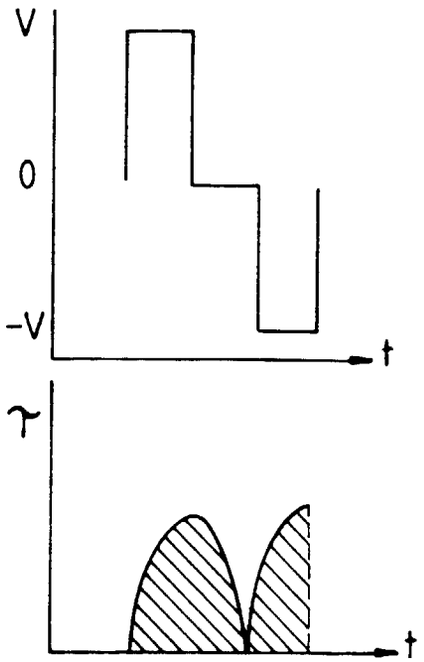


FIG 12b

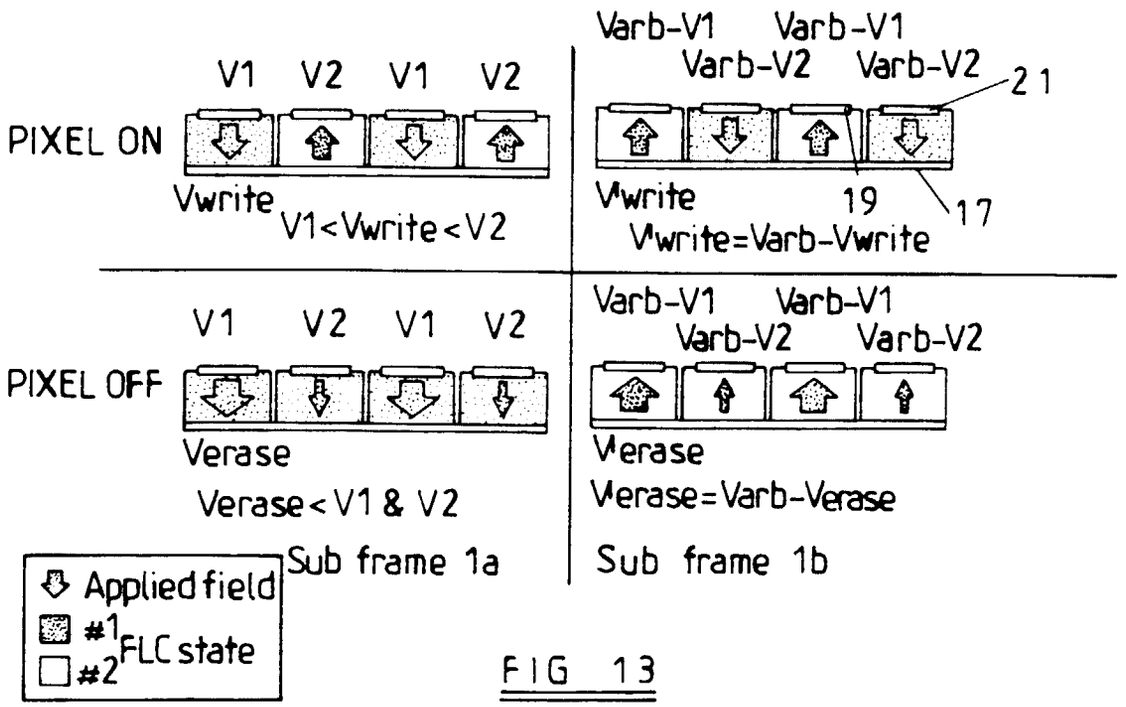


FIG 13

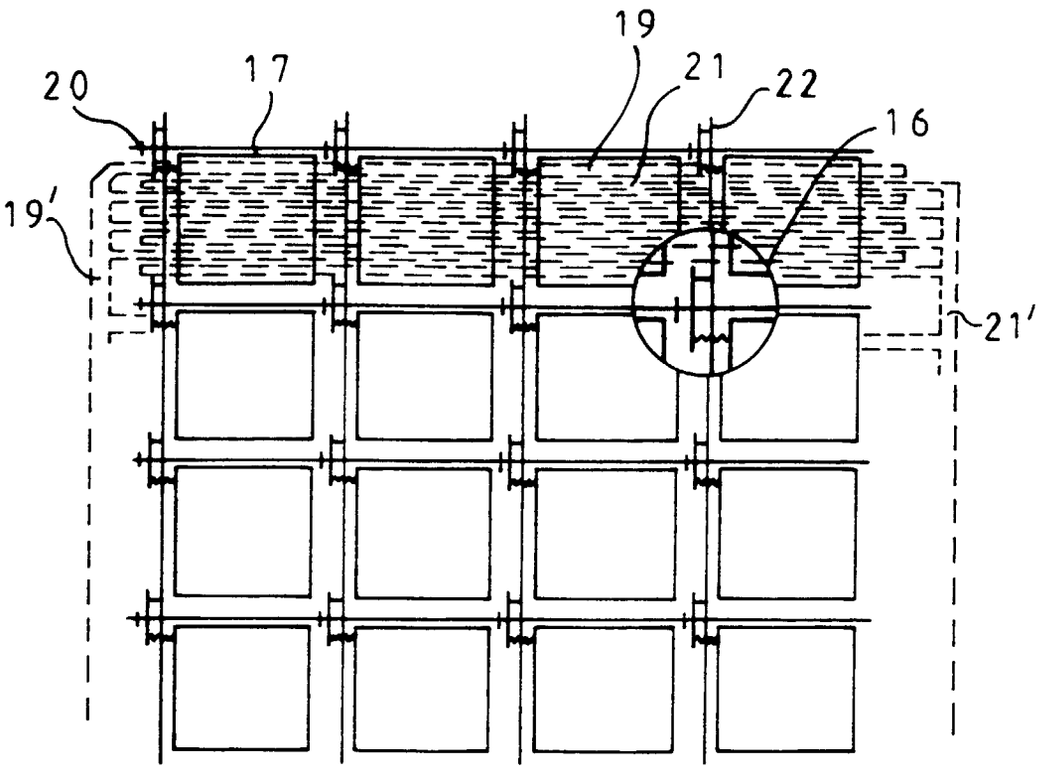


FIG 14

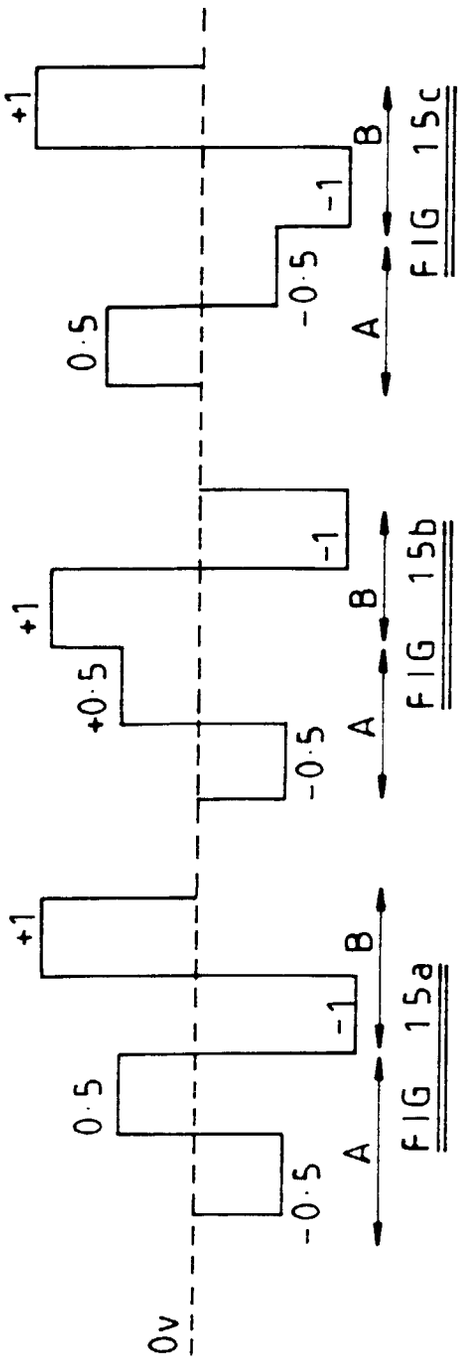


FIG 15a

FIG 15b

FIG 15c

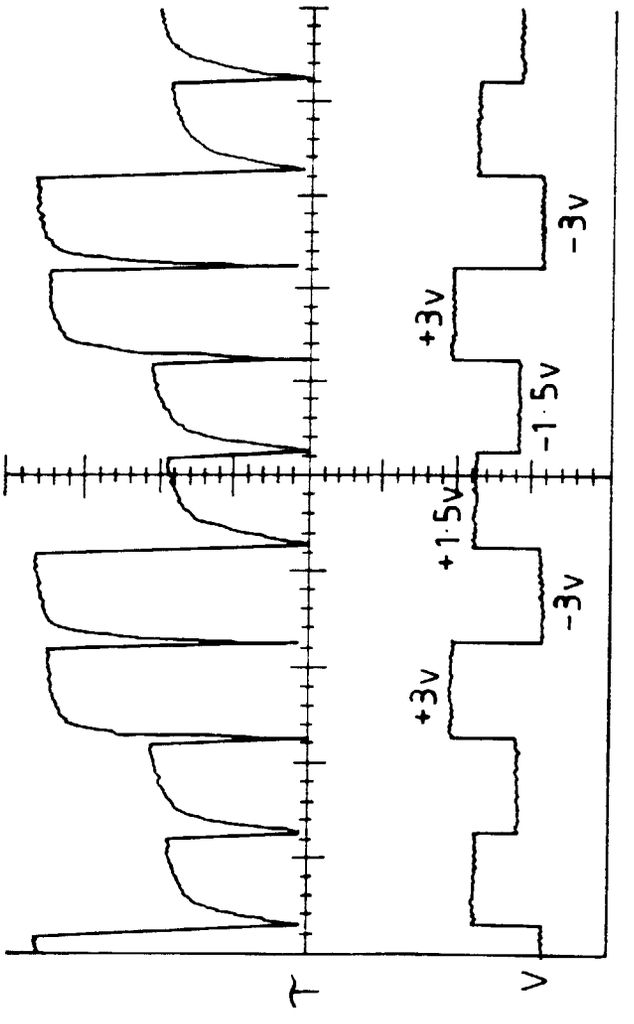


FIG 16

FIG 17

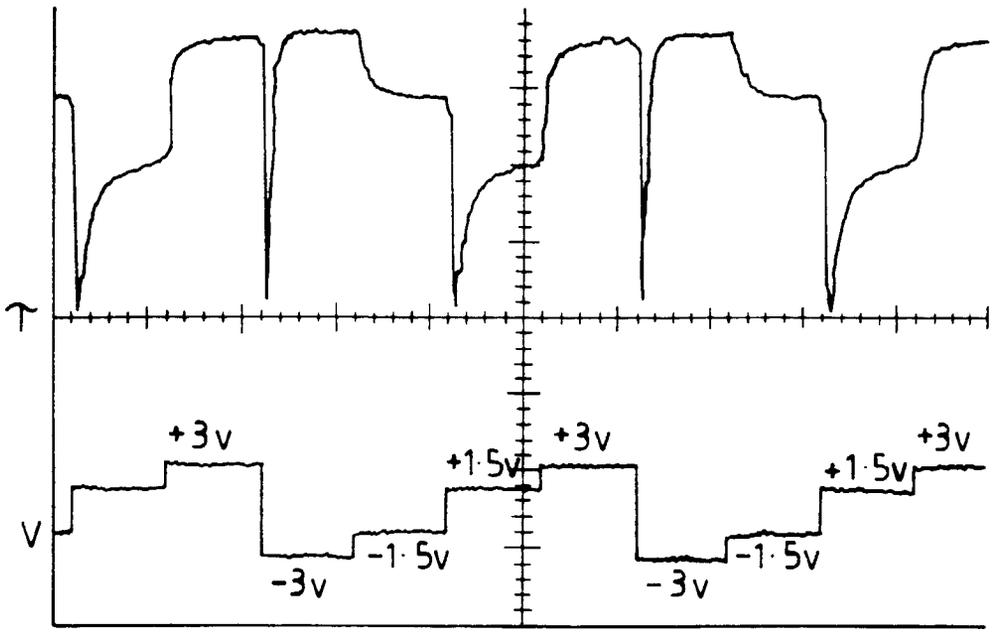
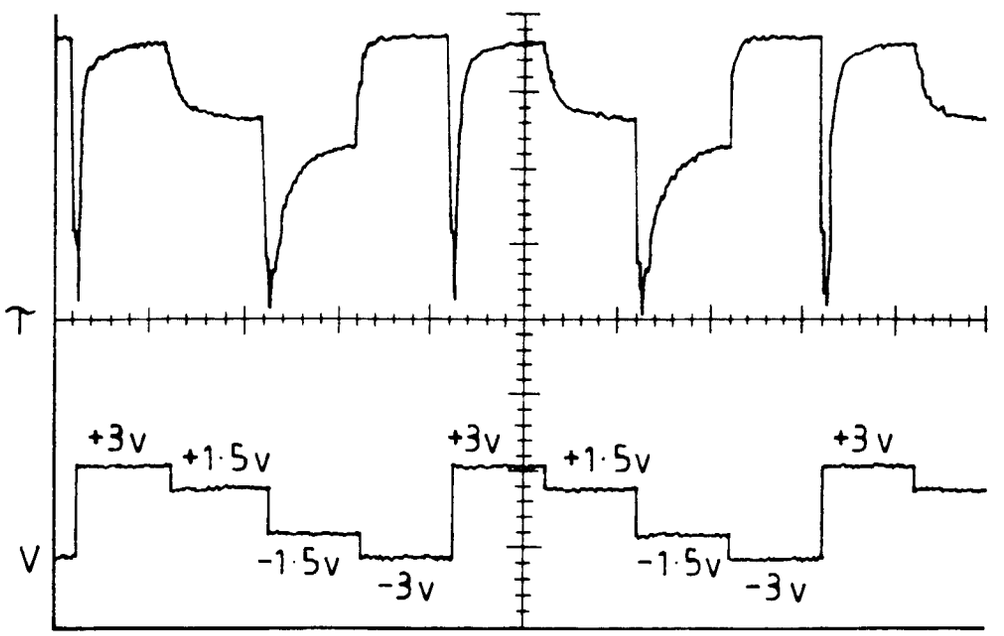


FIG 18



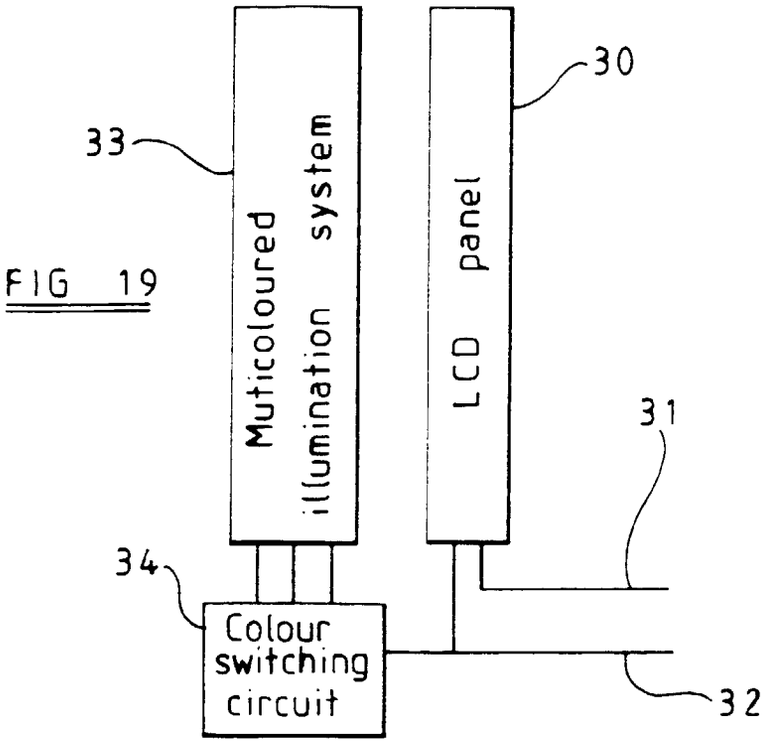

33
Muticoloured illumination system
LCD panel
30
31
34
Colour switching circuit
32

FIG 19

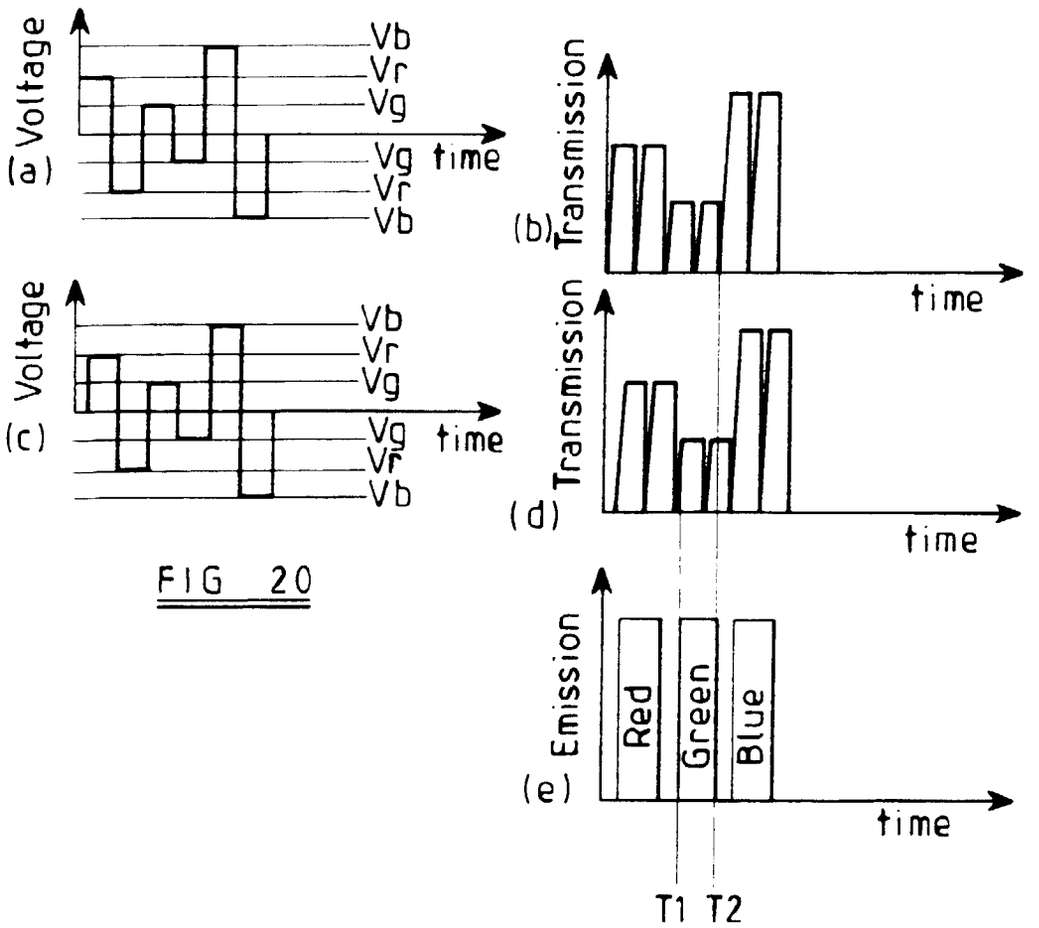

(a) Voltage
Vb
Vr
Vg
Vg
Vr
Vb
time
(b) Transmission
time
(c) Voltage
Vb
Vr
Vg
Vg
Vr
Vb
time
(d) Transmission
time
(e) Emission
Red
Green
Blue
time
T1 T2

FIG 20

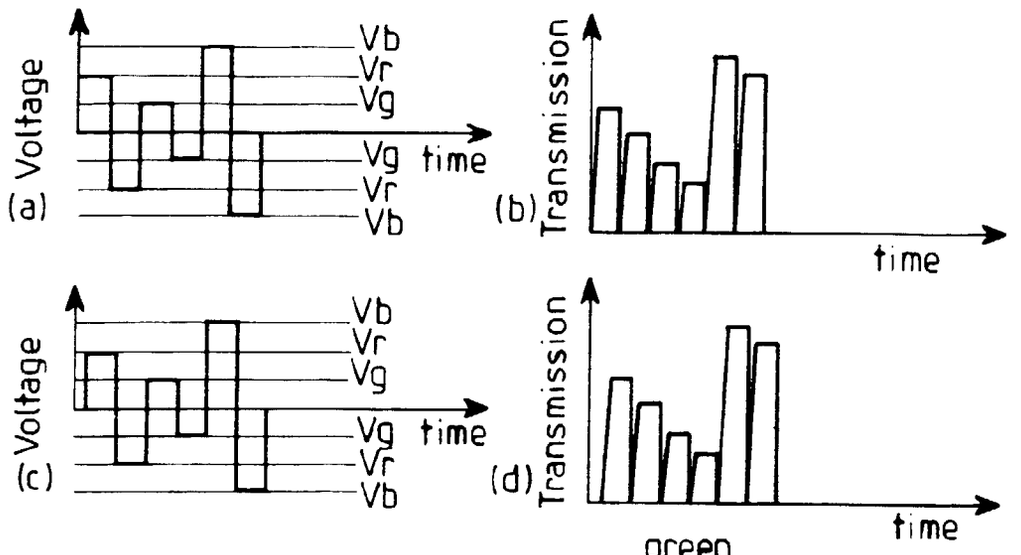
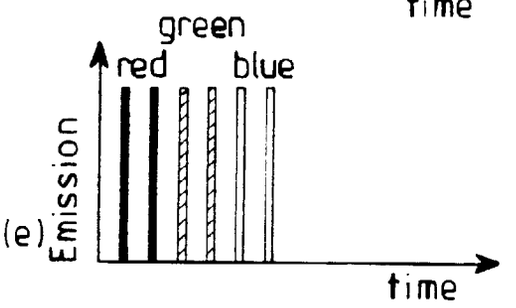

Voltage
Vb
Vr
Vg
time
Vg
Vr
Vb
(a)
Transmission
(b)
time
Voltage
Vb
Vr
Vg
time
Vg
Vr
Vb
(c)
Transmission
(d)
time

FIG 21


green
red
blue
Emission
(e)
time

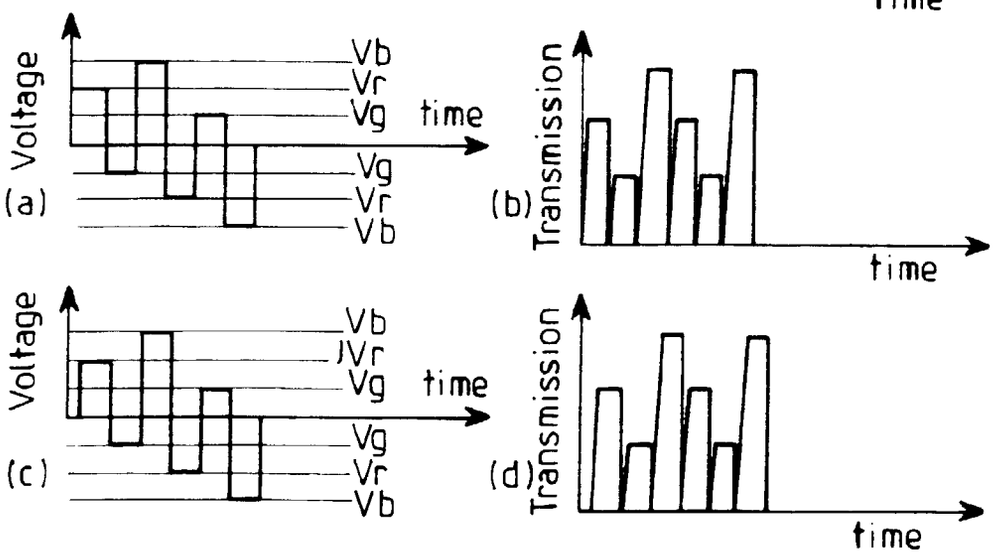
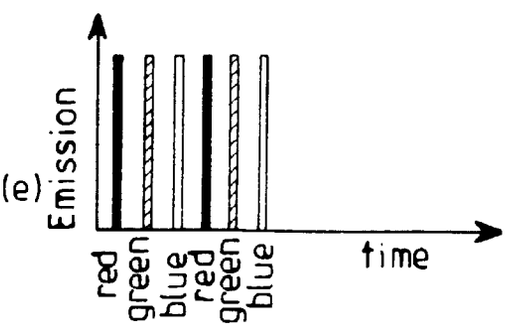

Voltage
Vb
Vr
Vg
time
Vg
Vr
Vb
(a)
Transmission
(b)
time
Voltage
Vb
Vr
Vg
time
Vg
Vr
Vb
(c)
Transmission
(d)
time

FIG 22


Emission
(e)
red
green
blue
red
green
blue
time

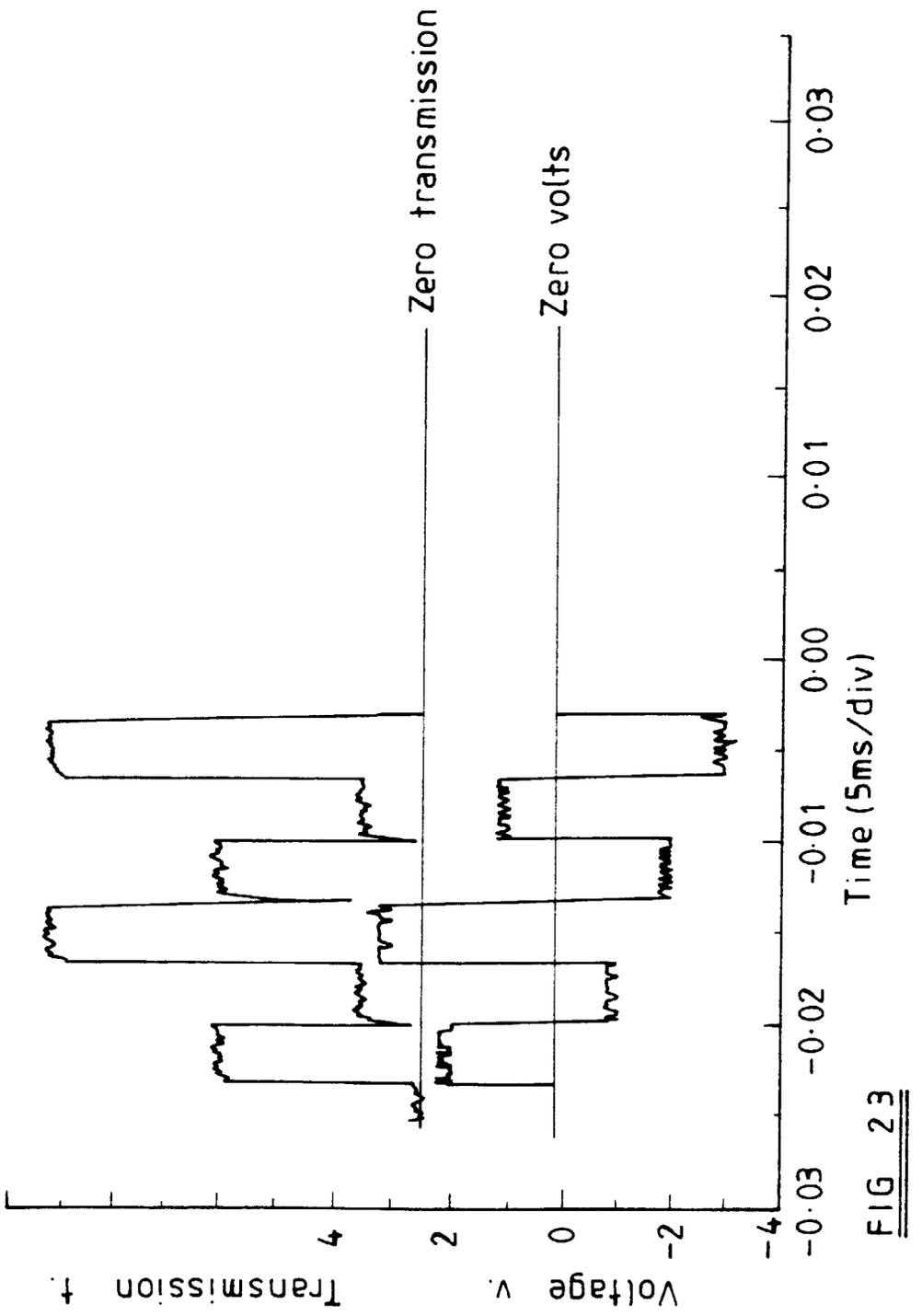

Zero transmission
Zero volts
Transmission t.
Voltage v.
4
2
0
-2
-4
-0·03
-0·02
-0·01
0·00
0·01
0·02
0·03
Time (5ms/div)

FIG 23

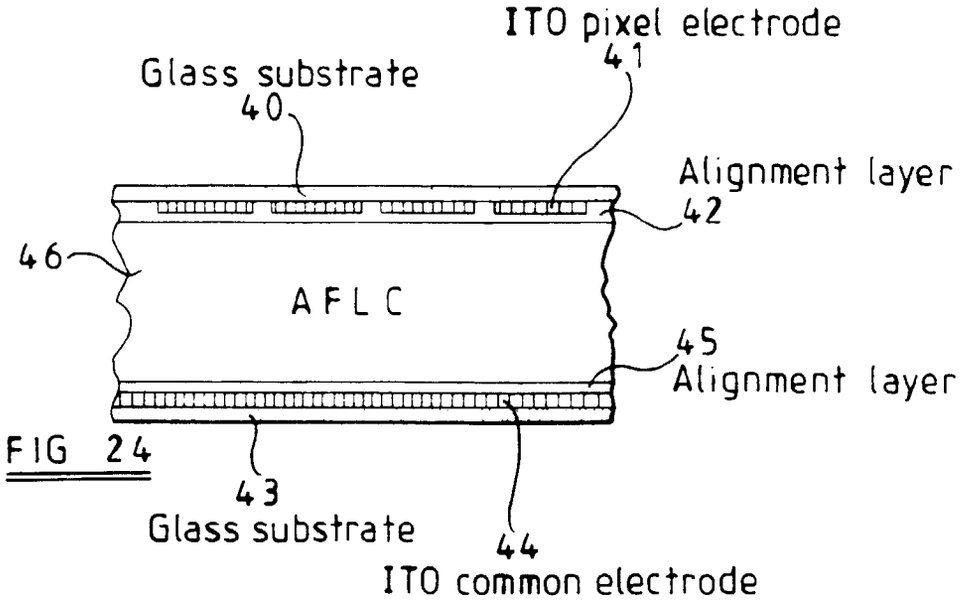


FIG 24

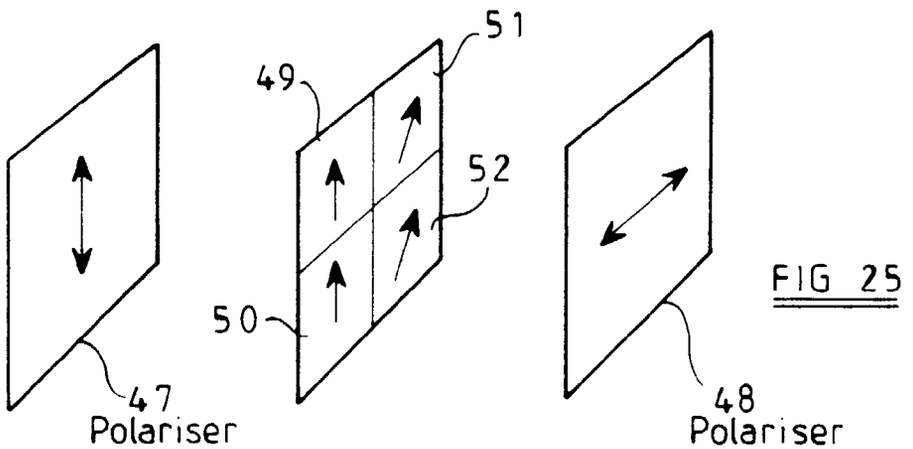


FIG 25

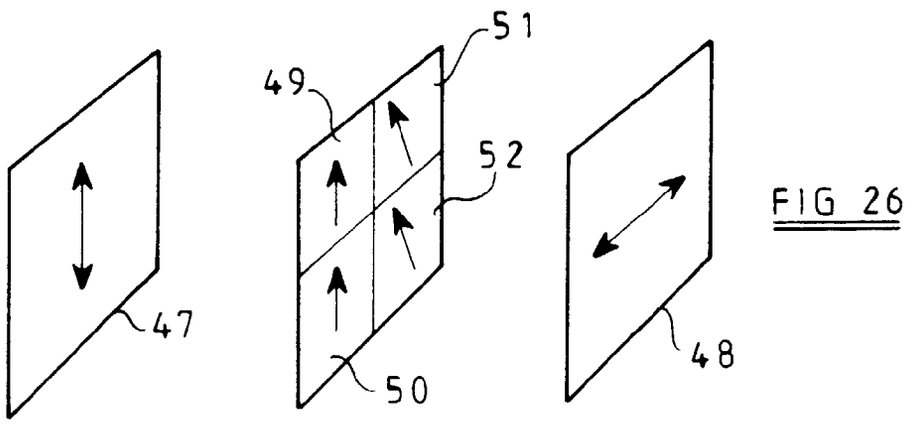


FIG 26

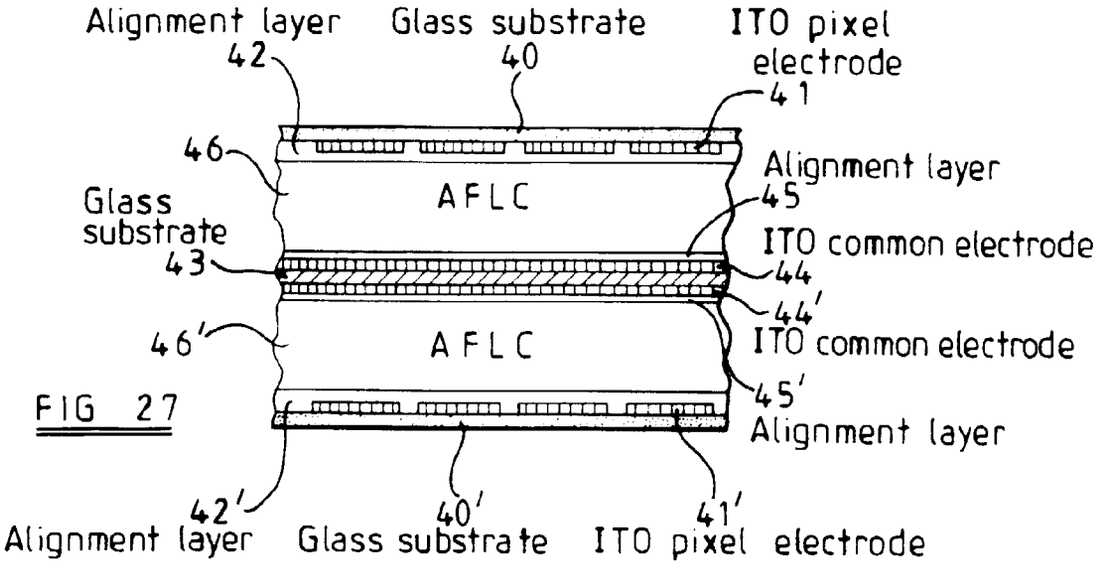


FIG 27

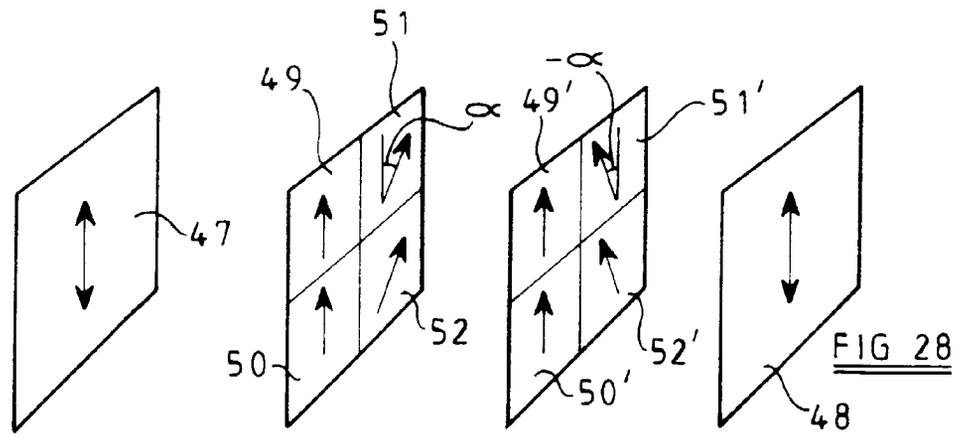


FIG 28

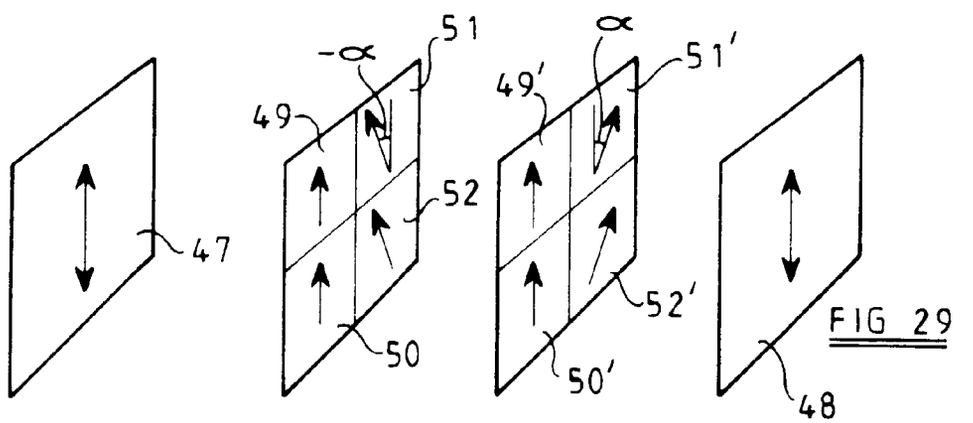


FIG 29

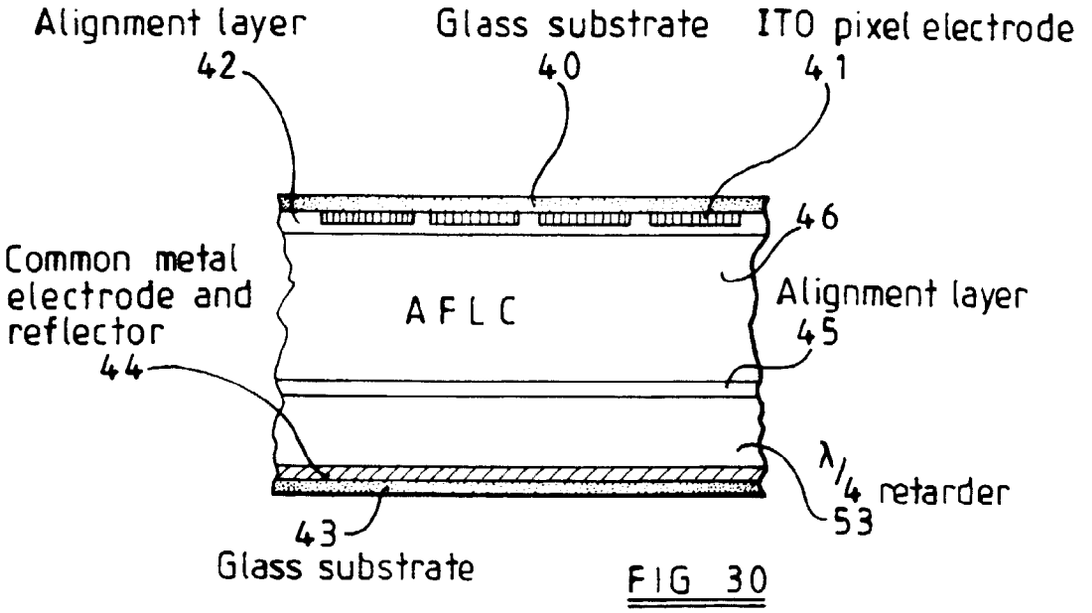


FIG 30

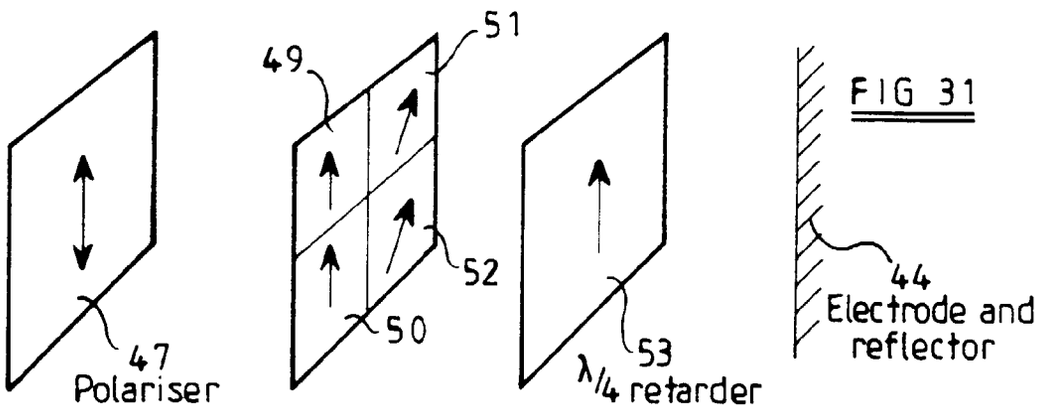


FIG 31

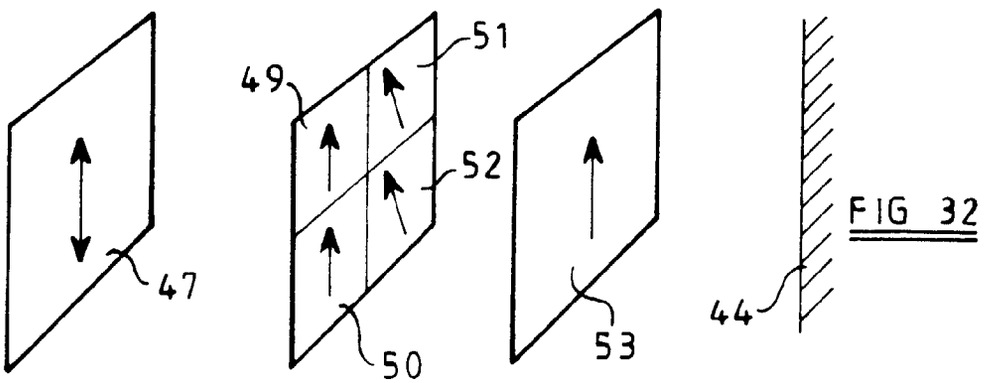


FIG 32