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(54) Stripline transition device

(57) An electronic circuit for transmitting high frequency signals, in particular ultrahigh frequency signals, comprises a first circuit part comprising: a first waveguide including a first electrode, a first coplanar strip line of a symmetrical configuration and including two strip line electrodes, and a first active device having a control terminal and two output terminals connected to the first electrode and to the two strip line electrodes respectively, a second circuit part comprising: a second coplanar strip line of a symmetrical configuration and including two strip line electrodes, a second waveguide including a second electrode, and a second active device having two control terminals and an output terminal, connected to the strip line electrodes and to the second electrode, respectively.

The first circuit part and the second circuit part are connected in a cascade configuration in which the first circuit part constitutes an input part or alternatively connected in a cascade configuration in which the second circuit part constitutes an input part.

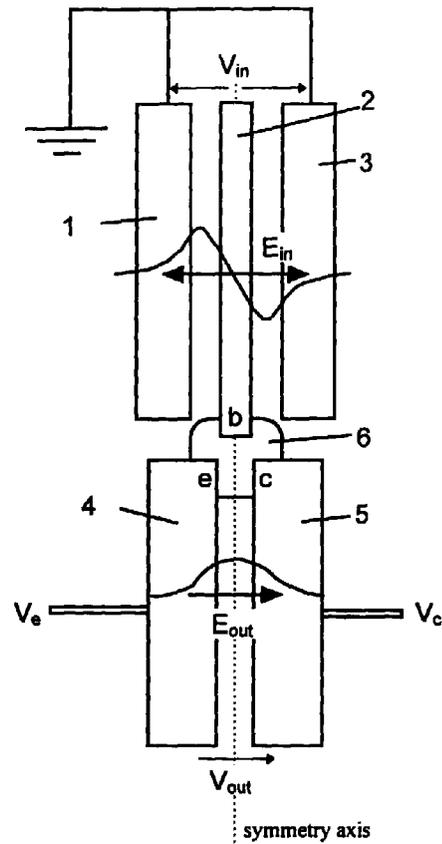


Figure 1

**Description****Field of the invention**

The present invention relates to the field of signal transmission circuits or electrical or electronic circuits, and in particular to high frequency transmission circuits, such as ultrahigh frequency transmission circuits.

**Background of the invention**

Signal-transmitting circuits or electrical circuits for transmitting highfrequency signals, in particular ultrahigh frequency signals, have gained an increasing importance within the electronic industry, in particular within the analog and digital signal transmission field. Numerous applications of high frequency transmission circuits, such as computer technology, including ultrafast computers, fiber interfaces, including optic fiber multiplexers and optic fiber demultiplexers, and ultrafast communication applications, etc.

Coplanar transmission lines exhibit superior properties for a low loss, high speed connection of devices operating in the frequency regime of 1 GHz to 1 THz. Technically, planar devices can be easily integrated in coplanar transmission lines. With decreasing device sizes, contact distances become smaller and parasitic capacitances,  $C_p$ , become larger. Together with the increasing operating frequency, the parasitic impedance  $1/\omega C_p$  ( $\sim 100 \Omega$ ) becomes smaller than the output impedance of the active device. The output impedance for dc signals of fast transistors is typically  $1k\Omega$ . In this case  $C_p$  forms a short over the device and the input signal can be measured almost unattenuated at the output.

This problem has been acknowledged by several groups measuring ultrafast device responses. In a recent publication by Ogawa et al. [Applied Physics Letters, Vol. 66, p. 1228 (1995)] this problem is directly addressed and the gate drain capacitance is measured to be 1.8 fF. Most of this capacitance is formed by the contacts and the intrinsic capacitance of the device itself is only 10 % of this value.

In principle a device response can be measured by subtracting the input signal from the output signal or by comparing output signals for different bias conditions. In all cases it was found that the output signal is only marginally affected (on the order of 10%) by the active device. Whereas this effect still might be sufficient to measure the device behavior, it means that this configuration cannot be used for circuits. The issue of cascading devices and hence building an ultra high speed circuit is unresolved. The described circuit design eliminates the signals due to this parasitic capacitive coupling.

From US patent No. 5,550,518, an active conversion circuit for conversion between microstrip and coplanar waveguide is known, to which US patent reference is made and which US patent is hereby incorpo-

rated in the present specification by reference.

**Summary of the invention**

A circuit design is provided for eliminating parasitic capacitive coupling across ultrahigh frequency devices. The signal due to parasitic coupling is eliminated by alternating between an even mode and an odd mode signal propagation. The even mode is supported by a coplanar strip line the odd mode by a coplanar waveguide. This design allows to cascade devices with micron or submicron contact distances operated at THz or near THz frequencies.

The present invention provides an electrical circuit in which the inherent parasitic capacitive coupling in prior art ultrahigh frequency signal transmission circuits is to a great extent eliminated or suppressed due to the cascading of even and odd mode signal parts or blocks.

A particular advantage of the present invention relates to a simple cascading of signal-transmitting elements or blocks each including an active device, such as an FET transistor or bipolar transistor providing within the individual signal-transmitting block or element a conversion from a two-wire transmission line into a waveguide, or vice versa, within the cascade of the individual alternating electric signal-transmitting blocks or elements.

The above feature and the above advantage together with numerous other features and advantages which will be evident from the below detailed description of advantageous embodiments of the present invention are according to the teachings of the present invention obtained by an electric circuit for transmitting high frequency signals, in particular ultrahigh frequency signals, comprising:

a first circuit part comprising:

a first waveguide means including a first electrode,

a first coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative to one another, and

a first active device having a control terminal and two output terminals, said control terminal of said first active device being connected to said first electrode of said first waveguide means, and said output terminals of said first active device being connected to said two strip line electrodes of said first coplanar strip line means,

a second circuit part comprising:

a second coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative

to one another,  
 a second waveguide means including a second electrode, and  
 a second active device having two control terminals and an output terminal, said control terminals of said second active device being connected to said strip line electrodes of said second coplanar strip line means, and said output terminal of said second active device being connected to said second electrode of said second waveguide means,

and said first circuit part and said second circuit part being connected in a cascade configuration in which said first circuit part constitutes an input part in which said first electrode of said first waveguide means constitutes an input electrode, in which said second circuit part constitutes an output part in which said second electrode of said second waveguide means constitutes an output electrode, and in which said two strip line electrodes of said first coplanar strip line means of said first circuit part also constitutes said two strip line electrodes of said second coplanar strip line of said second circuit part, or alternatively connected in a cascade configuration in which said second circuit part constitutes an input part in which said two strip line electrodes of said second coplanar strip line means of said second circuit part constitute two input electrodes in which said first circuit part constitutes an output part, in which said two strip line electrodes of said first coplanar strip line means of said first circuit part constitute two output electrodes, and in which said second electrode of said second waveguide means of said second circuit part also constitutes said first electrode of said first waveguide means of said first circuit part.

According to the basic realization of the present invention, a signal-transmitting circuit for transmitting high frequency signals, and in particular ultrahigh frequency signals, is produced through the cascading of alternating signal transmission converter blocks for converting from odd mode signal propagation into even mode signal propagation, and vice versa, or alternatively from even mode signal propagation into odd mode signal propagation, and vice versa.

According to the teachings of the present invention, the first waveguide means may be constituted by a first coplanar waveguide of a symmetrical configuration in which the first electrode constitutes a centre electrode and further including two ground electrodes arranged symmetrically relative to the electrode, and/or the second waveguide may be constituted by a second coplanar waveguide of a symmetrical configuration in which the first electrode constitutes a centre electrode and further including two ground electrodes arranged symmetrically relative to the centre electrode.

According to the teachings of the present invention, the electrical circuit may further comprise a plurality of first and second signal parts in a cascade signal-transmitting circuit as the electrical circuit may further comprise a cascade of alternating first or second circuit parts and second or first circuit parts, respectively.

Provided the number of circuit parts is an even number, the output configuration of the electrical circuit is identical to the input configuration of the electronic circuit. Thus, provided the number of circuit parts is even, an electric circuit having a coplanar waveguide input also provides a coplanar waveguide output. Similarly, an electric circuit according to the present invention having an even number of circuit parts may have a coplanar strip line input and consequently also provide a coplanar strip line output.

Alternatively, the electric circuit according to the present invention may, apart from producing the parasitic capacitance eliminating or reducing feature characteristic of the present invention, provide a conversion from a coplanar waveguide into a coplanar strip line, or vice versa, by providing an odd number of circuit parts.

The active devices of the circuit parts of the electrical circuit according to the present invention may according to a first embodiment be implemented by FET transistors in which instance the first active device may be constituted by an FET in which the control terminal is constituted by a gate terminal of the FET and in which the two output terminals are constituted by drain and source terminals of the FET. Similarly, provided the second active device of the electrical circuit according to the present invention be implemented by an FET, the control terminals are constituted by gate and drain terminals of the FET, and the output terminal is constituted by a source terminal of the FET.

According to an alternative or supplementary embodiment of the electrical circuit, the active devices of the circuit parts may entirely or partially be constituted by transistors comprising base, emitter and collector terminals. Provided the first active device is constituted by a transistor having a base terminal, an emitter terminal and a collector terminal, the control terminal is constituted by the base terminal, and the two output terminals are constituted by the emitter and collector terminals. Similarly, provided the second active device is constituted by a transistor having a base terminal, an emitter terminal and a collector terminal, the control terminals are constituted by the base and the emitter terminals, and the output terminal is constituted by the collector terminal.

The electronic circuit according to the present invention is implemented from a single wafer chip and the active devices may advantageously be flip-mounted on the coplanar waveguides and coplanar strip lines. It is, however, to be contemplated that the electronic circuit or electronic design according to the present invention may be implemented as a stacked structure including transitions from a two-layer electrode configura-

ration to a three-layer electrode configuration, and vice versa, in accordance with the teachings of the present invention and constituting transitions from even mode to odd mode signal propagations, and vice versa.

The electronic circuit according to the present invention is preferably used in the ultrahigh frequency range for transmitting and/or amplifying ultrahigh frequency signals of a frequency within the frequency area 1 GHz - 10 THz, such as 10 GHz - 1 THz, preferably 100 GHz - 1 THz.

The present invention also relates to electronic circuit elements of an electronic circuit for transmitting high frequency signals, which circuit elements in accordance with the teachings of the present invention may comprise:

a waveguide means including an electrode, a coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative to one another, and an active device having a control terminal and two output terminals, said control terminal of said active device being connected to said electrode of said waveguide means, and said output terminals of said active device being connected to said two strip line electrodes of said coplanar strip line means, and/or may comprise:

a coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative to one another,

a waveguide means including an electrode, and

an active device having two control terminals and an output terminal, said control terminals of said active device being connected to said strip line electrodes of said coplanar strip line means, and said output terminal of said active device being connected to said electrode of said waveguide means.

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in the CPS to CPW transition.

Figure 7. Cascading two transistors with a CPW-CPS-CPW transition.

Figure 8. Circuit diagram for the transistor connection in a CPW-CPS-CPW transition.

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A circuit design is described comprising of a combination of odd and even mode signal propagation to suppress parasitic modes. The principle is explained by using a transition from coplanar strip lines (CPS, 2 strips) to coplanar waveguides (CPW, 3 strips) at the device site. The circuit design is intended for frequencies above 100 GHz and the signal is assumed to be a pulse. First, as shown in Fig. 1, the transition from CPW to CPS is described. On the CPW the transient voltage is applied between the center electrode 1 and the ground electrodes 2 and 3. This mode is the fundamental differential mode of the CPW and the associated electrical field has an odd symmetry. The mode structure is sketched in Fig. 1; the field has opposite sign between electrodes 3 and 1 and the electrodes 1 and 2. This pulse propagates along the CPW to the base b of transistor 6 and switches the device. The response of the transistor then changes the voltage and the field between the strips 4 and 5 of the CPS, hence generating the fundamental differential mode of the CPS (sketched in Fig. 1). The crucial point is that the initial CPW mode does not match a mode in the CPS. The contacts are designed in a symmetrical way. The symmetry axis lies on the center of electrode 1, the node of the electrical field  $E_{in}$ , and the center of the slot is formed by electrodes 4 and 5. In general, also in cases where the layout is not geometrically symmetric, it has to be ensured that the coupling impedances from electrode 2 to 4 and 2 to 5 are equal. Out of symmetry considerations the coupling of the differential mode of the CPW via the contact capacitance cancels on the CPS.

In Fig. 2 the principle is reversed by utilizing a CPS-CPW transition at the transistor 9. Again, based on symmetry consideration it is not possible that the fundamental differential mode of the CPS can generate a differential mode on the CPW by passive coupling. However, in this case the CPS mode coupled by the contact capacitances can induce a slot mode on the CPW. This mode is described by a field that has the same sign on both sides of the center electrode and has, in contrast to the fundamental differential mode, no node in the center.

Figures 3 and 4 show the equivalent circuit for a differential length,  $dz$ , of the transmission lines in the vicinity

ity of the CPW-CPS and the CPW-CPS transition. The inductances,  $L_{CPW1}$ ,  $L_{CPW2}$  and capacitances,  $C_{CPW}$ , correspond to a differential length of the CPW while  $L_{CPS}$  and  $C_{CPS}$  correspond to a differential length of the CPS. The transition and device site is represented by the coupling capacitances  $C_{g1}$ ,  $C_{g2}$ ,  $C_{g3}$ , and  $C_{g4}$ . Inductive and resistive coupling across the transition is neglected and the device itself is not considered.

For the CPW-CPS transition (Fig.3) the capacitances  $C_{g2}$  and  $C_{g3}$  have to be equal to ensure equal coupling from the center CPW-line ( $L_{CPW2}$ ) to the two CPS lines ( $L_{CPS}$ ). In this case, the input signal  $V_{in}$  does not appear in the output signal  $V_{out}$ . The same applies to the CPS-CPW transition (Fig. 4).  $C_{g2}$  and  $C_{g3}$  have to be equal so that the differential signal (for example positive on the top line and negative on the bottom line) cancels on the center line of the CPW ( $L_{CPW2}$ ). The transient voltages,  $V_{in}$  and  $V_{out}$ , and the bias voltages,  $V_e$ ,  $V_c$ , and  $V_b$ , together with the device --exemplified with an npn-transistor-- are shown in Fig. 5 and 6. Here the transmission lines are not considered.

Most important for the design of ultrahigh frequency circuits is the capability to cascade devices by using the disclosed circuit principle. The cascading of two transistors with a CPW-CPS-CPW transition is shown in Fig. 7. The input signal,  $V_{in}$ , is applied to the center line of the CPW and connected to the base of the first transistor 23. The response of this transistor to a voltage pulse at the base is a transient voltage  $V_{ec}$ , which is a differential mode of the CPS formed by the electrodes 24 and 25. This pulse propagates on the CPS to the second device 26. Here the signal  $V_1$  represents an input voltage  $V_{eb}$ . The response of transistor 26 is a transient voltage  $V_{ec}$ . The signal  $V_1$  can not couple to the center line 28 if all coupling impedances are kept symmetrical.

Only the differential mode generated by transistor 23 can switch transistor 26. Now the differential CPS mode does not match the differential CPW mode while the device 26 generates a 0-order CPW mode. However, in this case the CPS mode coupled by the contact capacitances can induce a slot mode on the CPW. This mode is described by a field that has the same sign on both sides of the center electrode and has, in contrast to the fundamental differential mode, no node in the center. Considering the symmetry of this mode it is possible that this mode couples to the CPS in the next stage. However, there are known ways to suppress this slot mode. In the simplest case the slot mode is shorted with an airbridge between the two outside conductors.

The design is equally suitable for fast bipolar transistors (e.g. heterojunction bipolar transistors) and for fast field effect transistors (e.g. high electron mobility transistors or pseudomorphic high electron mobility transistors). In the latter case the base is replaced by the gate and emitter and collector by source and drain, respectively.

The same principle can be applied to a microstrip - CPS or microstrip - coupled microstrip transition. For

short distances where a waveguide is not important to transmit the signal, a single conductor - CPS transition can be used instead.

Experiments with a conventional design for integrating a transistor into a transmission line have shown that the response is dominated by intrinsic and extrinsic capacitances and is only marginally influenced by the transistor as an active device. Two recently published articles show illustrate this problem. In one article (A Zeng et al., *Optical and Quant. El.*, Vol. 28, p. 867-874 (1996) a modulation doped FET is integrated in a CPS. The response of the transistor as an active device can not be identified. In two articles by another group (K. Ogawa et al., *Appl. Phys. Lett.*, Vol. 66, p. 1228-1230, and J. Allam et al., *Optical and Quant. El.*, Vol. 28, p. 867-874 (1996) the response is directly explained by a parasitic gate-drain capacitance of approximately 2 fF. In this article it is acknowledged that these devices can only be used in at these high frequencies if the parasitic capacitance is reduced.

In Fig. 9 and 10 unpublished results are shown that clearly exhibit the shortcomings of a conventional design. Fig. 9 shows a circuit design where the elimination of parasitic coupling is not used. For testing purposes a hetero junction bipolar transistor is integrated in a CPS together with a photoconductive switch. The photoconductive switch is used to generate an electrical pulse,  $V_{in}$ , with a rise time of 800 fs and a fall time of 0.5-1 ns. This pulse is guided by the CPS to the base of the integrated transistor. The results in Fig. 10 show that this design can not be used for operating or cascading fast devices. The signal labelled feedthrough shows the time resolved output signal for an unbiased transistor and is dominated by parasitic coupling of the input signal,  $V_{in}$ , across the transistor as a passive device. The other curve is measured with a collector voltage,  $V_c$ , of 1 V. The figure shows that  $V_{out}$  is reduced by about 20 %. A careful analysis, however shows that this change is due to the bias induced change of the passive components of the transistor. The transistor response as a current amplifier sets in at  $t = 15$  ps in Fig. 10 and can hardly be identified on this scale.

## Description of Figures

Figure 1. Transition between a CPW and CPS. Signal propagation is from top to bottom.  $V_e$  and  $V_c$  are bias voltages for emitter and collector applied through additional electrodes. The transient input voltage  $V_{in}$  is applied to the center electrode of the CPW (electrode 2). The associated transversal field amplitude  $E_{in}$  is sketched. The input is connected to the base of a bipolar transistor. The voltage difference determines the output voltage on the emitter. The parasitic signals from the base electrode to the collector electrode that are capacitively coupled to the emitter electrode have opposite sign. For an electrode configuration that is symmetric around the output electrode these contributions cancel.

Figure 2. Transition between a CPS and CPW. Signal propagation is from top to bottom.  $V_b$  and  $V_e$  are bias voltages for base and emitter. The transient input voltage  $V_{in}$  is applied to the CPS (electrodes 7,8). The associated transversal field amplitude  $E_{in}$  is sketched. The input is connected to the base and collector of a bipolar transistor. The base voltage determines the output voltage between emitter and collector. The parasitic signals from the base electrode that are capacitively coupled to the emitter electrode and the collector electrode have the same sign. For an electrode configuration that is symmetric around the input electrode these contributions cancel in the differential voltage output.

Figure 3. Equivalent circuit for the CPW-CPS transition. The CPW and the CPS are modeled with a loss free symmetrical transmission line model. The active device is not considered. The equivalent circuit is displayed for a differential length,  $dz$ , around the transition region. The CPW is described by  $C_{CPW}$ , representing the capacitive coupling between center and ground electrodes, and by the self inductances  $L_{CPW1}$ , for the ground lines,  $L_{CPW2}$ , for the center line. Losses and mutual inductances are not considered. The CPS is described by  $C$ ,  $rCPS$  representing the capacitive coupling between the two electrodes, and by the self inductances  $L_{CPS}$ , for each electrode. The dashed line represent the continuation of the line with differential length elements to the point where the input voltage is applied or the output voltage is considered. The transition region is represented by the capacitances  $C_{g1}$  and  $C_{g4}$ , for coupling from the ground electrodes of the CPW to the two electrodes of the CPS, and by  $C_{g2}$  and  $C_{g3}$ , for coupling from the center electrode of the CPW to the two electrodes of the CPS. For a symmetric design  $C_{g1}$  and  $C_{g4}$  are equal and  $C_{g2}$  and  $C_{g3}$  are equal.

Figure 4. Equivalent circuit for the CPS-CPW transition. The model of the CPW and the CPS is the same as described in Fig. 3. The transition region is represented by the capacitances  $C_{g1}$  and  $C_{g4}$ , for coupling from the two electrodes of the CPS to the ground electrodes of the CPW, and by  $C_{g2}$  and  $C_{g3}$ , for coupling from the two electrodes of the CPS to the center electrode of the CPW. For a symmetric design  $C_{g1}$  and  $C_{g4}$  are equal and  $C_{g2}$  and  $C_{g3}$  are equal.

Figure 5. Circuit diagram for the transistor connection in Figure 1.  $V_e$  and  $V_c$  are bias voltages for emitter and collector, respectively.  $V_{in}$  and  $V_{out}$  are the transient input and output voltages.

Figure 6. Circuit diagram for the transistor connection in Figure 2.  $V_b$  and  $V_e$  are bias voltages for base and emitter, respectively.  $V_{in}$  and  $V_{out}$  are the transient input and output voltages.

Figure 7. Cascading two transistors with a CPW-CPS-CPW transition. The input signal,  $V_{in}$ , propagates on the CPW (electrodes 20,21,22) and switches transistor 23. The output of this transistor propagates on the

CPS (electrodes 24, 25) and switches transistor 26. The response of transistor 26 is guided by a CPW (electrodes 27,28,29).

Figure 8. Circuit diagram for the transistor connection in Figure 7.  $V_b$  and  $V_e$  are bias voltages for base and emitter, respectively.  $V_{in}$  and  $V_{out}$  are the transient input and output voltages.

Figure 9. Sketch of a transistor integrated in a CPS together with a photoconductive switch. The photoconductive switch is used to generate an electrical pulse,  $V_{in}$ , with a rise time of 800 fs and a fall time of 0.5-1 ns. The switch voltage is applied to electrode 32. A dc bias voltage is applied to the base ( $V_b$ ) via electrode 34 and to the collector ( $V_c$ ) via electrode 37. The output voltage,  $V_{out}$ , is measured by electro-optic sampling between electrode 33 and 37.

Figure 10. Electro-optically sampled output signal,  $V_{out}$ , of the transistor. The signal labelled "feedthrough" is measured when the transistor is unbiased, the other curve is measured with a collector voltage,  $V_c$ , of 1 V.

In the same symmetry considerations as for coplanar structures the design can be applied to vertical, stacked, structures. In this case the transition would be from a two-layer electrode configuration supporting an even mode to a three-layer electrode configuration supporting an odd mode. For stacked layers figures 1, 2 and 7 can be considered vertical cuts through the layers.

It would make the design more interesting if it could be used for voltage amplification, for example by using a pull-up resistor at the collector. (Fig. 7 electrode 24).

In principle, it is possible to use the design in a voltage amplifier configuration. The requirement is that the symmetry between the electrodes 24 and 25 is not disturbed too much. The connected resistor should be significantly higher than the characteristic impedance of the transmission lines which is of the order of 100 Ohms. The capacitance should be smaller than the transition capacitances sketched in Fig. 4.

## Claims

1. An electronic circuit for transmitting high frequency signals, in particular ultrahigh frequency signals, comprising:

a first circuit part comprising:

a first waveguide means including a first electrode,  
a first coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative to one another, and  
a first active device having a control terminal and two output terminals, said control terminal of said first active device being connected to said first electrode of said

first waveguide means, and said output terminals of said first active device being connected to said two strip line electrodes of said first coplanar strip line means,

a second circuit part comprising:

a second coplanar strip line means of a symmetrical configuration and including two strip line electrodes arranged symmetrically relative to one another,

a second waveguide means including a second electrode, and

a second active device having two control terminals and an output terminal, said control terminals of said second active device being connected to said strip line electrodes of said second coplanar strip line means, and said output terminal of said second active device being connected to said second electrode of said second waveguide means,

and said first circuit part and said second circuit part being connected in a cascade configuration in which said first circuit part constitutes an input part in which said first electrode of said first waveguide means constitutes an input electrode, in which said second circuit part constitutes an output part in which said second electrode of said second waveguide means constitutes an output electrode, and in which said two strip line electrodes of said first coplanar strip line means of said first circuit part also constitutes said two strip line electrodes of said second coplanar strip line of said second circuit part, or alternatively connected in a cascade configuration in which said second circuit part constitutes an input part in which said two strip line electrodes of said second coplanar strip line means of said second circuit part constitute two input electrodes in which said first circuit part constitutes an output part, in which said two strip line electrodes of said first coplanar strip line means of said first circuit part constitute two output electrodes, and in which said second electrode of said second waveguide means of said second circuit part also constitutes said first electrode of said first waveguide means of said first circuit part.

2. The electronic circuit according to claim 1, said first waveguide means being constituted by a first coplanar waveguide of a symmetrical configuration in which said first electrode constitutes a centre electrode and further including two ground electrodes arranged symmetrically relative to said centre electrode, and/or said second waveguide means being

constituted by a second coplanar waveguide of a symmetrical configuration in which said first electrode constitutes a centre electrode and further including two ground electrodes arranged symmetrically relative to said centre electrode.

3. The electronic circuit according to any of the claims 1 or 2, said circuit further comprising a cascade of alternating first or second circuit parts and second or first circuit parts, respectively.

4. The electronic circuit according to claim 3, said circuit including an even number of circuit parts.

5. An electronic circuit according to claim 3, said circuit including an odd number of circuit parts.

6. The electronic circuit according to any of the claims 1-5, said first active device being constituted by an FET transistor in which said control terminal is constituted by a gate terminal of said FET and in which said two output terminals are constituted by drain and source terminals of said FET.

7. The electronic circuit according to any of the claims 1-6, said second active device being constituted by an FET in which said control terminals are constituted by gate and drain terminals of said FET and in which said output terminal is constituted by a source terminal of said FET.

8. The electronic circuit according to any of the claims 1-5, said first active device being constituted by a transistor having a base terminal, an emitter terminal and a collector terminal, said control terminal being constituted by said base terminal, and said two output terminals being constituted by said emitter and collector terminals.

9. The electronic circuit according to any of the claims 1-6, said second active device being constituted by a transistor having a base terminal, an emitter terminal and a collector terminal, said control terminals being constituted by said base and emitter terminals, and said output terminal being constituted by said collector terminal.

10. The electronic circuit according to any of the claims 1-9, said active devices being flip-mounted on said coplanar waveguides and coplanar strip lines.

11. The electronic circuit according to any of the claims 1-9, said electronic circuit transmitting and/or amplifying ultrahigh frequency signals of a frequency within the frequency area 1 GHz - 10 THz, such as 10 GHz - 1 THz, preferably 100 GHz - 1 THz.

12. An electronic circuit element of an electronic circuit

for transmitting high frequency signals, said electronic circuit element comprising:

a waveguide means including an electrode,  
 a coplanar strip line means of a symmetrical 5  
 configuration and including two strip line electrodes arranged symmetrically relative to one another, and  
 an active device having a control terminal and 10  
 two output terminals, said control terminal of said active device being connected to said electrode of said waveguide means, and said output terminals of said active device being 15  
 connected to said two strip line electrodes of said coplanar strip line means.

13. An electronic circuit element of an electronic circuit for transmitting high frequency signals, said electronic circuit element comprising:

a coplanar strip line means of a symmetrical 20  
 configuration and including two strip line electrodes arranged symmetrically relative to one another,  
 a waveguide means including an electrode, 25  
 and  
 an active device having two control terminals and an output terminal, said control terminals of said active device being connected to said strip line electrodes of said coplanar strip line 30  
 means, and said output terminal of said active device being connected to said electrode of said waveguide means.

14. The electronic circuit element according to any of 35  
 the claims 12 or 13, further comprising any of the features of the electronic circuit according to any of the claims 1-11.

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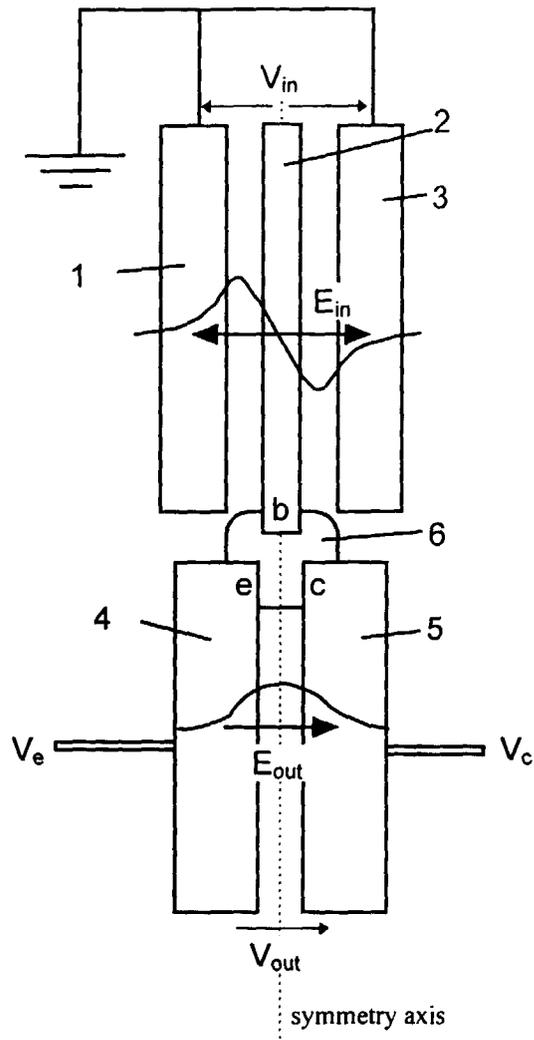


Figure 1

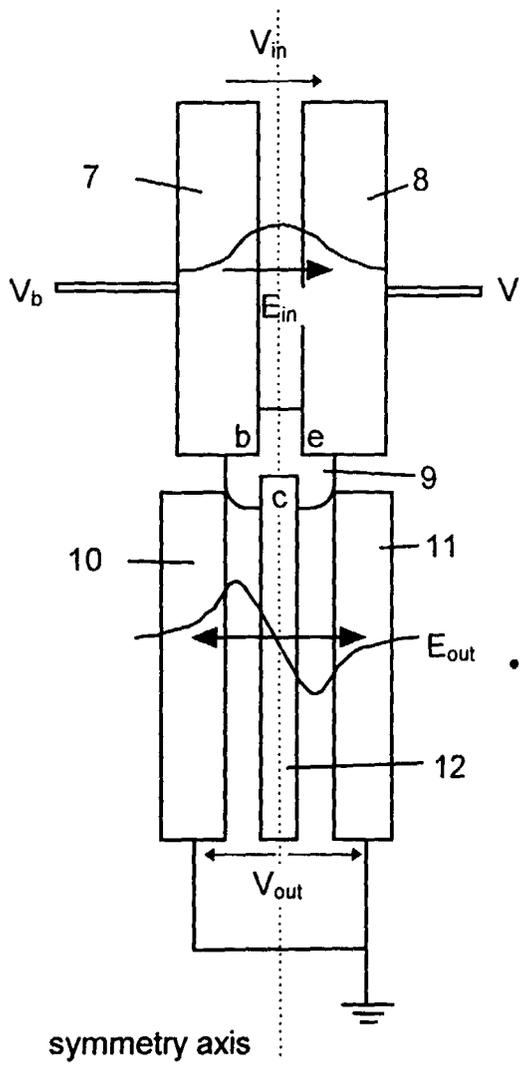


Figure 2

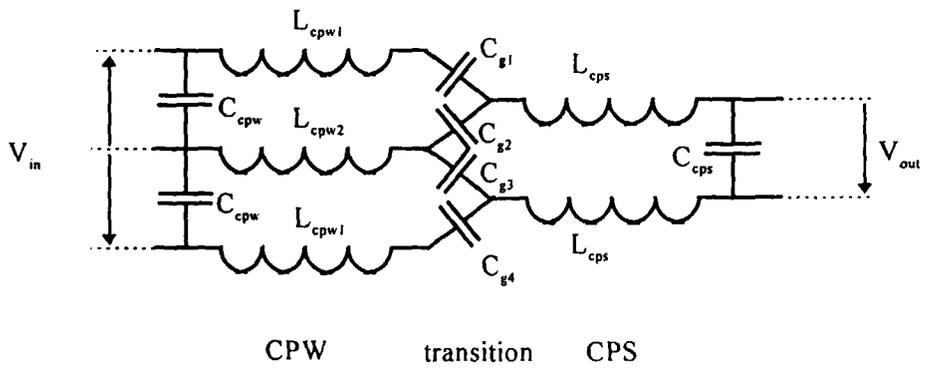


Figure 3

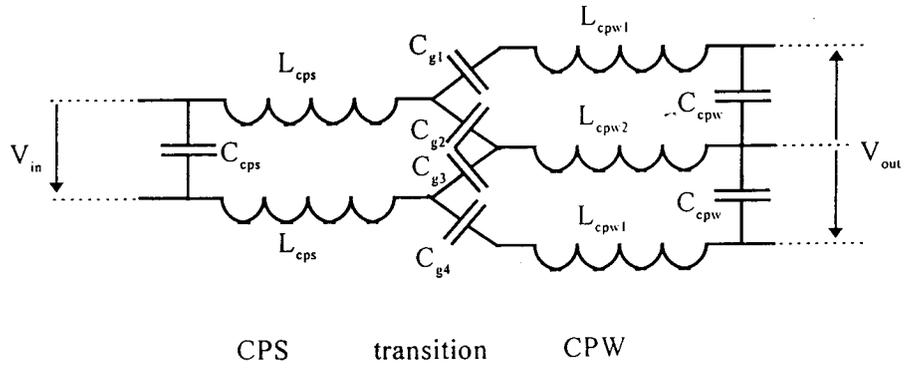


Figure 4

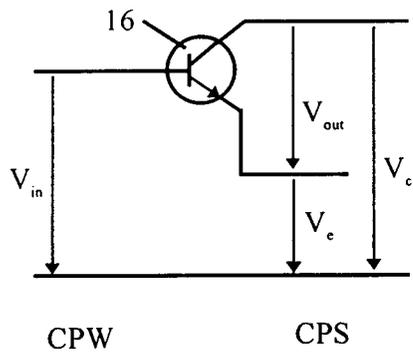


Figure 5

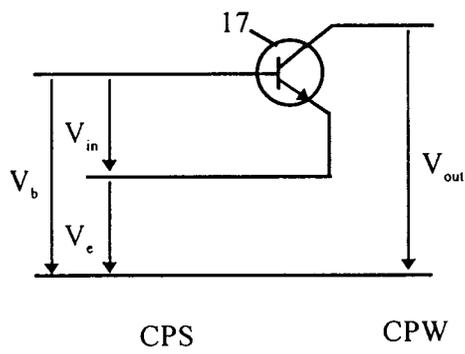


Figure 6

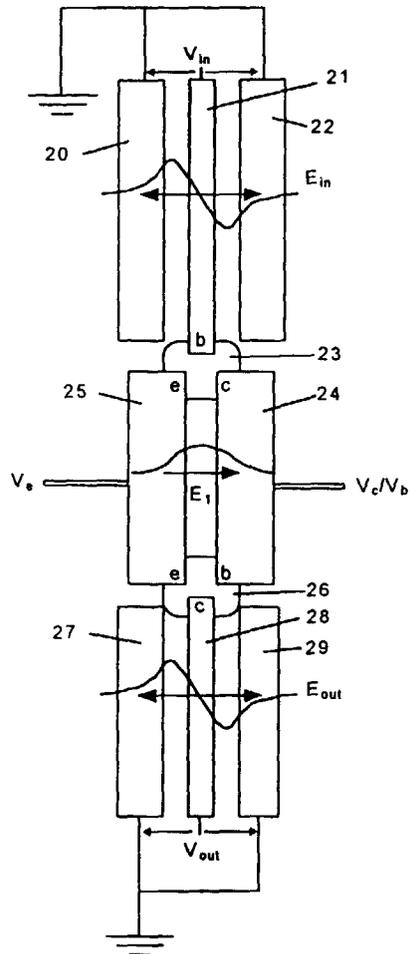


Figure 7

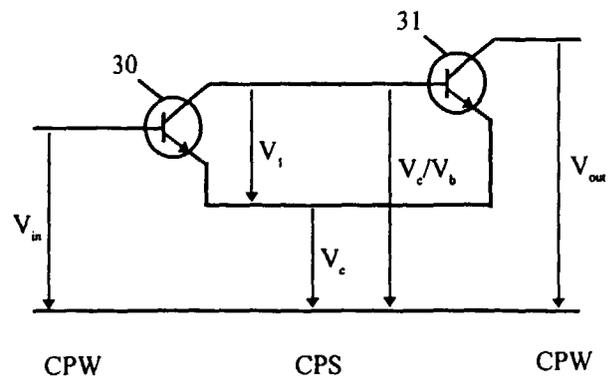


Figure 8

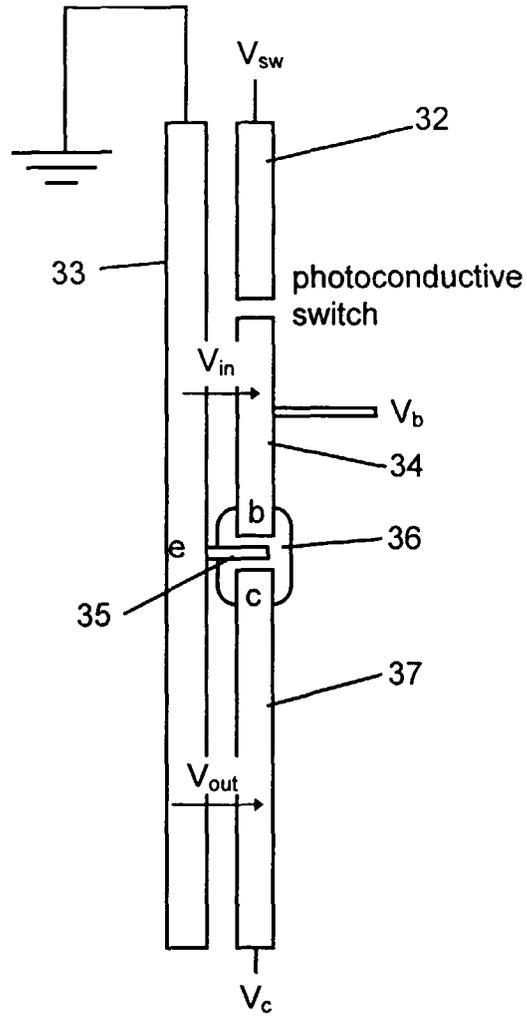


Figure 9

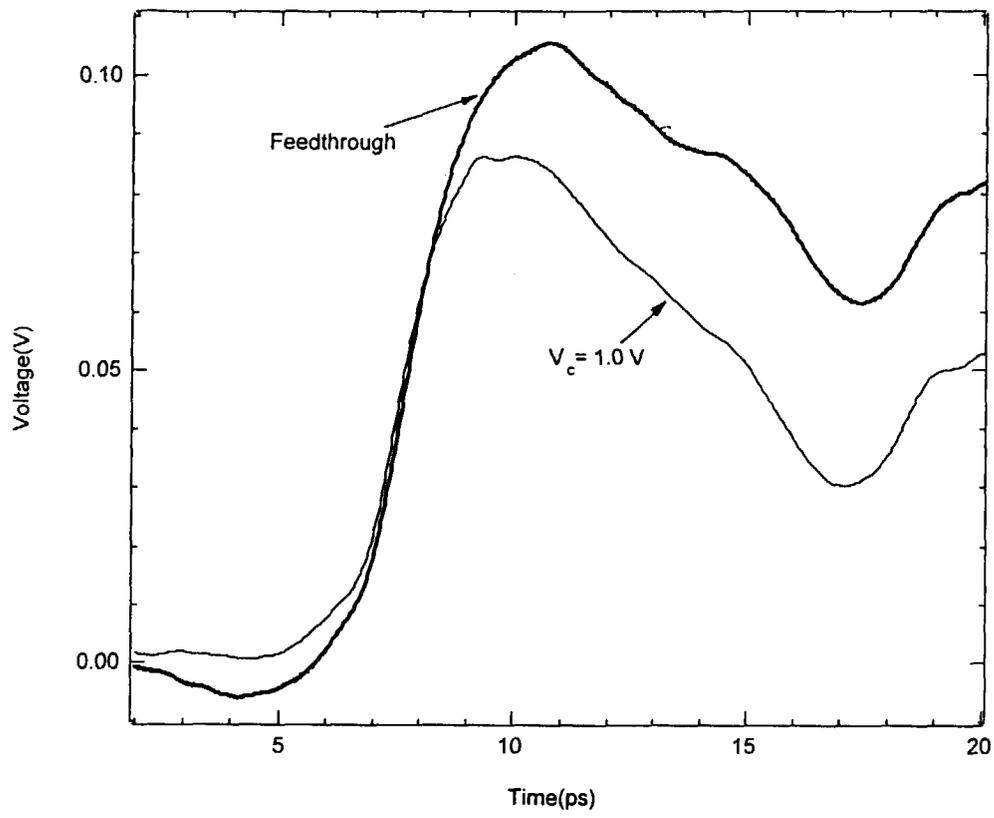


Figure 10



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Application Number  
EP 97 61 0017

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 3 805 194 A (MOULDING) * column 2, line 58 - column 3, line 14; figure 3 *	12	H01P5/10
Y	---	1-4,6, 10,11,14	
D,Y	US 5 550 518 A (MOHWINKEL)  * column 3, line 18 - column 4, line 20 * * column 4, line 44 - column 5, line 7; figures 3,4,7 *	1-4,6, 10,11,14	H01P H03H
X	---	12	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 321 (E-367), 17 December 1985 & JP 60 153602 A (NIPPON DENSHIN DENWA KOSHA), 13 August 1985, * abstract *	1,13	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
X	---	12	H01P H03H
A	US 5 142 255 A (CHANG ET AL.) * column 11, line 12 - line 32; figure 26 *  --- MASAYOSHI AIKAWA ET AL: "MMIC PROGRESS IN JAPAN" MICROWAVE AND MILLIMETER WAVE MONOLITHIC CIRCUITS SYMPOSIUM, LONG BEACH, JUNE 12 - 13, 1989, no. -, HUA QUEN TSERNG, pages 1-6, XP000131922 * figure 3A *  --- -/--	1,6,7, 11-13	
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>6 October 1997</b>	Examiner <b>Den Otter, A</b>
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document	

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EUROPEAN SEARCH REPORT

Application Number  
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	GROSS W: "BALANCED RESISTIVE MESFET MIXER IN UNIPLANAR TECHNOLOGY" PROCEEDINGS OF THE 23RD. EUROPEAN MICROWAVE CONFERENCE, MADRID, SEPT. 6 - 9, 1993, EUROPEAN MICROWAVE CONFERENCE MANAGEMENT COMMITTEE, page 405/406 XP000629954 * figures 5,7 *	1,6,7, 11-13	
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
Place of search THE HAGUE		Date of completion of the search 6 October 1997	Examiner Den Otter, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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