(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 886 257 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
23.12.1998 Bulletin 1998/52

(51) Int. Cl.[6]: **G09G 3/36**

(21) Application number: **98111163.6**

(22) Date of filing: **17.06.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **19.06.1997 JP 163093/97**
17.07.1997 JP 192927/97

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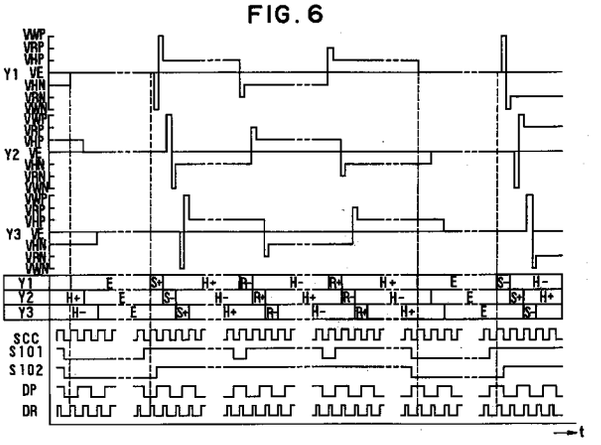
(54) Liquid crystal display device with matrix electrode structure, using an antiferroelelectric liquid crystal

(57) The present invention provides a liquid crystal display device, using an antiferroelectric liquid crystal, having a matrix electrode structure in which flicker of picture images displayed on a panel (10) is invisible. Scanning electrodes (Y1 to Yn) of the matrix are driven by alternating voltages which include voltages for holding picture images displayed on the panel. Refresh pulse voltages are imposed on the scanning electrodes every time the polarity of the holding voltages is reversed, so that the brightness of the picture images does not change before and after the reversal of the holding voltage polarity. An interlaced scanning is employed to further reduce the flicker by making a picture frame frequency higher. In addition, the same polarity of selecting voltages is maintained for a certain period of time to reduce the flicker due to an asymmetric characteristic of the liquid crystal (10c).

FIG. 6



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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is related to and claims priority from Japanese Patent Applications No. Hei-9-163093, filed on June 19, 1997 and No. Hei-9-192927, filed on July 17, 1997, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a liquid crystal display device, and more particularly to a liquid crystal display device which has a matrix electrode structure to drive n × m pixels.

2. Description of Related Art

JP-A-7-43676 discloses a liquid crystal display with a simple matrix electrode structure which is able to display images of intermediate brightness in addition to bright and dark images. As the liquid crystal for the display, an anti-ferroelectric material is used. The anti-ferroelectric liquid crystal of this kind has at least one anti-ferroelectric state (the first stable state) and two ferroelectric states (the second and third stable states), and each of these states can be attained stably.

According to the disclosure of the above-mentioned publication, voltages applied to the liquid crystal panel are reversed periodically so that a direct current component is not applied to the panel. A transparent state of the panel is realized by using two ferroelectric states alternately, and a non-transparent state is realized by using the anti-ferroelectric state of the anti-ferroelectric liquid crystal. To display images of intermediate brightness, an eliminating period in which pixels are temporarily turned to a dark state (anti-ferroelectric state) is provided before each selecting period.

The anti-ferroelectric liquid crystal panel shows different refractive anisotropies (Δn) between the two ferroelectric states when it is seen from slanting directions. Therefore, the display will flicker when the switching frequency between the two ferroelectric states becomes lower than, e.g., 30 Hz. The flicker of this kind is referred to as the slanting direction flicker. In addition, since the dark state appears temporarily in the eliminating period even when the bright state continues before and after the eliminating period, this dark state also causes the flicker. In order to eliminate the flicker, it is conceivable to choose a switching frequency which is higher than 30 Hz.

However, there is a certain limit in increasing the switching frequency in consideration of a response speed of the anti-ferroelectric liquid crystal, especially when a higher number of scanning electrodes is required to attain high definition of the display.

Proposals to prevent the flicker have been made, for example, in JP-A-4-311920. It proposes to switch the polarity of the applied voltage at a frequency which does not show the flicker during a holding period. However, since the holding voltage is switched or reversed at a same value, a brightness of the panel after the switching does not maintain the brightness before the switching. This is because the anti-ferroelectric liquid crystal does not respond as quickly as the polarity changes. Therefore, the brightness of the panel changes every time the polarity is switched, and the flicker on the panel caused by the frequency rewriting pictures on the panel cannot be avoided. This problem is more notable when the images of intermediate brightness are displayed.

Also, JP-A-7-20441 proposes to prevent the flicker by not providing the eliminating period and partially rewriting the pixels, thereby decreasing the brightness change from the bright state to the dark state. However, the intermediate brightness cannot be obtained because the eliminating period is not provided. It is also proposed in this publication to employ an interlaced scanning (in which the scanning electrodes are not scanned sequentially but scanned in a fashion jumping one or more neighboring scanning electrodes). However, if the interlaced scanning is used together with the eliminating period to obtain the intermediate brightness, brightness change due to the eliminating period causes a problem such as a scrolling stripe or a line flicker. The scrolling stripe is such a phenomenon in which change of brightness moving in the direction of scanning is observed as a stripe, and the line flicker is a phenomenon in which change of brightness is seen in parallel to the scanning electrodes. Both phenomena are observed as a substantially same phenomenon.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above-mentioned problems, and an object of the present invention is to provide a liquid crystal display device which does not show the flicker when it is driven by an alternating voltage. Another object of the present invention is to provided a liquid crystal display device in which scrolling stripes and/or the line flicker are practically invisible.

The liquid crystal display device is substantially composed of a display panel having a matrix electrode structure and a liquid crystal such as an anti-ferroelectric liquid crystal, a scanning electrode driving circuit and a signal electrode driving circuit. One scanning field is composed of a selecting period in which picture images are written on the pixels, a holding period in which the picture images are maintained, and an eliminating period in which the picture images written on the pixels are eliminated. Signals carrying picture images are imposed on the signal electrodes in synchronism with the scanning voltages. In the holding period, the

holding voltage polarity is reversed.

According to the present invention, a refresh pulse voltage is imposed every time the holding voltage polarity is reversed in order to keep the brightness of the picture images constant before and after the reversal of the holding voltage polarity. The level and duration of the refresh pulse voltage are selected so that the anti-ferroelectric state of the liquid crystal is not switched to the ferroelectric states while positive and negative ferroelectric states are switched to and from each other. Also, the interlaced scanning in which one or more scanning electrodes are jumped is employed to further reduce the flicker. A proper number of jumping in the interlaced scanning is selected so that the flicker including the line flicker and the scrolling flicker becomes substantially invisible.

The polarity of the voltage imposed in the selecting period may be reversed every selecting period. However, it is preferable to keep it at the same polarity for a certain period of time, for example, three hours, to avoid the brightness change which may occur due to an asymmetric characteristic of the anti-ferroelectric liquid crystal. The polarity switchover of the selecting voltage may be attained by a timer installed in the control circuit, or at a time when power supply to the display device newly commences or every time when a screen saver is in operation.

Various tests have been conducted as to how the anti-ferroelectric liquid crystal responds to the voltages applied thereto. Generally, there are three types of the response in the anti-ferroelectric liquid crystal: when it changes from the anti-ferroelectric state to the ferroelectric states, from one of the ferroelectric states to the other ferroelectric state, and from the ferroelectric states to the anti-ferroelectric state. To attain the object of the present invention, it is necessary that the brightness of the display panel does not change when the polarity of the applied voltage is reversed during a holding period. In other words, it is required to maintain the brightness of the panel at the same level after the polarity of the applied voltage is reversed during the holding period as the level which is attained before the voltage is reversed. If this is realized, the polarity of the applied voltage can be reversed during the holding period without causing the flicker.

A graph in FIG. 38 shows response time characteristics of the anti-ferroelectric liquid crystal versus voltages applied thereto. In this graph, a curve L1 shows the response time (τr) of the anti-ferroelectric state to the ferroelectric state at a temperature of 40°C, and a curve L2 shows its response time (τ) when it changes from a positive ferroelectric state to a negative ferroelectric state or vice versa at 40°C. According to this graph, when 20 volts is applied, the response time (τr) is 250 μ sec., and the response time (τ) is 33.5 μ sec. It is apparent that there is a big difference between the response time (τr) and (τ).

This difference can be utilized to change the state of the liquid crystal, regions of which are in one ferroelectric state, to another ferroelectric state, while keeping regions which are in the anti-ferroelectric state in the same state. This means that it is possible to switch the polarity of the applied voltage during the holding period without causing a visible flicker on the display. In other words, when a refresh voltage (a recovery voltage) of 20 volts having a duration of 33.5 μ sec. is applied at the time of polarity change during the holding period, only the change between the positive and negative ferroelectric states occurs without causing the change from the anti-ferroelectric state to the ferroelectric state. Thus, the visible flicker can be suppressed.

As illustrated in FIG. 39, regions of a pixel which are in one of the ferroelectric states can be changed to the other ferroelectric state by applying such a refresh voltage, while keeping regions which are in the anti-ferroelectric state unchanged. Thus, the brightness of the display can be maintained at the same level before and after the change of the polarity of the voltage applied during the holding period. This can be attained irrespective of the level of brightness, i.e., bright, dark or intermediate levels.

According to the graph of FIG. 38, when the refresh pulse of 20 volts, which is to be applied during the holding period, having a pulse width or duration in a range between the curve L1 and L2 is chosen, the brightness of the panel can be kept at the same level or the brightness change can be minimized before and after the polarity of the holding voltage is reversed. By utilizing the phenomenon mentioned above, the present invention can provide a liquid crystal display device with a matrix electrode structure in which the flicker of the display is substantially invisible.

Further, a level of signal voltages applied to a group of signal electrodes during the period in which the refresh voltage is applied to scanning electrodes is chosen at a base level of variations of the signal voltages. Because of this, signal voltages representing a bright display or a dark display are not affected by adding the base level of the signal voltages. Accordingly, a brightness of a pixel which is refreshed is not affected by signal voltages representing a brightness of other pixels on the same scanning electrode as the pixel to be refreshed.

Further, the polarity of the holding voltage of a scanning electrode is opposite to that of a neighboring scanning electrode during at least a half of a repeating cycle of a selecting period. This makes the switching frequency of the holding voltage polarity look faster than that of a field reversing method, and, accordingly, the flicker of the display due to the polarity switching is prevented.

According to the present invention, the holding voltage polarity can be alternately reversed on each of the scanning electrodes to prevent an image stick on the display without causing the flicker thereon by adding the refresh voltage to the holding voltage at every time

when the holding voltage polarity is reversed.

Other objects and features of the present invention will become more readily apparent from a better understanding of the preferred embodiments described below with reference to the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a whole structural diagram showing a first embodiment of a liquid crystal display device with a matrix electrode structure according to the present invention;

FIG. 2 is a cross-sectional view of a liquid crystal display panel;

FIG. 3 is a drawing showing a model of pixels of the display panel;

FIG. 4 is a diagram showing a scanning electrode driving circuit;

FIG. 5 is a detailed diagram showing a decoder circuit;

FIG. 6 is a timing chart for explaining the operation of the scanning electrode driving circuit;

FIG. 7 is a signal electrode driving circuit diagram;

FIG. 8 is a detailed circuit diagram of a decoder;

FIG. 9 is a timing chart for explaining the operation of the signal electrodes driving circuit;

FIG. 10 is a timing chart for explaining an operation of the liquid crystal display device;

FIG. 11 is a timing chart showing waveforms of voltages applied to a pixel G(i,1) at its bright state;

FIG. 12 is a timing chart showing waveforms of voltages applied to a pixel G(i,2) at its dark state;

FIG. 13 is a timing chart showing waveforms of voltages applied to a pixel G(i,3) at its bright state;

FIG. 14 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its bright state in a first field and transparent light intensities of an anti-ferroelectric liquid crystal;

FIG. 15 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its dark state in a first field and transparent light intensities of an anti-ferroelectric liquid crystal;

FIG. 16 is a timing chart showing the scanning voltages supplied from the scanning electrode driving circuit, when the selecting voltage of a same polarity is imposed on the scanning electrodes for more than one field and the holding voltage polarity is switched one time in a field;

FIG. 17 is a timing chart continued from FIG. 16;

FIG. 18 is a timing chart showing the scanning voltage, the signal voltage and the brightness of the display when the holding voltage polarity is switched one time in a field;

FIG. 19 is a timing chart showing waveforms of voltages applied to a pixel G(i,1) at its bright state;

FIG. 20 is a timing chart showing waveforms of voltages applied to a pixel G(i,2) at its dark state;

FIG. 21 is a timing chart showing waveformes of voltages applied to a pixel G(i,3) at its bright state;

FIG. 22 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its bright state and transparent light intensity of the anti-ferroelectric liquid crystal;

FIG. 23 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its dark state and transparent light intensity of the anti-ferroelectric liquid crystal;

FIG. 24 is a timing chart showing the scanning voltages supplied from the scanning electrode driving circuit, when the selecting voltage of a same polarity is imposed on the scanning electrodes for more than one field and the holding voltage polarity is switched three times in a field;

FIG. 25 is a timing chart showing the scanning voltage, the signal voltage and the brightness of the display when the holding voltage polarity is switched three times in a field;

FIG. 26 is a whole structural diagram showing a third embodiment of a liquid crystal display device with a matrix electrode structure according to the present invention;

FIG. 27 is a diagram showing a scanning electrode driving circuit;

FIG. 28 is a diagram showing a 2-bit register shown in FIG. 27;

FIG. 29 is a timing chart for explaining the operation of the scanning electrode driving circuit;

FIG. 30 is a timing chart showing scanning voltages and scanning patterns;

FIG. 31 is a timing chart showing the scanning voltage and signal voltage;

FIG. 32 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its bright state and transparency of anti-ferroelectric liquid crystal;

FIG. 33 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its bright state shifting to its intermediate state and transparency of anti-ferroelectric liquid crystal;

FIG. 34 is a timing chart showing waveforms of voltages applied to a pixel G(i,j) at its bright state shifting to its dark state and transparency of anti-ferroelectric liquid crystal;

FIG. 35A is a chart showing brightness of each row and an average brightness under sequential scanning;

FIG. 35B is a chart showing brightness of each row and an average brightness under interlaced scanning;

FIG. 36 is a chart showing the flicker and scrolling stripe which are observed under sequential and interlaced scanning (the number of scanning electrodes jumped: 1, 2, 3 and 4);

FIGS. 37A, 37B and 37C are charts for explaining the scrolling stripe;

FIG. 38 is a graph showing the response time of anti-ferroelectric liquid crystal versus the holding

voltage; and

FIG. 39 is a model showing the change of states in anti-ferroelectric liquid crystal when a refresh voltage is applied.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

A first embodiment according to the present invention will be described with reference to FIGS. 1 to 15.

FIG. 1 shows a whole structure of a liquid crystal display device with a matrix electrode arrangement. The device includes a liquid crystal display panel 10, as shown in FIG. 1 and FIG. 2. The display panel is composed of electrode plates 10a and 10b, an anti-ferroelectric liquid crystal 10c filling the space between the two plates, and two polarizer layers 10d and 10e each of which is attached to the surface of the respective electrode plates 10a and 10b.

As shown in FIG. 2, the electrode plate 10a is composed of: a glass substrate 11; a color filter layer 12 having m stripes of R (red), G (green) and B (blue), which is disposed on the bottom surface of the glass substrate 11; a transparent electrode layer 13 having m stripes disposed underneath the color filter layer 12; and an orientation film 14 disposed underneath the transparent electrode layer 13.

The electrode plate 10b is composed of: a glass substrate 15; a transparent electrode layer 16 having n stripes disposed on the glass substrate 15; and an orientation film 17 disposed on the transparent electrode layer 16.

The m stripes of the transparent electrode layer 13 and the n stripes of the transparent electrode layer 16 constitute an ($m \times n$) matrix of pixels together with the anti-ferroelectric liquid crystal 10c, as shown in FIG. 3. The pixels, G(1,1), G(1,2).....G(m,n) are arranged as shown in FIG. 3. The m stripes of the transparent electrodes 13 correspond to signal electrodes, X1, X2...Xm, in FIG. 1 and the n stripes of the transparent electrodes 16 correspond to scanning electrodes, Y1, Y2...Yn, in FIG. 1.

The polarizer plates 10d and 10e are disposed in a cross nicol relation. Due to this arrangement, the anti-ferroelectric liquid crystal becomes non-transparent in its anti-ferroelectric state. The two electrode plates 10a and 10b are kept at a uniform distance of, e.g., 2 μm by a number of spacers not shown in the drawing.

As the anti-ferroelectric liquid crystal material 10c, a material such as, for example, 4-(1-trifluoromethylheptoxycarbonylphenyl)-4'-octyloxycarbonylphenyl-4-carboxylate shown in JP-A-5-119746 can be used. Some other materials such as a mixture of several kinds of anti-ferroelectric liquid crystal or a mixture of liquid crystal materials including one kind of anti-ferroelectric liquid crystal may be used.

As shown in FIG. 1, the display device includes a control circuit 20, a power source circuit 30, another power source circuit 40, a scanning electrode driving circuit 50 and a signal electrode driving circuit 60. The control circuit 20 delivers output signals, two DPs, DR, SI01, SI02, SCC, LCK, STD, and SIC, while receiving a vertical synchronizing signal VSYC and a horizontal synchronizing signal HSYC from outside circuits. One of the DP signals (a first DP), DR signal, SI01 signal, SI02 signal and SCC signal are fed to the scanning electrode driving circuit 50. The other DP (a second DP), LCK, STD, and SIC signals are fed to the signal electrode driving circuit 60.

The SI01 and SI02 signals are the signals to decide a condition of the scanning electrodes, Y1, Y2....Yn. In this embodiment, a condition where the SI01 signal is L (low) and SI02 signal is also L corresponds to an eliminating period of the scanning electrode. Similarly, when SI01 is H (high) and SI02 is L, the scanning electrode is in a selecting period; when SI01 is H and SI02 is H, the scanning electrode is in a holding period; and when SI01 is L and SI02 is H, the scanning electrode is in a refreshing period.

The power source circuit 30 delivers seven output signals, VWP VRP, VHP, VE, VHN, VRN and VWN (FIGS. 1 and 6), while the other power source circuit 40 outputs nine voltages for displaying eight levels of brightness, V1, V2, V3, V4, V5, V6, V7, V8 and VG (FIGS. 1 and 9).

The scanning electrode driving circuit 50 supplies eight voltage levels sequentially to the scanning electrodes, Y1... Yn, which correspond to the eliminating, selecting, holding and refreshing periods, based on the signals, the first DP, DR, SI01, SI02 and SCC from the control circuit 20. The driving circuit 50 also switches the polarity of the applied voltages at every selecting period for driving the scanning electrodes by alternating voltages (refer to FIG. 10).

Referring to FIG. 10, operation of the scanning electrode driving circuit 50 will be explained, taking a scanning electrode Y1 as an example. During an eliminating period (E in FIG. 10), displays on all of the pixels located on the scanning electrode Y1 are eliminated by applying the voltage VE to the scanning electrode Y1. The selecting period (S in FIG. 10) is divided into three periods. During a positive selecting period, the voltage VE which is the same as the voltage applied during the eliminating period is applied in the first period, a negative selecting voltage VWN in the second period, and a positive selecting voltage VWP in the third period, as shown in FIG. 10. Picture image data coming from the signal electrodes are imposed on the pixels on the scanning electrode Y1 during the selecting period. In a positive holding period (H+ in FIG. 10), a positive holding voltage VHP is applied to the scanning electrode Y1 and the picture image data is maintained.

A negative refreshing period (R in FIG. 10) is divided into two periods, a first and a second period. A

negative refreshing voltage VRN is applied to the scanning electrode in the first period. The first period corresponds to a period during which a voltage VG is delivered from the signal electrode driving circuit 60 as described later, and the polarity of the holding voltage is reversed in this period while maintaining the image data as before. A negative holding voltage VHN is applied in the second period of the negative refreshing period. Then, a negative holding period (H- in FIG. 10) follows. During the negative holding period, the negative holding voltage VHN is applied and the image data are kept as before. Then, a positive refreshing period (R in FIG. 10) and the next positive holding period follow. The eliminating period comes again after the positive holding period.

Then, the next selecting period follows. This selecting period is a negative one as opposed to the foregoing positive selecting period. In the first period of the negative selecting period, the voltage VE is applied, and the positive selecting voltage VWP is applied in the second period. Then, in the third period the negative selecting voltage VWN is applied to the scanning electrode. The image data coming from the signal electrodes are imposed on the pixels on the scanning electrode Y1 during the selecting period. Then, the negative holding voltage VHN is applied in the negative holding period and the image data are maintained. Then, the positive refreshing period, the positive holding period, the negative refreshing period, and the negative holding period follow. These sequences are repeated thereafter.

The operation described for the scanning electrode Y1 is applied in the same manner to other scanning electrodes, Y2....Yn. The scanning from the electrode Y1 through the electrode Yn is done sequentially with a phase difference of the duration of the selecting period as shown in FIG. 10. In order to prevent the flicker on the display, the polarity of neighboring scanning electrodes is alternately selected, in such a way that, for example, Y1 is positive, Y2 is negative, Y3 is positive, and so forth.

The operation of the scanning electrode driving circuit 50 will be explained referring to FIG. 4.

The scanning electrode driving circuit 50 includes n 2-bit registers (RY1, RY2...RYn), n decoder circuits (DY1, DY2...DYn), n level shifters (SY1, SY2...SYn), and n analog switch circuits (WY1, WY2...WYn). Each of the analog switch circuits includes seven analog switches. The scanning electrode driving circuit 50 performs the function mentioned above based on five kinds of signals received from the control circuit 20.

The 2-bit registers (RY1, RY2...RYn) sequentially receive SI01 and SI02 signals from the control circuit 20 in synchronism with the rising of a SCC signal, and output 2-bit data (bit-1 and bit-2) to the decoder circuits (DY1, DY2...DYn). The decoder circuits (DY1, DY2...DYn) produce signals of seven kinds which perform switching operations on the analog switch circuits (WY1, WY2...WYn), based on the 2-bit data from the 2-bit registers (RY1, RY2...RYn) and the first DP signal and the DR signal from the control circuit 20.

Each of the decoder circuits (DY1, DY2...DYn) is composed as shown in FIG. 5, and has six logic circuits 51 through 56. The operation of the decoder circuit will be explained taking DY1 as an example.

The logic circuit 51 composed of four inverters and four AND gates, as shown in FIG. 5, decodes the 2-bit data (bit-1 and bit-2) received from the 2-bit register RY1, and converts them into signals, DDE, DDW, DDR and DDH which perform a switching function. During the eliminating period (SI01 is L and SI02 is L), only the DDE signal becomes H (high) and other signals become L (low). During the selecting period (SI01 is H and SI02 is L), only the DDW signal becomes H and other signals become L. During the refreshing period (SI01 is L and SI02 is H), only the DDR signal becomes H and other signals become L. During the holding period (SI01 is H and SI02 is H), only the DDH signal becomes H and other signals become L.

The logic circuit 52 composed of four AND gates, an inverter and two OR gates, as shown in FIG. 5, controls switching signals from the logic circuit 51 based on the DR signal, and outputs the signals of DEE, DWW, DRR and DHH. When the DDE signal is H, only the DEE signal becomes H. When the DDW signal is H, only the DEE signal becomes high during the time when the DR signal is H, and only the DWW signal becomes H during the time when the DR signal is L. When the DDR signal is H, only the DRR signal becomes H during the time when the DR signal is H, and only the DHH signal becomes H during the time when the DR signal is L. When the DDH signal is H, only the DHH signal becomes H.

The logic circuit 53 is composed of elements shown in FIG. 5. In the logic circuit 53, clocked inverters 53c and 53f are operated by an inverted output from an inverter 53a, and clocked inverters 53d and 53e are operated by a cascade output from the inverters 53a and 53b. According to the operation of the clocked inverters and other logic gates, the logic circuit 53 is reset when the DDW signal is H and reverses an output of an OR gate 53g in synchronism with rising of the DDR signal.

The logic circuit 54 is composed of elements shown in FIG. 5 and performs a function of latching data. In the logic circuit 54, a clocked inverter 54c is operated by an inverted output from an inverter 54a which inverts the DDW signal, and a clocked inverter 54d is operated by a cascade output from the inverters 54a and 54b. According to the operation of the clocked inverters and other logic gates, the logic circuit 54 outputs the first DP signal as it is when the DDW signal is H, and latches the first DP signal when the DDW signal is L.

The logic circuit 55 is composed of an exclusive OR gate and outputs an exclusive logical sum of the outputs from the logic circuits 53 and 54 as a DPP signal to the logic circuit 56. During the time when the DDW signal is H, the DPP signal corresponds to the first DP signal and

its voltage polarity is controlled by the first DP signal, because the logic circuit 53 is reset and its output becomes L and the logic circuit 54 outputs the same output as the output of the logic circuit 53. When the DDW signal becomes L, the DPP signal becomes independent from the first DP signal because the logic circuit 54 performs the latch function. Since the logic output from the logic circuit 53 is reversed in synchronism with the rising of the DDR signal, the DPP signal is reversed every time the DDR signal rises and the voltage polarity is reversed at every refreshing period.

The logic circuit 56 composed of six AND gates as shown in FIG. 5 switches the voltage polarity according to the signals from the logic circuit 52 and the DPP signal from the logic circuit 55. When the DWW and DPP signals are H, the DWP signal becomes H. When the DWW signal is H and the DPP signal is L, the DWN signal becomes H. When the DRR and DPP signals are H, the DRP signal becomes H. When the DRR signal is H and the DPP signal is L, the DRN signal becomes H. When the DHH and DPP signals are H, the DHP signal becomes H. When the DHH signal is H and the DPP signal is L, the DHN signal becomes H. The seven control signals DEE, DWP, DWN, DRP, DRN, DHP, and DHN are thus synthesized.

The DEE signal controls the analog switch (refer to FIG. 4) connected to a VE terminal of the power source circuit 30 through the level shifter. The DWP signal controls the analog switch connected to a VWP terminal of the power source circuit 30 through the level shifter. The DWN signal controls the analog switch connected to a VWN terminal of the power source circuit 30 through the level shifter. The DRP signal controls the analog switch connected to the VRP terminal of the power source circuit 30 through the level shifter. The DRN signal controls the analog switch connected to the VRN terminal of the power source circuit 30 through the level shifter. The DHP signal controls the analog switch connected to the VHP terminal of the power source circuit 30 through the level shifter. The DHN signal controls the analog switch connected to the VHN terminal of the power source circuit 30 through the level shifter. When a control signal is H, a corresponding analog switch becomes closed (ON) and a corresponding voltage is supplied from the power source circuit 30 to the scanning electrode. This applies to each one of the control signals (DEE, DWP, DWN, DRP, DRN, DHP and DHN).

Thus, voltages having a predetermined waveform as shown in FIG. 6 are supplied to each scanning electrode (Y1, Y2...Yn) according to the signals SCC, SI01, SI02 and first DP.

The signal electrode driving circuit 60, as shown in FIGS. 1 and 7, is composed of m 3-bit registers (RX1, RX2...RXm), m decoder circuits (DX1, DX2...DXm), m level shifters (SX1, SX2...SXm) and m analog switches (WX1, WX2...WXm). The signal electrode driving circuit 60 supplies signal voltages of nine levels from the power source circuit 40 to the signal electrodes (X1, X2...Xm) according to the picture image signal DAP from the outside and the signals, second DP, LCK, STD and SIC from the control circuit 20. The DAP signal is a 3-bit signal because the liquid crystal panel displays images having eight brightness steps.

The operation of the signal electrode driving circuit 60 will be explained referring to the timing chart shown in FIG. 9. The picture image signals DAP having 3-bit data are sent from the outside to the signal electrode driving circuit 60 as a series of data for all of the signal electrodes (X1, X2,...Xm). The picture image data are sent from the outside to the signal electrode driving circuit 60 sequentially, i.e., the data for the pixels on the scanning electrode Y1 come first and the data for the pixels on the scanning electrode Y2 come next, and the data come continuously in this way till the scanning electrode Yn. In FIG. 9, D(1,i) denotes a series of picture image data for pixels on the scanning electrode Y1, and D(1,1), D(1,2)....D(1,m), each denotes the picture image datum for the respective signal electrode, X1, X2...Xm. When the STD signal is H, the picture image signal corresponding to the signal electrode X1 is fed to the 3-bit register in synchronism with the rising of the SIC signal. Similarly, the picture image signals corresponding to the signal electrodes, X2, X3...Xm are sequentially fed to the 3-bit registers in synchronism with the rising of the SIC signal. Thus, the picture image data for the pixels on the one scanning electrode are stored in the 3-bit registers, RX1, RX2...RXm. The data stored in the 3-bit registers are fed to the decoder circuits.

As shown in FIG. 8, each of the decoders, DX1, DX2...DXm, has five logic circuits 61, 62, 63, 64 and 65. The operation of the decoders will be explained with reference to FIG. 8, taking DX1 as an example.

The logic circuit 61 composed of three D-type flip-flops latches the 3-bit picture image data in synchronism with a rising of the LCK signal from the control circuit 20. The logic circuit 62 composed of three exclusive OR gates reverses the picture image signals latched by the logic circuit 61 when the second DP signal from the control circuit 20 is H. The logic circuit 63 is composed of three pairs of inverters and eight AND gates, and constitutes a decoder. The logic circuit 63 decodes the 3-bit picture image data signals from the logic circuit 62 and converts them to eight line outputs. The logic circuit 64 composed of an inverter reverses the LCK signal from the control circuit 20. The logic circuit 65 having eight AND gates receives signals from the logic circuit 63 and outputs control signals, D1, D2... D8, which switch the eight analog switches of the analog switch circuit WX1, according to the outputs from the logic circuit 64. Also, the decoder circuit DX1 outputs the LCK signal as a control signal DG.

The decoder circuit DX1 constituted as mentioned above makes its respective outputs, D1 through D8, high (H) when the 3-bit data latched by the logic circuit 61 are respectively (L,L,L), (L,L,H), ... (H,H,L), (H,H,H),

under the condition that the second DP signal is L and the LCK signal is L. Under the condition that the second DP signal is H and the LCK signal is L, the decoder circuit DX1 makes its respective outputs, D8 through D1, high (H) in this order when 3-bit data latched by the logic circuit 61 are respectively (L,L,L), (L,L,H), ... (H,H,L), (H,H,H). Under the condition that the LCK signal is H, the outputs D1 through D8 become L irrespective of the 3-bit data, and only the output DG becomes H.

The outputs D1 through D8 and the output DG from the decoder control the analog switches connected to the voltages V1 through V8 and VG of the power source circuit 40, respectively, through the level shifter (refer to FIG. 7). When the outputs D1 through D8 and the output DG are H, corresponding analog switches become ON and the output voltages from the power source circuit 40 are supplied to the signal electrode.

After the picture image data for pixels on a scanning electrode are latched by the logic circuit 61 in synchronism with the rising of the LCK signal, the 3-bit registers (RX1 through RX2) begin to input the picture image data for the pixels on a next scanning electrode. Accordingly, as seen from the timing chart shown in FIG. 9, voltage outputs having prescribed waveforms are supplied to the signal electrodes X1 through Xm in response to the signals SIC, STD, LCK and second DP and picture image data DAP.

The output voltage VE from the power source circuit 30 and the output voltage VG from the power source circuit 40 are set at a common level. The signals, SCC, first DP and LCK, are synchronized with the signals, LCK and second DP, all signals being fed from the controller circuit 20. The picture image data for the pixels on a scanning electrode which is in the selecting period are input in advance by one selecting period. Thus, the waveforms shown in FIG. 10 are realized.

The operation of an example of the liquid crystal display device constructed according to the present invention, in which a one-frame display frequency is 5 Hz (a display period of one-frame is 200 ms), number of rows is 220, number of columns is 960, a scanning duty is 1/N (N=1000) and an eliminating period is E (E=100), will be explained below.

To the pixels, G(i,1), G(i,2), and G(i,3), the positions of which are shown in FIG. 3 as a model, driving voltages having waveforms shown in FIGS. 11, 12 and 13 are supplied. As shown in those drawings, the driving voltages imposed on the pixels are composed of voltages of the selecting, holding and eliminating periods. The driving voltages imposed during the holding period consist of a refresh pulse voltage and a holding voltage, and the polarity thereof is reversed at a frequency more than 30 Hz. Every time the polarity is reversed, the refresh pulse is imposed. One frame of the display consists of a first field and a second field. Referring to FIGS. 11, 12 and 13, the operation of the first frame will be explained below.

First, the sequence of the driving voltage imposed to the pixels will be explained. During a selecting period, a voltage VE having a pulse width t1 (t1 = 33.3 μs), a voltage VWN having a pulse width t2 (t2 = 33.3 μs) and a voltage VWP having a pulse width t2 are sequentially imposed. During a holding period which follows the selecting period, a holding voltage VHP is imposed. After 10 ms counting from the beginning of the selecting period, a refresh voltage VRN having a pulse width t1 is imposed, and then a holding voltage VHN is imposed until 10 ms lapses counting from the beginning of the refresh voltage. Then, a refresh voltage VRP having a pulse width t1 is imposed. After that, a holding voltage VHP is imposed until 10 ms lapses counting from the beginning of the refresh voltage VRP.

Thereafter, the cycle having the refresh pulse voltage and the holding voltage is repeated every 10 ms, changing the polarity thereof. This continues until the end of the Pth holding period (P = 9 in this example). The total time from the beginning of the selection period to the end of the Pth holding period is $(N-E) \cdot (t1+t2 \cdot t2)$. Then, the voltage VE is imposed for the eliminating period, i.e., $E \cdot (t1+2 \cdot t2)$.

The second field is constituted by the same selecting, holding and eliminating periods as in the first field, but the polarity of all the voltages imposed is just reversed.

Next, the sequence of signal voltages imposed at the pixels will be explained. Signal voltages for the selecting period consist of three pulse voltages having a pulse width, t1, t2 and t2, respectively, in accordance with the driving voltage waveform imposed on the scanning electrodes. To display a bright image in the first field, the voltage VG with a pulse width t1 is imposed, and then the voltage V8 with a pulse width t2 and the voltage V1 with a pulse width t2 follow. To display a dark image in the first field, the voltage VG with a pulse width t1 is imposed, and then the voltage V1 with a pulse width t2 and the voltage V8 with a pulse width t2 follow. To display a bright image in the second field, the voltage VG with a pulse width t1 is imposed, and then the voltage V1 with a pulse width t2 and the voltage V8 with a pulse width t2 follow. To display a dark image in the second field, the voltage VG with a pulse width t1 is imposed, and then the voltage V8 with a pulse width t2 and the voltage V1 with a pulse width t2 follow. The image signals mentioned above determine the display condition of the pixels in combination with the waveform of the scanning voltages.

The refresh pulse voltage imposed at the beginning of the holding period to the scanning electrodes is synchronized with the signal voltage VG. That is, the refresh pulse is imposed during the period when the signal voltage is VG. Thus, it is possible to always impose the refresh voltage VRP or VRN with a pulse width t1, irrespective of any combination with image signal waveforms which display a bright image or a dark image. Accordingly, a pixel which has been refreshed can display a image with the same brightness as before without

being influenced by image signal waveforms for other pixels on the same signal electrode, only the polarity of the holding voltage being reversed. The voltage imposed during the refreshing period is not necessarily limited to the voltage VG, but it may be a voltage corresponding to a base level voltage of signal voltage variation. When the base level voltage is used in stead of VG, substantially the same result can be obtained.

In order to improve angular visibility characteristics of the display, the polarity of neighboring scanning electrodes is reversed one by one, or group by group.

In the manner mentioned above, the voltages having the waveforms as shown in FIGS. 11, 12 and 13 are imposed on the pixels G(i,1), G(i,2) and G(i,3), respectively. The waveforms shown in the drawings correspond to the conditions where G(i,1) displays a bright image, G(i,2) a dark image and G(i,3) a bright image. The voltage imposed on each of those pixels is shifted in its phase by a period of (t1+2 • t2). In other words, a series of voltages imposed on the pixel G(i,2) during the selecting, holding and eliminating periods is delayed in its phase by the period (t1+2 • t2), compared with a series of voltages imposed on the pixel G(i,1). Similarly, the phase of the voltages imposed on following pixels are shifted by the same period.

Next, the state of a pixel G(i,j) where it is in a condition to display a bright image will be explained referring to FIG. 14 which shows the voltages imposed thereon and transparent light intensities of an anti-ferroelectric liquid crystal. The driving voltage having the waveform as shown in FIG. 14 is imposed. In the selecting period of the first field, the anti-ferroelectric liquid crystal is in a second stable state (a positive ferroelectric state shown by F+ in FIG. 14), and this state continues during the first holding period which follows the selecting period. The state of the liquid crystal is switched to a third stable state (a negative ferroelectric state shown by F- in FIG. 14) from the second stable state by a refresh pulse voltage VRN with a pulse width t1 which is imposed at the beginning of the second holding period, and this state is maintained during the second holding period by the holding voltage. Then, the state of the liquid crystal is again switched to the second stable state from the third stable state by a refresh pulse voltage VRP with a pulse width t1 which is imposed at the beginning of the third holding period, and this state is maintained during the third holding period by the holding voltage. Thereafter, the switching between the second stable state and the third stable state, which is performed every time the refresh pulse voltage is imposed, is repeated. The switching frequency is chosen so that flicker of the display is not visible, for example, 50 Hz. At the end of all holding periods, the state of the liquid crystal is switched to a first stable state (an anti-ferroelectric state).

In the second field, the anti-ferroelectric liquid crystal is in the third stable state during the selecting period, and this state is maintained during the first holding period which follows the selecting period. The state of the liquid crystal is switched to the second stable state from the third stable state by the refresh pulse voltage VRP with a pulse width t1 which is imposed at the beginning of the second holding period, and this state is maintained during the second holding period by the holding voltage imposed after the refresh pulse voltage. Then, the state of the liquid crystal is switched from the second stable state to the third stable state by the refresh pulse voltage VRN with a pulse width t1 which is imposed at the beginning of the third holding period, and this state is maintained during the third holding period by the holding voltage imposed after the refresh pulse voltage. Thereafter, the switching between the second stable state and the third stable state, which is performed every time the refresh pulse voltage is imposed, is repeated. The switching frequency is chosen so that flicker of the display is not visible, for example, 50 Hz. At the end of all holding periods, the state of the liquid crystal is switched to a first stable state (an anti-ferroelectric state).

Next, the state of a pixel G(i,j) where it is in a condition to display a dark image will be explained referring to FIG. 15 which shows the voltages imposed thereon and transparent light intensity of an anti-ferroelectric liquid crystal. The driving voltage having the waveform as shown in FIG. 15 is imposed. In the selecting period of the first field, the anti-ferroelectric liquid crystal is in a first stable state (an anti-ferroelectric state shown by AF in FIG. 15), and this state continues during the first holding period which follows the selecting period. The state of the liquid crystal is not switched from the first stable state to the third stable state by the refresh pulse voltage VRN with a pulse width t1 which is applied at the beginning of the second holding period, and the first stable state is maintained during the second holding period by the holding voltage. Similarly, the state of the liquid crystal is not switched from the first stable state to the second stable state by the refresh pulse voltage VRP with a pulse width t1 which is applied at the beginning of the third holding period, and the first stable state is maintained during the third holding period by the holding voltage. Thereafter, the first stable state is similarly maintained without being affected by the polarity change which occurs every time the refresh pulse voltage is imposed. Also, the liquid crystal is kept in its first stable state in the eliminating period

In the second field, the anti-ferroelectric liquid crystal is in the first stable state during the selecting period, and this state is maintained during the first holding period. The state of the liquid crystal is not switched from the first stable state to the second stable state by the refresh pulse voltage VRP with a pulse width t1 which is imposed at the beginning of the second holding period, and this state is maintained during the second holding period by the holding voltage imposed after the refresh pulse voltage. Similarly, the state of the liquid crystal is not switched from the first stable state to the third stable state by the refresh pulse voltage VRN with

a pulse width t1 which is imposed at the beginning of the third holding period, and this state is maintained during the third holding period by the holding voltage imposed after the refresh pulse voltage. Thereafter, the first stable state is maintained without being affected by the polarity switching which is performed every time the refresh pulse voltage is imposed. During the eliminating period, the first stable state of the anti-ferroelectric liquid crystal is kept unchanged.

As explained above, the switching between the positive and negative ferroelectric states of the anti-ferroelectric liquid crystal is performed without changing the state of pixels which are in the anti-ferroelectric state. Therefore, the display brightness does not change and is maintained in the same level before and after the polarity change of the holding voltage. Accordingly, flicker on the display is not visible and good picture images can be attained. Also, an image contrast higher than 40 was achieved at 40° C in the embodiment according to the present invention.

The number of refresh pulse voltage impositions in one field is not necessarily limited to 8 times and can be modified to an appropriate number. The polarity of the refresh voltages imposed on a scanning electrode is chosen so that it alternates in neighboring holding periods. In this way, the anti-ferroelectric electric liquid crystal is driven by the alternating voltage, thereby preventing image stick or imprinting on the pixels.

In the embodiment disclosed herein, the polarity of the holding voltages is chosen so that neighboring scanning electrodes have an opposite polarity from each other during most of their holding periods. However, this may be modified so that neighboring scanning electrodes have an opposite polarity from each other during a period more than a half of a repeating period of the selecting period. The period during which the neighboring scanning electrodes have an opposite holding voltage polarity from each other can be decided according to the number of the refresh pulse impositions.

According to the present invention, the polarity switching frequency of the holding voltage looks higher for viewers, compared with a field reversing method. Accordingly, while attaining the advantage resulting from the imposition of the refresh pulse voltage, the flicker on the display caused by the switching of the holding voltage polarity can be prevented at the same time.

The structure of the logic circuits in the embodiment mentioned above may be replaced by programmed routines of a microprocessor.

(Second Embodiment)

A second embodiment according to the present invention will be described, referring to FIGS. 16 to 25. In the second embodiment, the polarity of the selecting voltage is not reversed every time after the eliminating period, as opposed to the first embodiment described above in which it is reversed every time after the eliminating period.

As described above, the anti-ferroelectric liquid crystal has three states, the anti-ferroelectric state (AF), a positive ferroelectric state (F+) and a negative ferroelectric state (F-). The images on the panel are displayed by switching the states of the anti-ferroelectric liquid crystal. The switchover characteristic between AF and F+ and that between AF and F- are not always the same. Namely, those characteristics may be asymmetric. If the characteristics are asymmetric, and the selecting voltage is reversed every time after the eliminating period, the flicker may occur in the display. To avoid this problem, the selecting voltage polarity in the second embodiment is not reversed for a longer time, for example, three hours or one day, using a timer installed in the control circuit 20. Other structures and operation of the second embodiment are the same as those of the first embodiment. Therefore, only the differences from the first embodiment will be described below.

FIGS. 16 and 17 (the timing chart of FIG. 16 continues to FIG. 17) show the scanning voltage applied to the scanning electrodes Y1, Y2 and Y3, based on the signals (SCC, SI01, SI02, first DP and DR) from the control circuit 20. In the timing chart, E is the eliminating period, S is the selecting period, H+ is the positive holding period, R is refreshing period, and H- is the negative holding period, all being the same as in the first embodiment. In this timing chart, the same polarity of the selecting voltage is imposed in the first four selecting periods, and its polarity is reversed in the fifth selecting period. This is only for illustrating purpose, and the same polarity of the selecting voltage is kept for a much longer time as mentioned above.

FIG. 18 shows the scanning voltage imposed on the scanning electrodes Y1, Y2 and Y3, the signal voltage on the signal electrode Xi and the brightness of the pixel G(i,1), in the same manner as in FIG. 10 of the first embodiment.

FIG. 19 shows waveforms of the voltage applied to a pixel G(i,1) at its bright state. FIG. 20 shows waveforms of the voltage applied to a pixel G(i,2) at its dark state. FIG. 21 shows waveforms of the voltage applied to a pixel G(i,3) at its bright state. These waveforms are similar to those in FIGS. 10, 11 and 12 of the first embodiment. However, in the second embodiment, the polarity of the selecting voltage imposed at the beginning of the second field is the same as that imposed at the beginning of the first field.

FIGS. 22 and 23 show waveforms of the voltage applied to a pixel G(i,j) at its bright state and dark state, respectively, in the same manner as in FIGS. 14 and 15 of the first embodiment. In FIG. 22, a selecting voltage is imposed at the beginning of the first field, and then the anti-ferroelectric liquid crystal takes the state F+ (the second stable state or the positive ferroelectric state) in the first holding period of the first field. Then, a negative refreshing voltage is imposed, thereby switch-

ing the holding voltage polarity, and the anti-ferroelectric liquid crystal takes the state F- (the third stable state or the negative state) in the second holding period of the first field. Then, the third, fourth, fifth .... holding periods follow, alternating its polarity and switching the anti-ferroelectric liquid crystal states between F+ and F-, and then the eliminating period E follows. At the beginning of the second field, a selecting voltage having the same polarity as that of the first field is imposed, and the same process as in the first field is repeated. In the dark state shown in FIG. 23, the anti-ferroelectric liquid crystal takes the state AF (anti-ferroelectric state or the first stable state) from the beginning of the first field. The state AF is not switched to F+ or F- by imposing the refresh pulse voltage as described above, and accordingly the state AF is kept through the first and second fields as shown in FIG. 23.

FIGS. 24 and 25 show timing charts similar to FIGS. 16 and 18. However, in FIGS. 24 and 25, the holding voltage is reversed three times in one field, as opposed to the charts in FIGS. 16 and 18 where the holding voltage is reversed just one time in one field. The number of holding voltage reversals in one field may be selected arbitrarily, as long as it is an odd number. As shown in FIGS. 24 and 25, the selecting voltage with the same polarity is imposed at the beginning of each field, and the holding voltage polarity of the first holding period in each field remains the same, for a predetermined period. The reversal of the selecting voltage polarity may be made by various ways other than the timer installed in the control circuit 20. For example, it can be made at a time when power supply to the device starts or when a screen saver for the display panel 10 is operated.

Since the anti-ferroelectric state of the anti-ferroelectric liquid crystal is switched to the same polarity of ferroelectric state for a predetermined long period in the second embodiment, the flicker on the display is further reduced and becomes invisible even when the anti-ferroelectric liquid crystal has an asymmetric switchover characteristic.

(Third Embodiment)

Referring to FIGS. 26 to 37, a third embodiment according to the present invention will be described. In the third embodiment, interlaced scanning is employed in which the scanning electrodes are scanned by jumping one or more neighboring scanning electrodes) in addition to the features of the first and/or second embodiment. Since the most structures and operation of the third embodiment are similar to those of the first or second embodiment, only the specific features of the third embodiment will be described below.

FIG. 26 shows a whole structure of a liquid crystal display device, in which a control circuit 20A and a scanning electrode driving circuit 50A are used in place of the control circuit 20 and the scanning electrode driving circuit 50 of the first embodiment. The control circuit 20A delivers output signals: the first and second DPs, DR, SCC, LCK, STD and SIC (same as output signals of the control circuit 20); SI01a and SI02a (in place of SI01 and SI02 of the control circuit 20); and ACK (an additional signal). The signals SI01a and SI02a decide the condition of the scanning electrodes in the same manner as in the first embodiment, though the waveforms of SI01a and SI02b are different from those of SI01 and SI02. That is, a period when both SI01a and SI02a are L (low) corresponds to the eliminating period (E); a period when SI01a is H (high) and SI02a is L corresponds to the selecting period (S); a period when both SI01a and SI02a are H corresponds to the holding period (H); and a period when SI01a is L and SI02a is H corresponds to the refreshing period (R).

The scanning electrode driving circuit 50A imposes voltages on the scanning electrodes Y1, Y2, Y3 ... in the interlaced fashion by selecting the seven voltages from the power source circuit 30. In this particular embodiment, the interlaced scanning is performed by jumping two scanning electrodes.

The operation of the scanning electrode driving circuit 50A will be described, taking the scanning electrode Y1 as an example. FIG. 29 shows scanning voltages imposed on the scanning electrodes together with the input signals to the scanning electrode driving circuit 50A in the similar manner as in FIG. 6. In FIG. 29 and following drawings, the selecting period is shown by S+ (positive) or S- (negative), the holding period by H+ or H-, the refreshing period by R+ or R-, the eliminating period by RS+ or RS-. The selecting period is divided into three periods, the first, second and third periods. In the positive selecting period (S+), voltage VE is imposed in the first period, voltage VHP in the second period, and voltage VWP in the third period. In the negative selecting period (S-), voltage VE is imposed in the first period, voltage VHN in the second period and voltage VWN in the third period. In the positive eliminating period (RS+), voltage VWP is imposed at the beginning and then voltage VE follows. In the negative eliminating period (RS-), voltage VWN is imposed at the beginning and then voltage VE follows. The scanning electrode driving circuit 50A operates in the substantially same manner as in scanning electrode driving circuit 50 except for the points mentioned above.

FIG. 30 shows the scanning voltages imposed on each scanning electrode, Y1, Y2, Y3, Y4, Y5 .... and so forth. Since the interlaced scanning which jumps two neighboring electrodes is employed in this embodiment, the scanning electrode Y1 is first scanned, and then Y4, Y7, Y10 ... are scanned in this order in a staggered manner by delaying one selecting period for each electrode scanned. Also, selecting voltage polarity is reversed for each electrode scanned. After a first series of scanning is completed to the bottom, a second series of scanning starts from the electrode Y2, and then Y5, Y8, Y11 ... are scanned in this order. Then, the third

series of scanning starts from the scanning electrode Y3, and then Y6, Y9, Y12 ... are scanned in this order. One picture frame is completed when all the scanning electrodes are thus scanned. Then, scanning for the next picture frame is repeated from the scanning electrode Y1 with a reversed polarity.

Referring to FIGS. 27 and 28, the structure of the scanning electrode driving circuit 50A, which is similar to that of the scanning electrode driving circuit 50 shown in FIG. 4, will be described. The 2-bit registers RY1, RY2 ... RYn in FIG. 4 are replaced by 2-bit registers RY'1, RY'2 ... RY'n; signals SI01, SI02 are replaced by signals SI01a, SI02a; and signal ACK is added in this embodiment, as shown in FIG. 27. The 2-bit registers RY'1 to RY'n sequentially receive the signals SI01a, SI02a from the control circuit 20A in synchronism with the rising edge of the ACK signal and output 2-bit data (bit-1 and bit-2) to the decoders DY1 to DYn in synchronism with the rising edge of the SCC signal.

Details of the 2-bit registers RY'1 to RY'n are shown in FIG. 28. The structure of the 2-bit registers will be described, taking the 2-bit registers RY'1 and RY'2 as examples. The 2-bit register RY'1 is composed of a pair of D-type flip-flops Fa, Fb constituting an 1-bit and a pair of D-type flip-flops Fc, Fd constituting another 1-bit. The flip-flops Fb, Fd receive the signals SI01a, SI02a, respectively, in synchronism with the rising of the ACK signal, and deliver their outputs from respective Q terminals to the flip-flops Fa, Fc, respectively. The flip-flops Fa, Fc receive the outputs from the flip-flops Fb, Fd, respectively, in synchronism with the rising of the SCC signal, and deliver their outputs to the decoder DY1 as the 2-bit data (bit-1 and bit-2). Similarly, the 2-bit register RY'2 is composed of a pair of D-type flip-flops Fa, Fb and another pair of D-type flip-flops Fc, Fd. The flip-flops Fb, Fd of RY'2 receive the outputs from respective Q terminals of the flip-flops Fb, Fd of RY'1, respectively, in synchronism with the rising of the ACK signal, and deliver their outputs from respective Q terminals to the flip-flops Fa, Fc of RY'2, respectively. The flip-flops Fa, Fc of RY'2 receive the outputs from the flip-flops Fb, Fd of RY'2, respectively, in synchronism with the rising of the SCC signal, and deliver their outputs to the decoder DY2 as 2-bit data (bit-1 and bit-2). Other 2-bit registers RY'3 to RY'n operate in the same manner and deliver their outputs as the 2-bit data to DY3 to DYn, respectively. The decoders DY1 to DYn generate seven signals for operating the analog switches WY1 to WYn, based on the 2-bit data from the 2-bit registers RY'1 to RY'n, the first DP signal from the control circuit 20A and the DR signal from the control circuit 20A in the similar manner as in the first embodiment.

The structure of the decoders DY1 to DYn used in the third embodiment is the same as that of the first embodiment (shown in FIG. 5). The decoders DY1 to DYn operate in the same manner as in the first embodiment, except that the signals SI01, SI02 of the first embodiment are replaced by the signals SI01a and SI02a. Thus, the scanning voltages shown in FIG. 29 and described above are supplied to the scanning electrodes from the scanning electrode driving circuit 50A. Since one clock of the ACC signal corresponds to three clocks of the ACK signal in the third embodiment, the interlaced scanning is performed by jumping two scanning electrodes according to the signals SI01a and SI02a, as shown in FIG. 30.

The signal electrode driving circuit 60 operates in the same manner as in the first embodiment, because it operates based on the second DP, LCK, STD and SIC signals fed from the control circuit 20A, all of which are identical to those of the first embodiment. Therefore, the signal voltages are imposed on the signal electrodes with timing shown in FIG. 31, in which the signal voltages imposed on the signal electrode X1 are shown as an example.

An example of the operation of the liquid crystal display device according to the third embodiment will be described below, referring to FIGS. 32, 33 and 34. In this particular example, the frame display frequency is 20 Hz (the display period of one-frame is 50 ms), the number of the row electrodes (scanning electrodes) is 1024, the number of the column electrodes (signal electrodes) is 3840, scanning duty is 1/N (N = 512), and the eliminating period E (E = 12). FIG. 32 shows voltages imposed on a pixel G(i,j) and the light transparency (transparent light intensity) of the same pixel, when the pixel in the bright state maintains the same bright state after the eliminating period. FIG. 33 shows the same when the pixel in the bright state changes its state to the intermediate state after the eliminating period. FIG. 34 shows the same when the pixel in the bright state changes its state to the dark state after the eliminating period. The holding voltage polarity is reversed at a frequency higher than 30 Hz.

In the positive selecting period (S+), voltage VE having width t1 (t1 = 32.6 μs) is imposed first, and then voltage VHP having pulse width t2 (t2 = 32.6 μs) and voltage VWP having pulse width t2 are sequentially imposed as the selecting voltage. The pulse width t1, t2 corresponds to that of the first embodiment shown in FIG. 11 but is a little shorter than that. Then, the holding voltage VHP is imposed during the holding period (H+). In the refreshing period (R-) which starts after 9.7 ms counting from the beginning of the selecting period (S+), refresh voltage VRN having pulse width t1 is imposed. Then holding voltage VHN is imposed during the holding period (H-) which ends after a lapse of 9.7 ms counting from the beginning of the refreshing period (R-). In the following refreshing period (R+), refreshing voltage VRP having pulse width t1 is imposed, and then holding voltage VHP is imposed during the holding period (H+) which is 9.7 ms counting from the beginning of the refreshing period (R+). Thereafter, the same process is repeated up to the end of the Pth holding period (P = 5 in this particular example). The length of the first field from the beginning of the selecting period

(S+) to the end of the 5th holding period is (N-E) • (t1+2 • t2) . At the end of the 5th holding period, voltage VWN having pulse width t1 is imposed and then voltage VE is imposed for a period of E • (t1+2 • t2)-t1 for eliminating the images written on the pixel G(i,j).

In the following selecting period (S-), voltages VE, VHN and VWN, are sequentially imposed in this order on the scanning electrode, thereby starting the second field. Thereafter, the same process described in the first field is repeated.

To display a bright image in the first field, voltage VG of pulse width t1, voltage V8 of pulse width t2 and voltage V1 of pulse width t2 are sequentially imposed on the signal electrode in the selecting period. To display a dark image in the first field, voltage VG of pulse width t1, voltage V1 of pulse width t2 and voltage V8 of pulse width t2 are sequentially imposed on the signal electrode in the selecting period. Conversely, to display a bright image in the second field, voltage VG of pulse width t1, voltage V1 of pulse width t2 and voltage V8 of pulse width t2 are imposed in this order. To display a dark image in the second field, voltage VG of pulse width t1, voltage V8 of pulse width t2 and voltage V1 of pulse width t2 are imposed in this order. To display an intermediate brightness, intermediate voltages V2 to V7 are selected. The refreshing voltage is imposed on the scanning electrode in synchronism with voltage VG on the signal electrode. Therefore, the level of the refreshing pulse, VRP or VRN, is not affected by the level of the signal voltage, and the brightness before and after the holding voltage polarity is reversed is kept unchanged, in the same manner as in the first embodiment.

In the eliminating period, the bright image or the intermediate image is eliminated, namely, the pixel is brought to the dark state. The brightness change caused by the elimination is about 2% of the average brightness of one field. This change may be observed as a flicker having a frequency of the frame display frequency (20 Hz in the example described above) when the sequential scanning is employed. When the interlaced scanning is employed as in the third embodiment, the flicker frequency is increased (three times of the frame display frequency in the example described above, that is, 60 Hz). Therefore, the flicker can be made invisible. This will be further explained with reference to FIGS. 35A and 35B.

FIG. 35A shows the sequential scanning in which the scanning electrodes are scanned from the top to the bottom without jumping any electrode. The average brightness changes with the same frequency as the frame frequency of 20 Hz, as shown in the right graph, which can be observed by a viewer. FIG. 35B shows the interlaced scanning in which the scanning electrodes are scanned by jumping two electrodes (n = 2) as in the third embodiment described above. In this case, the average brightness changes with a frequency three times higher than the frame frequency, that is, 60 Hz which is not observed as the flicker. The display contrast of the third embodiment is about 40 at a temperature of 40 °C, and no flicker is observed. Relation between the number (n) of electrodes jumped under the interlaced scanning and the flicker is shown in FIG. 36. The scrolling flicker is also shown in the chart. The flicker and the scrolling flicker are checked by taking the average brightness change as a parameter. The flicker under the sequential scanning is also checked for comparison purpose. It is seen from the chart that the flicker is visible when the average brightness change is higher than 2% under the sequential scanning. Under the interlaced scanning (n = 1), the flicker is observed when the average brightness change is higher than 5%. Under the interlaced scanning (n = 2), the flicker is not visible but the scrolling stripe (this will be explained below using separate drawings) is observed when the average brightness change is 10%. Under the interlaced scanning (n = 3), the scrolling stripe is observed when the average brightness is higher than 5%. Under the interlaced scanning (n = 4) the scrolling stripe is observed when the average brightness change is higher than 2%. It is concluded from the above that the optimum number (n) is 2. However, the results shown in the chart are obtained by viewing the panel at a distance of 5 cm from the panel, and the scrolling flicker becomes more invisible when the panel is viewed at a farther distance. Therefore, the number n can be higher than 2 in practical use.

Referring to FIGS. 37A, 37B and 37C, details of the scrolling stripe will be explained. A stripe having width Ls appears on the upper portion of the panel at time T1 as shown in FIG. 37A and moves downward. It is seen at the position shown in FIG. 37B at time T2 and further moves down, and is seen at the position shown in FIG. 37C at time T3. The scrolling stripe does not always move downward, but it may move upward, depending on the viewer's position or the direction of eye movement. As the width Ls becomes narrower, the stripe becomes difficult to be observed. Also, it becomes more invisible as the distance from a viewer to the panel becomes larger. When the width Ls is narrower than 5 mm, and the distance from a viewer to the panel is in a range from 20 cm to 60 cm (a normal distance), the scrolling stripe is usually invisible.

The features of each embodiment described above (the first, second or third embodiment) may be used alone or in combination with the features of other embodiments. Though the anti-ferroelectric liquid crystal is used in the embodiments, other liquid crystals such as smectic liquid crystal having characteristics similar to the anti-ferroelectric liquid crystal may be used.

While the present invention has been shown and described with reference to the foregoing preferred embodiments, it will be apparent to those skilled in the art that changes in form and detail may be made therein without departing from the scope of the invention as defined in the appended claims.

Claims

1. A liquid crystal display device comprising:

   a liquid crystal display panel (10) having n×m pixels constituted by a matrix electrode structure having n stripes of scanning electrodes (Y1 to Yn) and m stripes of signal electrodes (X1 to Xm), and a liquid crystal (10c) interposed between the scanning electrodes and the signal electrodes;
   scanning electrode driving means (20, 20A, 30, 50, 50A) for imposing scanning voltages on the scanning electrodes, the means providing a selecting period (S) in which a selecting voltage is imposed and picture images are written on the pixels, a holding period (H) in which the picture images are maintained by a holding voltage, a polarity of which is reversed at least one time, and an eliminating period (E, RS) in which the picture images on the pixels are eliminated, the selecting, holding and eliminating periods constituting one scanning filed; and
   signal electrode driving means (20, 20A, 40, 60) for imposing signal voltages representing the picture images sequentially on the signal electrodes in synchronism with the scanning voltages, thereby displaying picture images on the display panel; wherein:
   a refresh pulse voltage is imposed on the scanning electrodes at the time the polarity of the holding voltage is reversed; and
   the scanning voltages are imposed on the scanning electrodes in an interlaced fashion by jumping at least one neighboring scanning electrode.

2. The liquid crystal display device as in claim 1, wherein:

   the liquid crystal (10c) is an anti-ferroelectric liquid crystal which exhibits an anti-ferroelectric state (AF), a positive ferroelectric state (F+) and a negative ferroelectric state (F-) according to voltages imposed thereon; and
   the refresh pulse voltage imposed on the scanning electrodes has such a level and a duration that the refresh pulse voltage causes transition between the positive (F+) and negative (F-) ferroelectric states but does not cause transition from the anti-ferroelectric state (AF) to either of the ferroelectric states (F+, F-).

3. The liquid crystal display device as in claim 1 or 2, wherein:

   the interlaced scanning is performed by jumping such number of neighboring scanning electrodes that makes flicker on the display practically invisible in relation to a frequency of the scanning.

4. The liquid crystal display device as in claim 3, wherein:

   the number of scanning electrodes jumped in the interlaced scanning is in a range from 2 to 4.

5. The liquid crystal display device as in claim 1 or 2, wherein:

   the eliminating period (E, RS) is shorter than 10% of a duration of the one scanning field.

6. The liquid crystal display device as in claim 1 or 2, wherein:

   a distance of the scanning electrodes which are jumped in the interlaced scanning is selected so that scrolling stripes on the display are practically invisible.

7. The liquid crystal display device as in claim 6, wherein:

   the distance of the scanning electrodes which are jumped in the interlaced scanning is less than 5 mm.

8. The liquid crystal display device as in claim 1 or 2, wherein:

   the polarities of the holding voltages imposed on neighboring scanning electrodes are opposite to each other during a period more than a half of the one scanning field.

9. The liquid crystal display device as in claim 1 or 2, wherein:

   the refresh pulse voltage is imposed on the scanning electrodes at the time the signal voltage imposed on the signal electrodes is at a base level (VG).

10. The liquid crystal display device as in claim 1 or 2, wherein:

    the polarity of the selecting voltage imposed on the scanning electrodes in the selecting period is reversed every field.

11. The liquid crystal display device as in claim 1 or 2, wherein:

the polarity of the selecting voltage imposed on the scanning electrodes in the selecting period is reversed every plurality of fields.

12. The liquid crystal display device as in claim 1 or 2, wherein:

the polarity of the selecting voltage imposed on the scanning electrodes in the selecting period is reversed every time power supply to the display device newly commences.

13. The liquid crystal display device as in claim 1 or 2, wherein:

the polarity of the selecting voltage imposed on the scanning electrodes in the selecting period is reversed every time a screen saver becomes in operation.

14. The liquid crystal display device as in claim 1 or 2, wherein:

the polarity of the holding voltage is reversed odd number of times in the one scanning field.

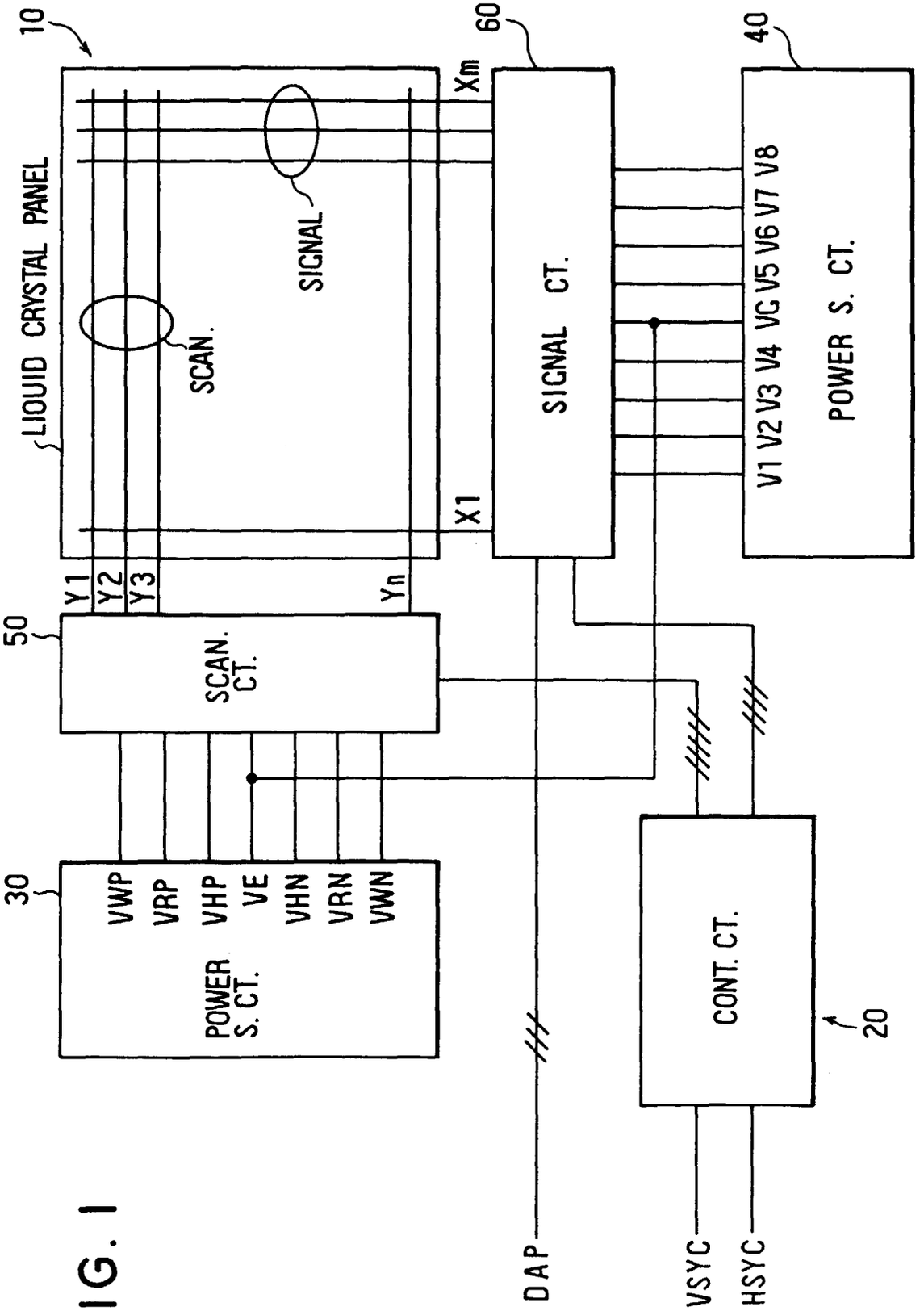

10
LIQUID CRYSTAL PANEL
SCAN.
SIGNAL
Xm
X1
Y1
Y2
Y3
Yn
60
SIGNAL CT.
40
POWER S. CT.
V1 V2 V3 V4 VC V5 V6 V7 V8
50
SCAN. CT.
30
POWER S. CT.
VWP
VRP
VHP
VE
VHN
VRN
VWN
CONT. CT.
20
DAP
VSYC
HSYC

FIG. 1

FIG. 2

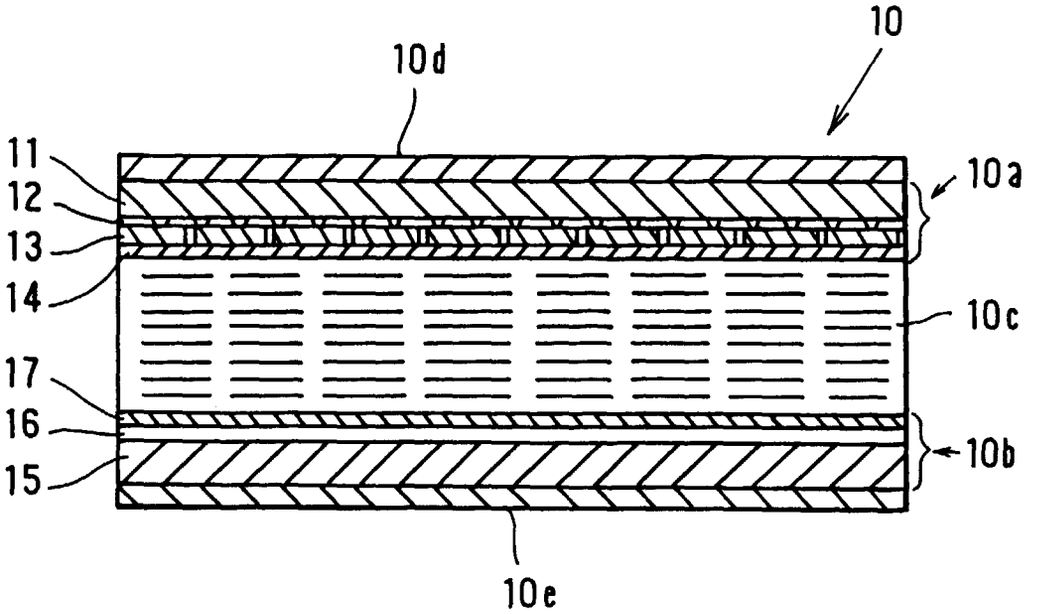

10
10d
11
12
13
14
17
16
15
10a
10c
10b
10e

FIG. 3

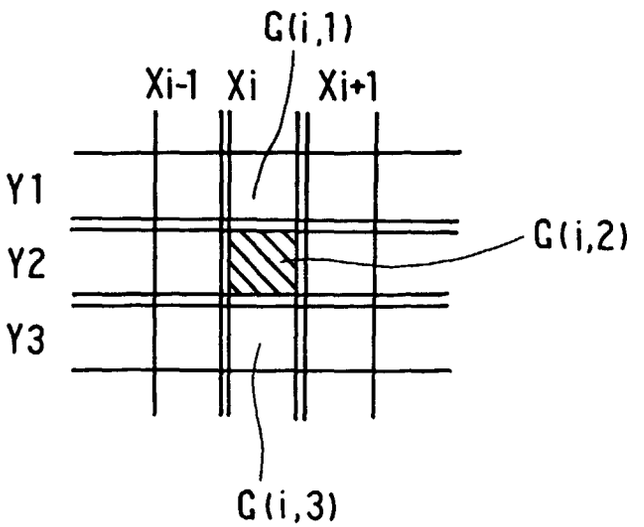

G(i,1)
Xi-1
Xi
Xi+1
Y1
Y2
Y3
G(i,2)
G(i,3)

FIG. 4

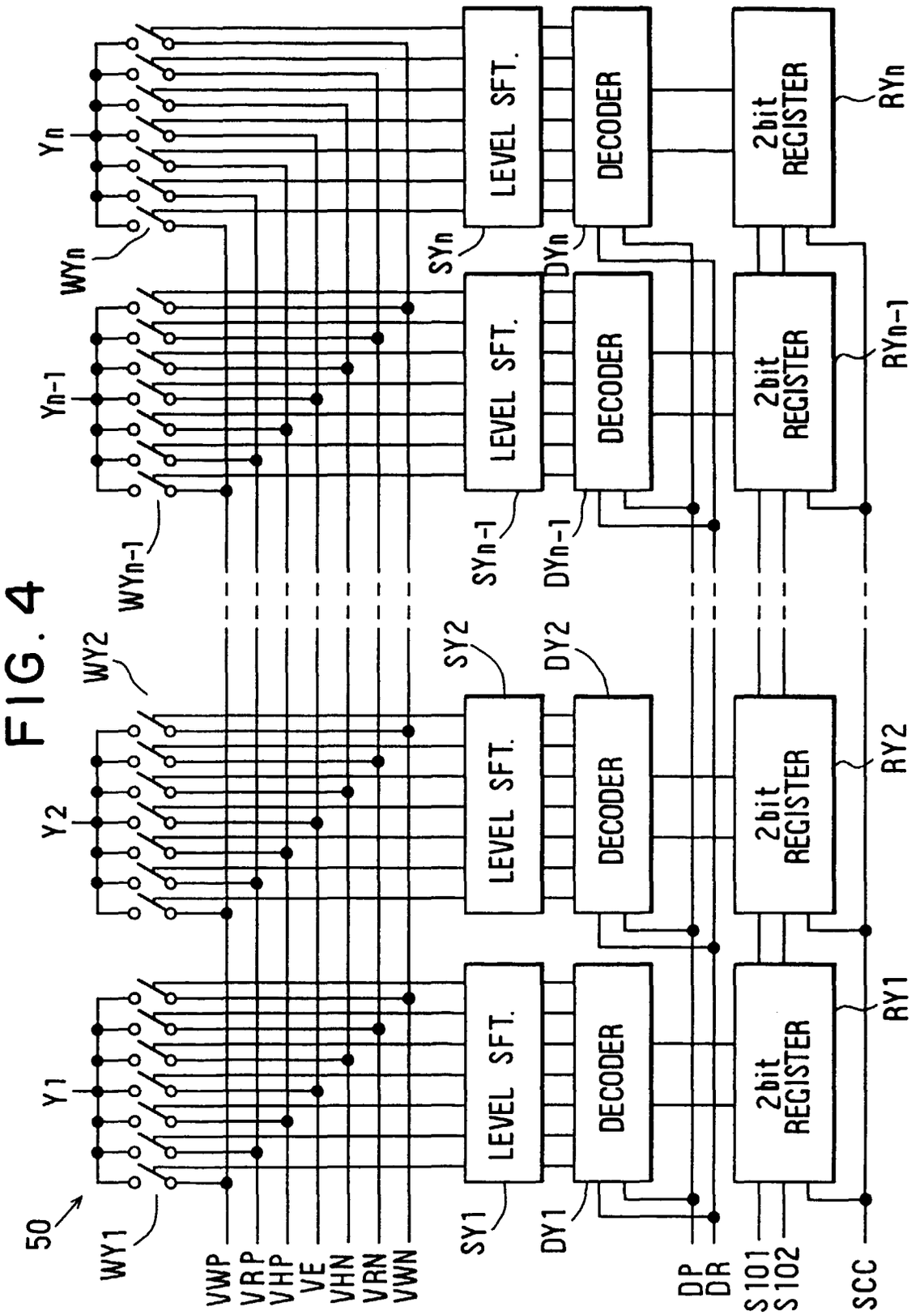

50
WY1
WY2
WYn-1
WYn
Y1
Y2
Yn-1
Yn
VWP
VRP
VHP
VE
VHN
VRN
VWN
LEVEL SFT.
DECODER
2bit REGISTER
SY1
SY2
SYn-1
SYn
DY1
DY2
DYn-1
DYn
RY1
RY2
RYn-1
RYn
DP
DR
S101
S102
SCC

FIG. 5

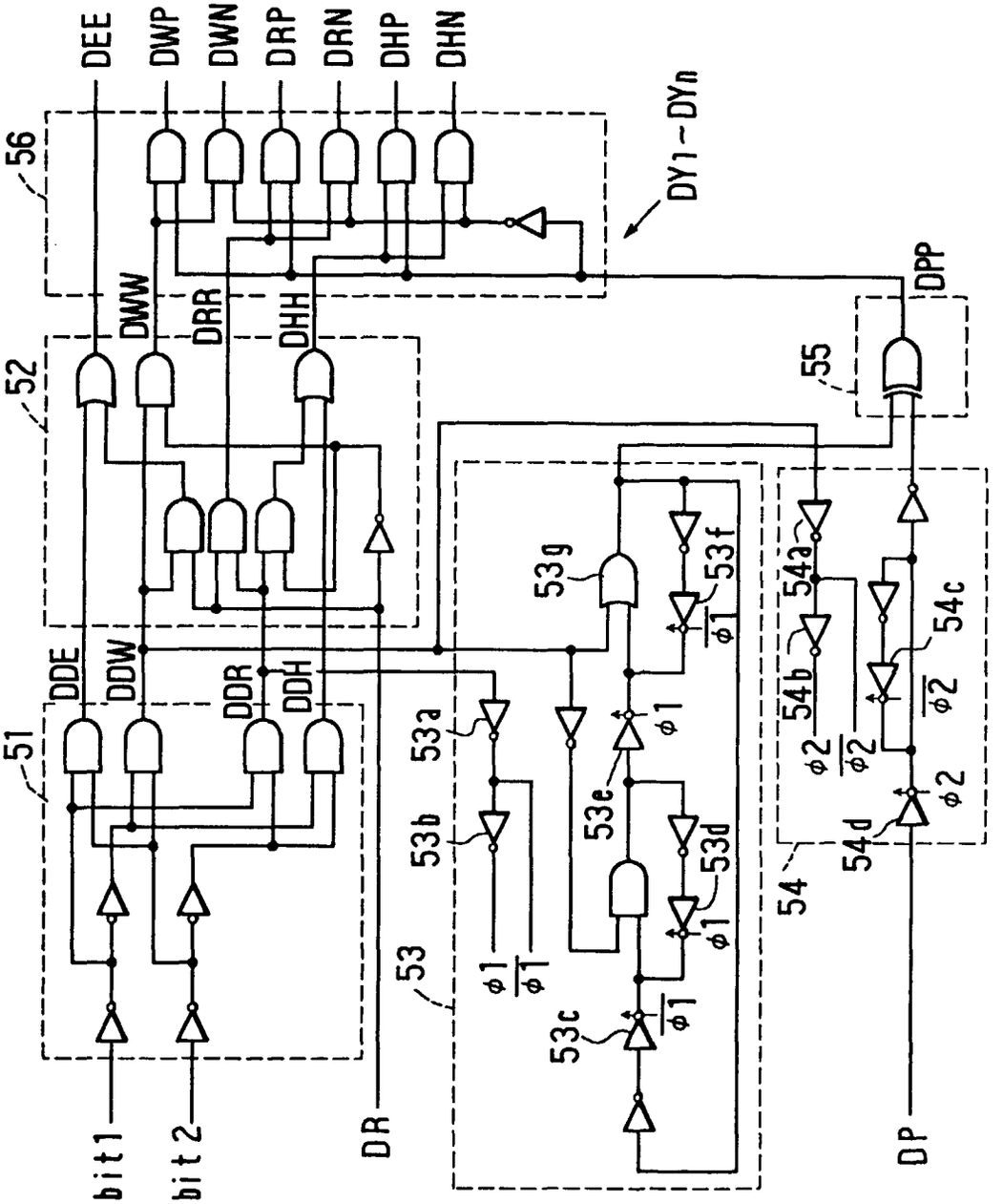

DEE
DWP
DWN
DRP
DRN
DHP
DHN
56
DY1-DYn
DPP
55
DWW
DRR
DHH
52
DDE
DDW
DDR
DDH
51
53g
53f
53a
53b
53e
53d
53c
53
54a
54b
54c
54d
54
bit1
bit2
DR
DP

FIG. 6

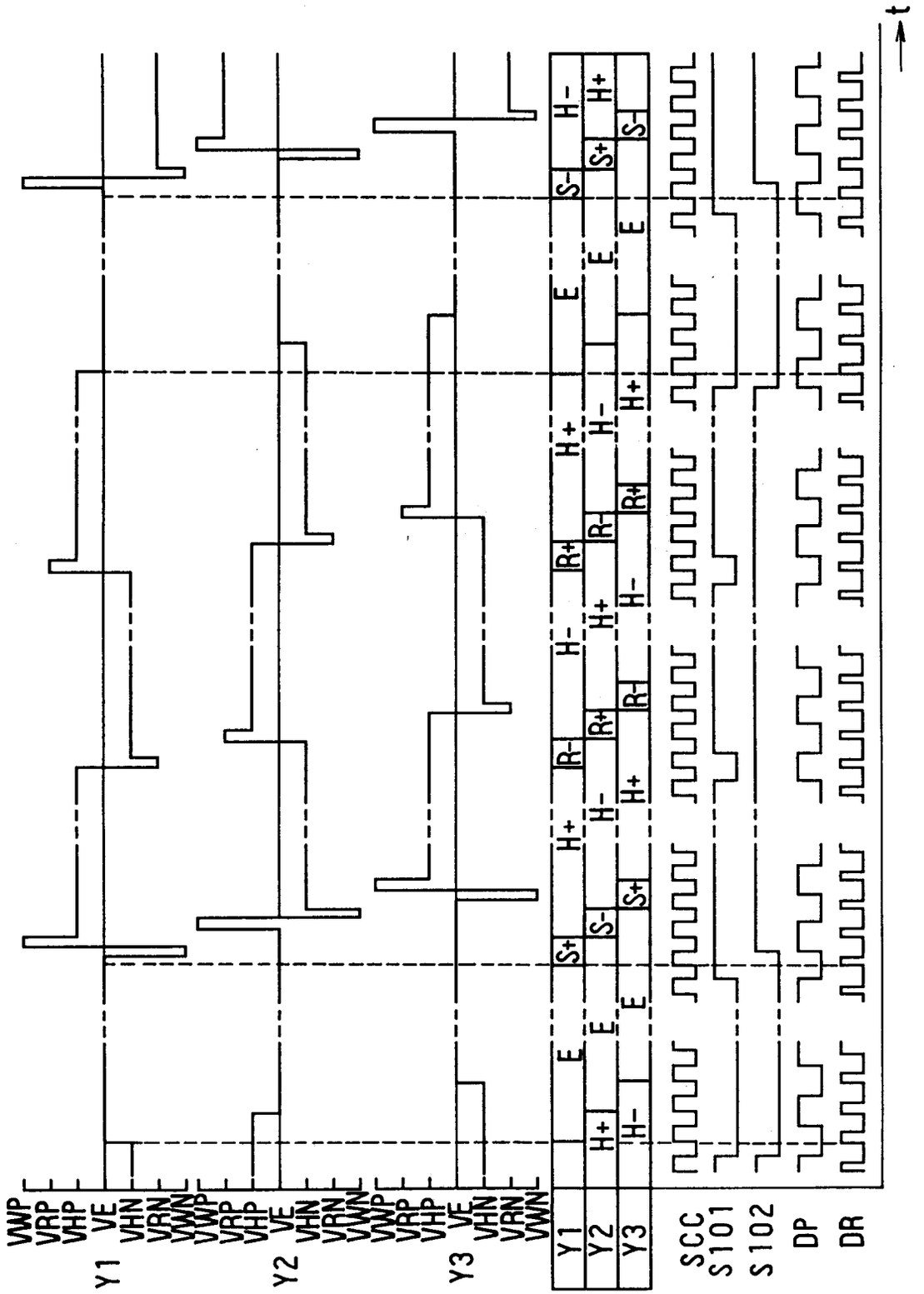


FIG. 7

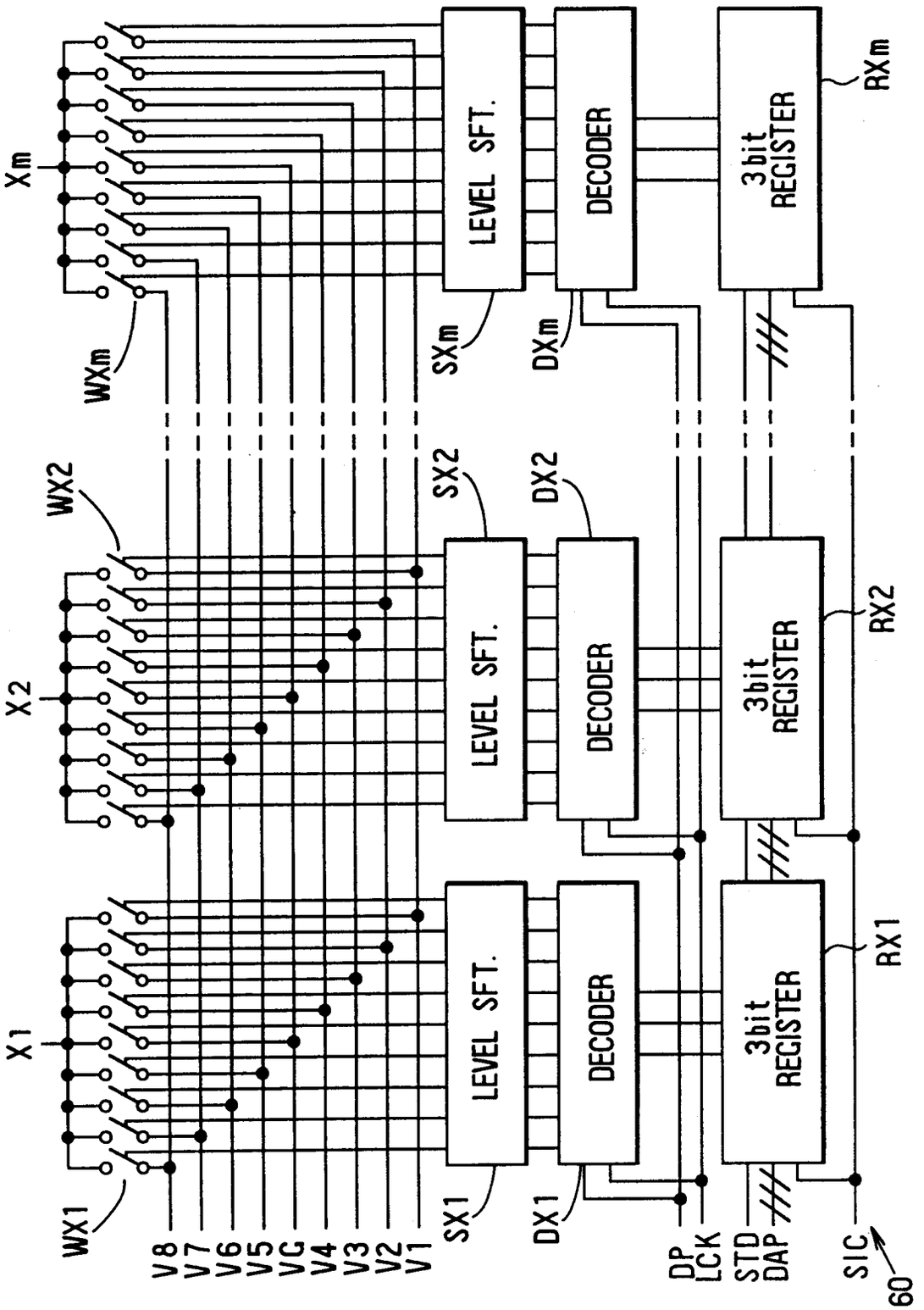

Xm
WXm
LEVEL SFT.
DECODER
3bit REGISTER
RXm
SXm
DXm
X2
WX2
SX2
DX2
RX2
X1
WX1
SX1
DX1
RX1
V8
V7
V6
V5
VC
V4
V3
V2
V1
DP
LCK
STD
DAP
SIC
60

FIG. 8

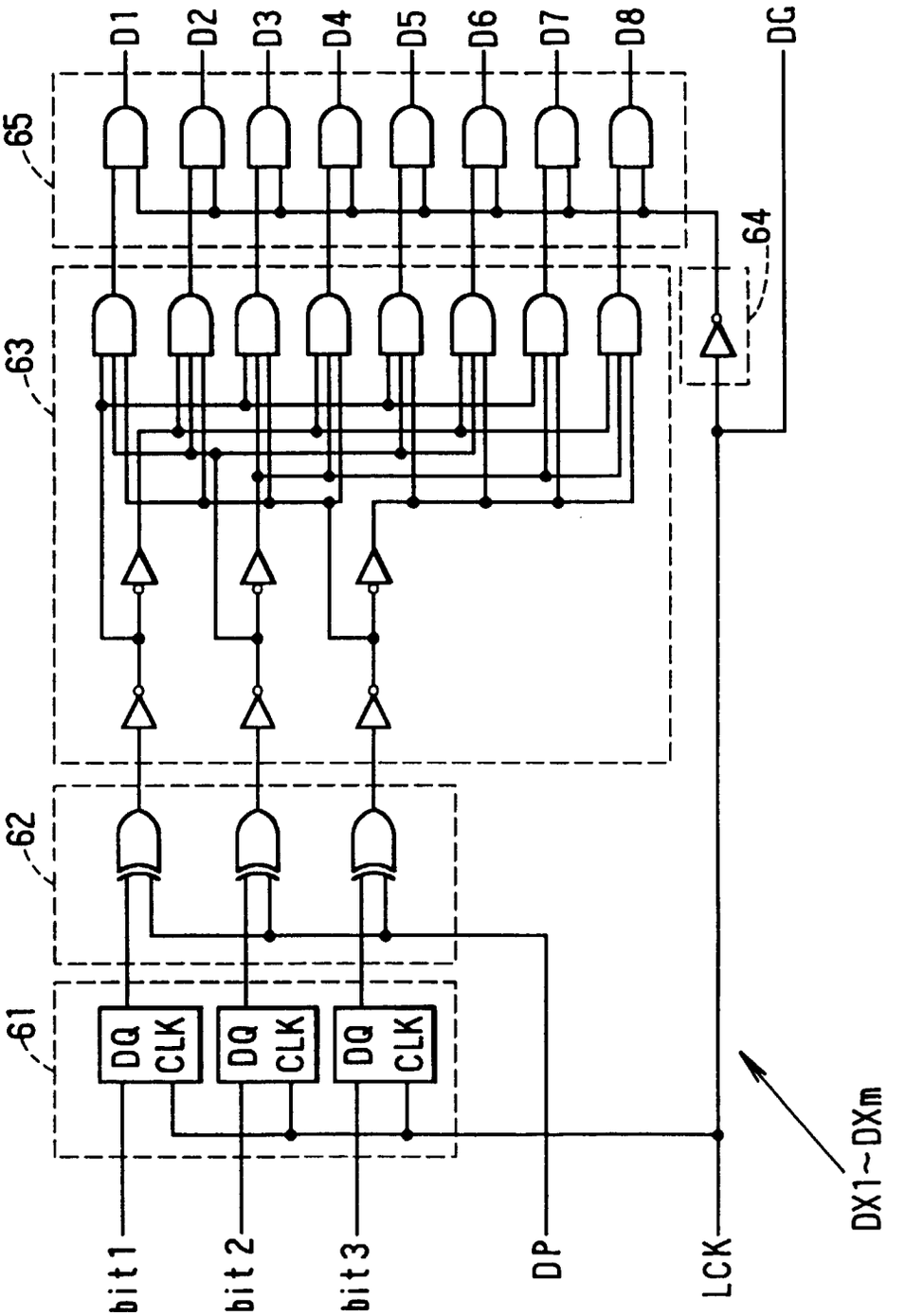

D1
D2
D3
D4
D5
D6
D7
D8
DC
65
64
63
62
61
DQ
CLK
bit1
bit2
bit3
DP
LCK
DX1~DXm

FIG. 9

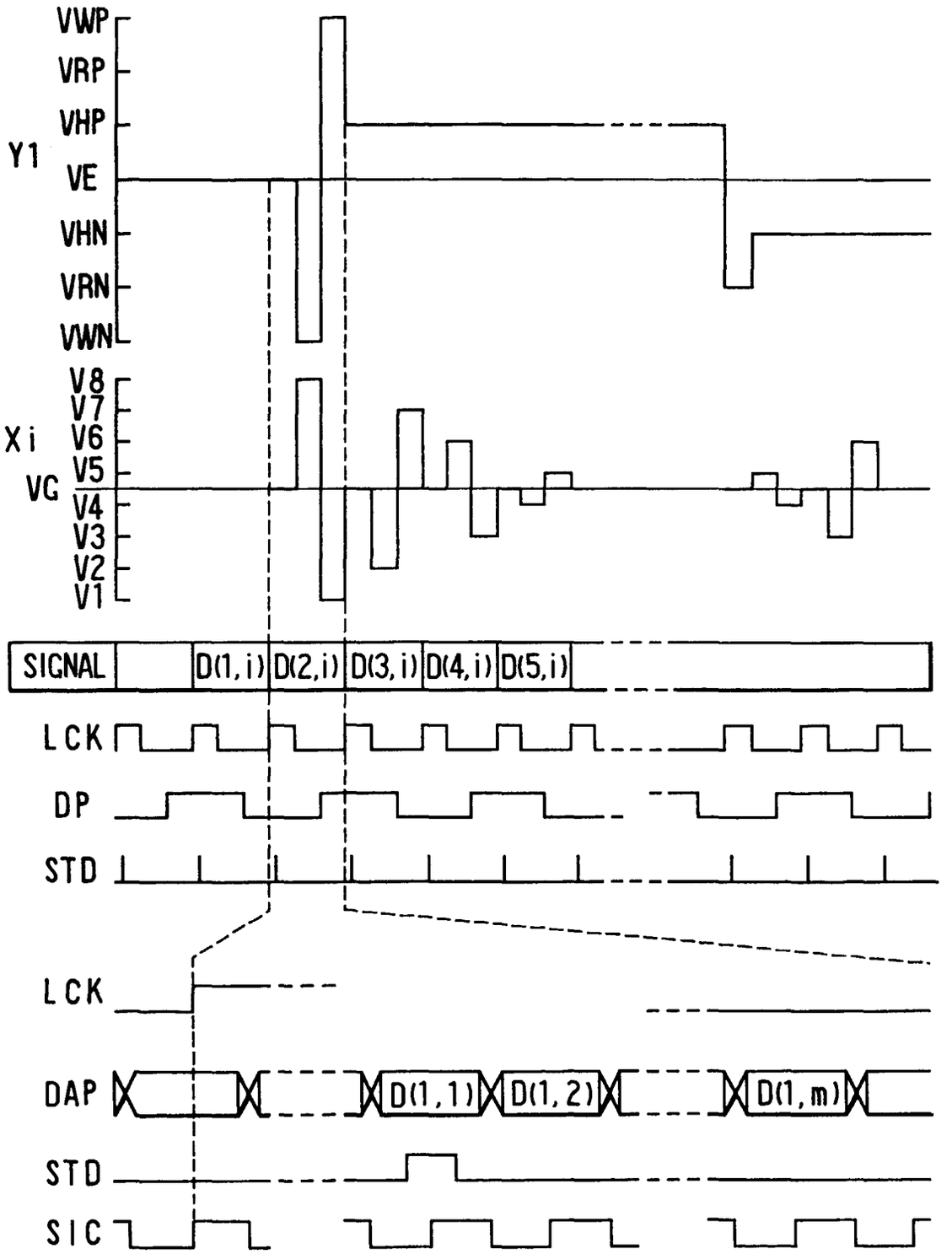

VWP
VRP
VHP
Y1
VE
VHN
VRN
VWN
V8
V7
Xi
V6
V5
VG
V4
V3
V2
V1
SIGNAL
D(1,i)
D(2,i)
D(3,i)
D(4,i)
D(5,i)
LCK
DP
STD
LCK
DAP
D(1,1)
D(1,2)
D(1,m)
STD
SIC

FIG. 10

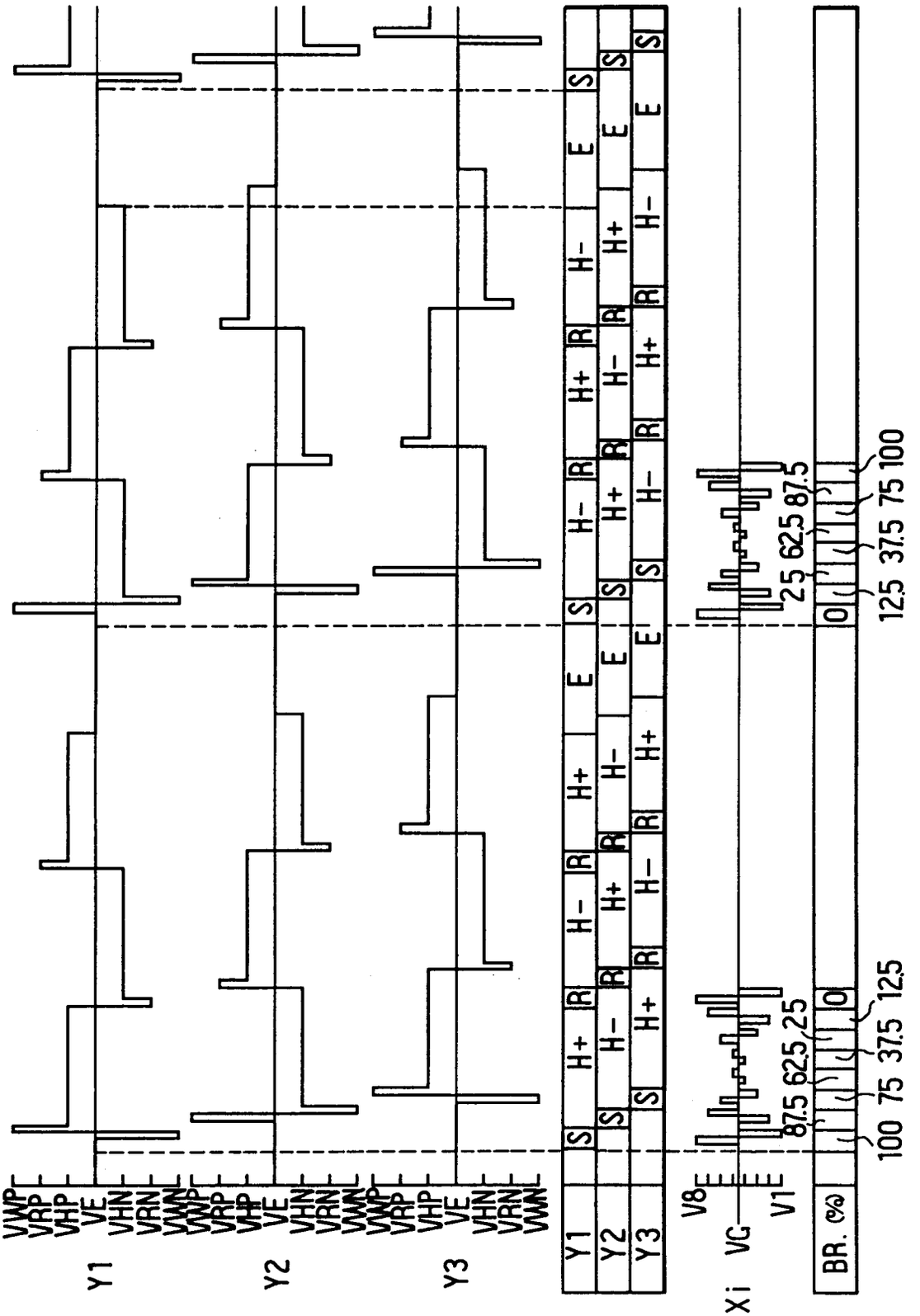

VWP
VRP
VHP
VE
VHN
VRN
VWN
Y1
Y2
Y3
S
R
E
H+
H−
V8
VG
V1
Xi
BR. (%)
100 75 37.5 12.5
87.5 62.5 25
25 62.5 87.5
12.5 37.5 75 100

FIG. 11

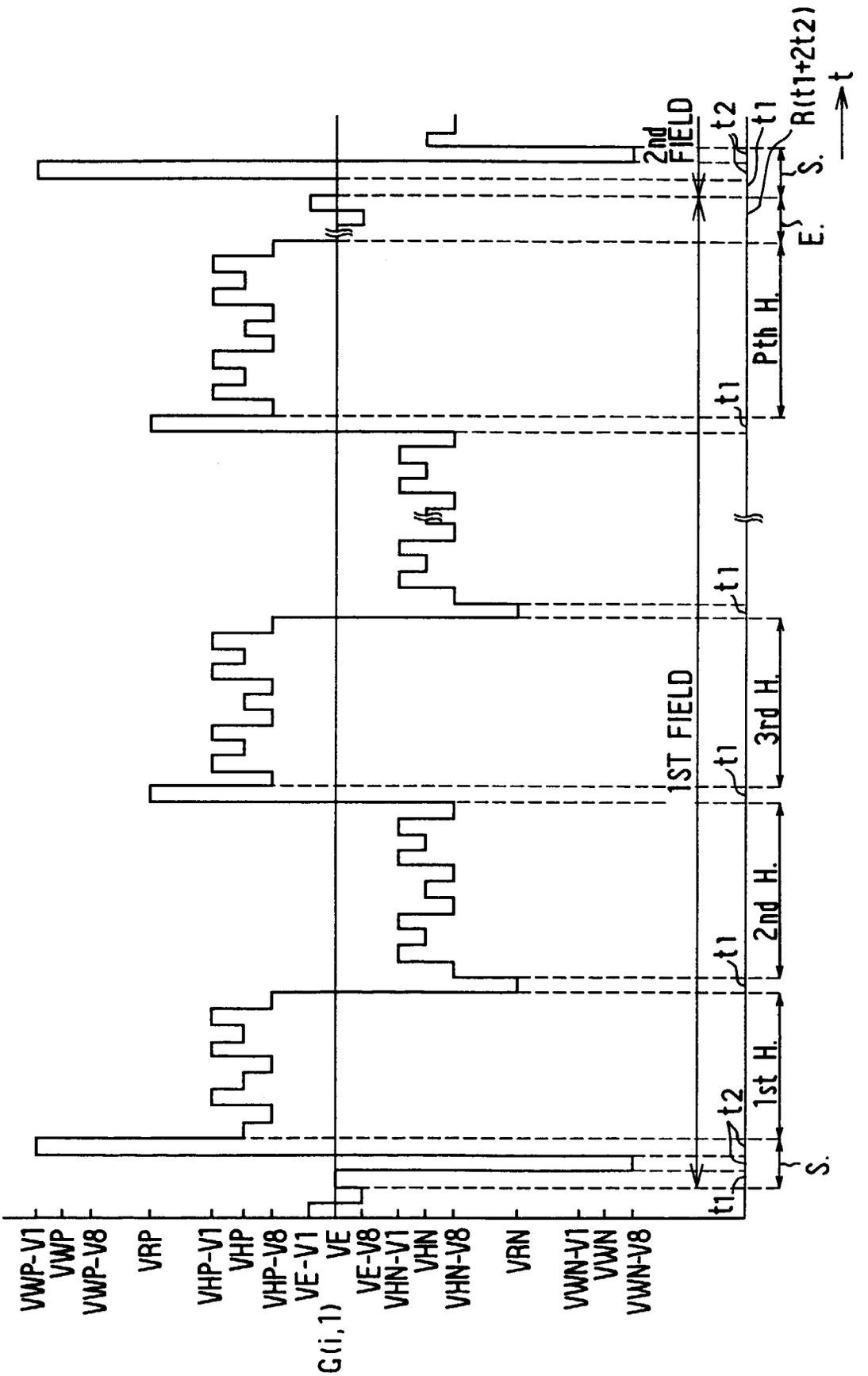

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
G(i,1)
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
1ST FIELD
2nd FIELD
1st H.
2nd H.
3rd H.
Pth H.
t1
t2
S.
E.
R(t1+2t2)
t

FIG. 12

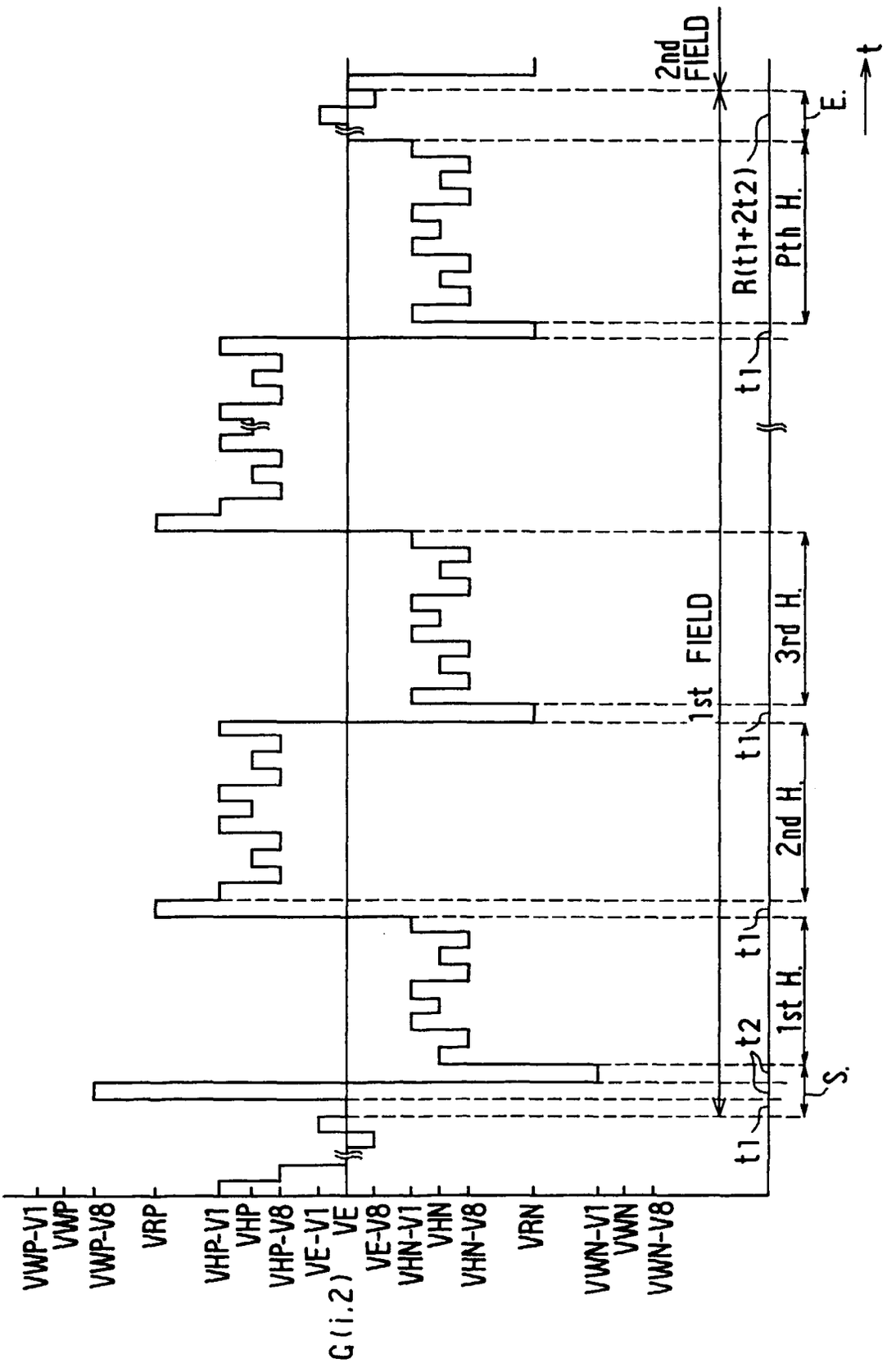

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
G(i,2)
t1
t2
S.
1st H.
2nd H.
3rd H.
Pth H.
E.
R(t1+2t2)
1st FIELD
2nd FIELD
t

FIG. 13

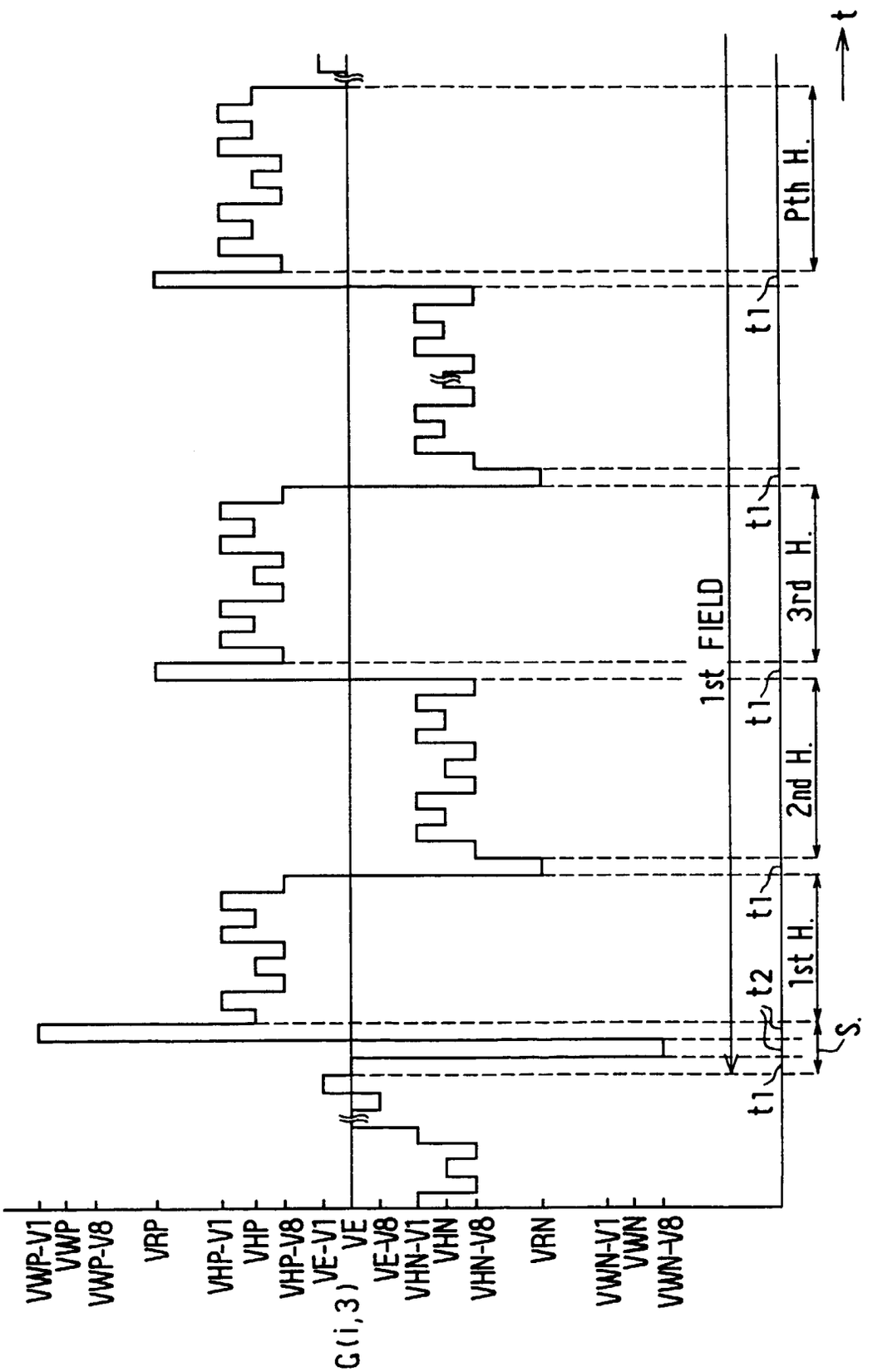

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
G(i,3)
t
t1
t2
S.
1st H.
2nd H.
3rd H.
Pth H.
1st FIELD

FIG. 14

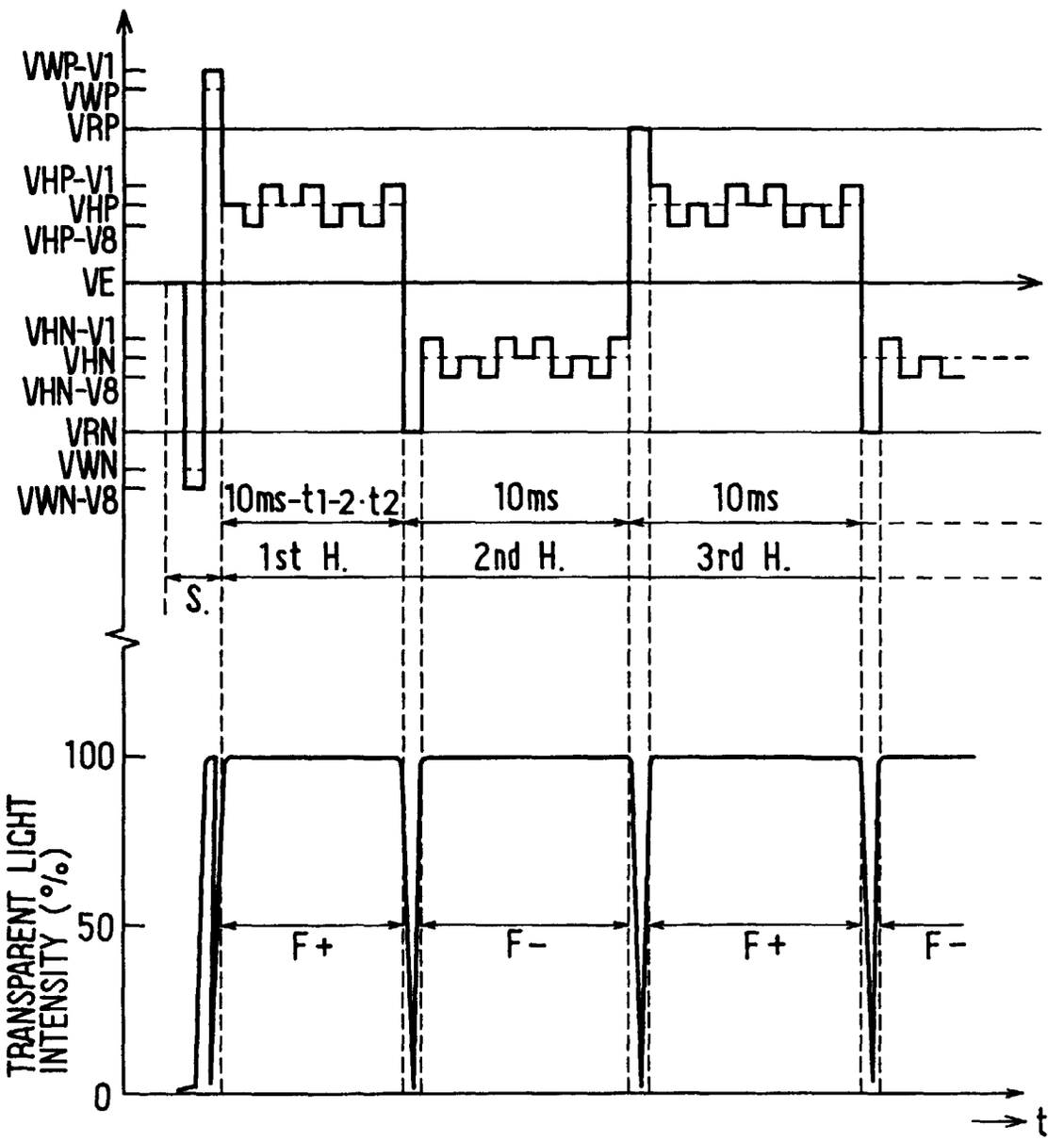
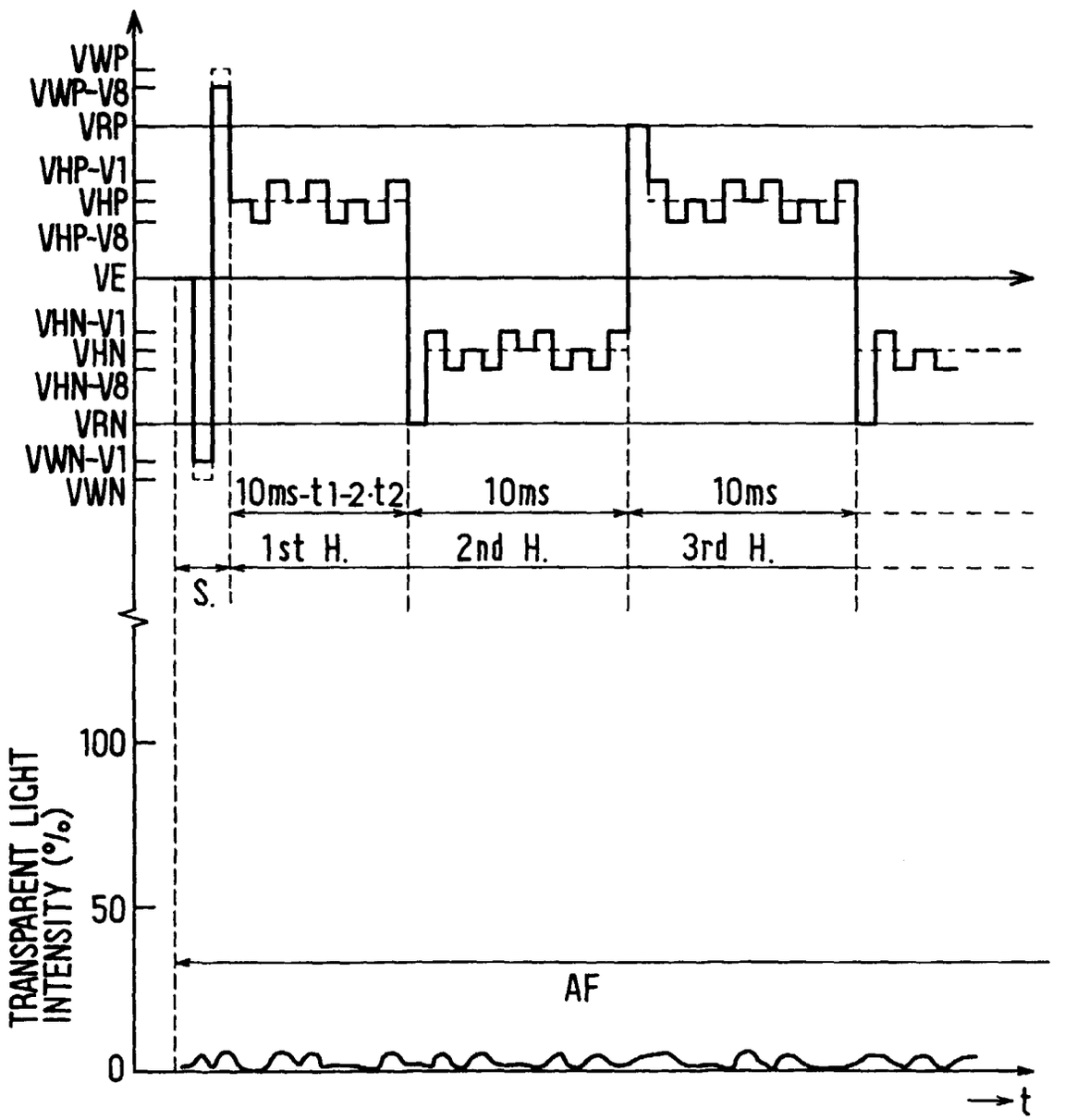

VWP-V1
VWP
VRP
VHP-V1
VHP
VHP-V8
VE
VHN-V1
VHN
VHN-V8
VRN
VWN
VWN-V8
10ms-t1-2·t2
10ms
10ms
1st H.
2nd H.
3rd H.
S.
100
50
0
TRANSPARENT LIGHT INTENSITY (%)
F+
F-
F+
F-
t

FIG. 15


VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
10ms-t1-2·t2
10ms
10ms
1st H.
2nd H.
3rd H.
S.
TRANSPARENT LIGHT INTENSITY (%)
100
50
0
AF
t

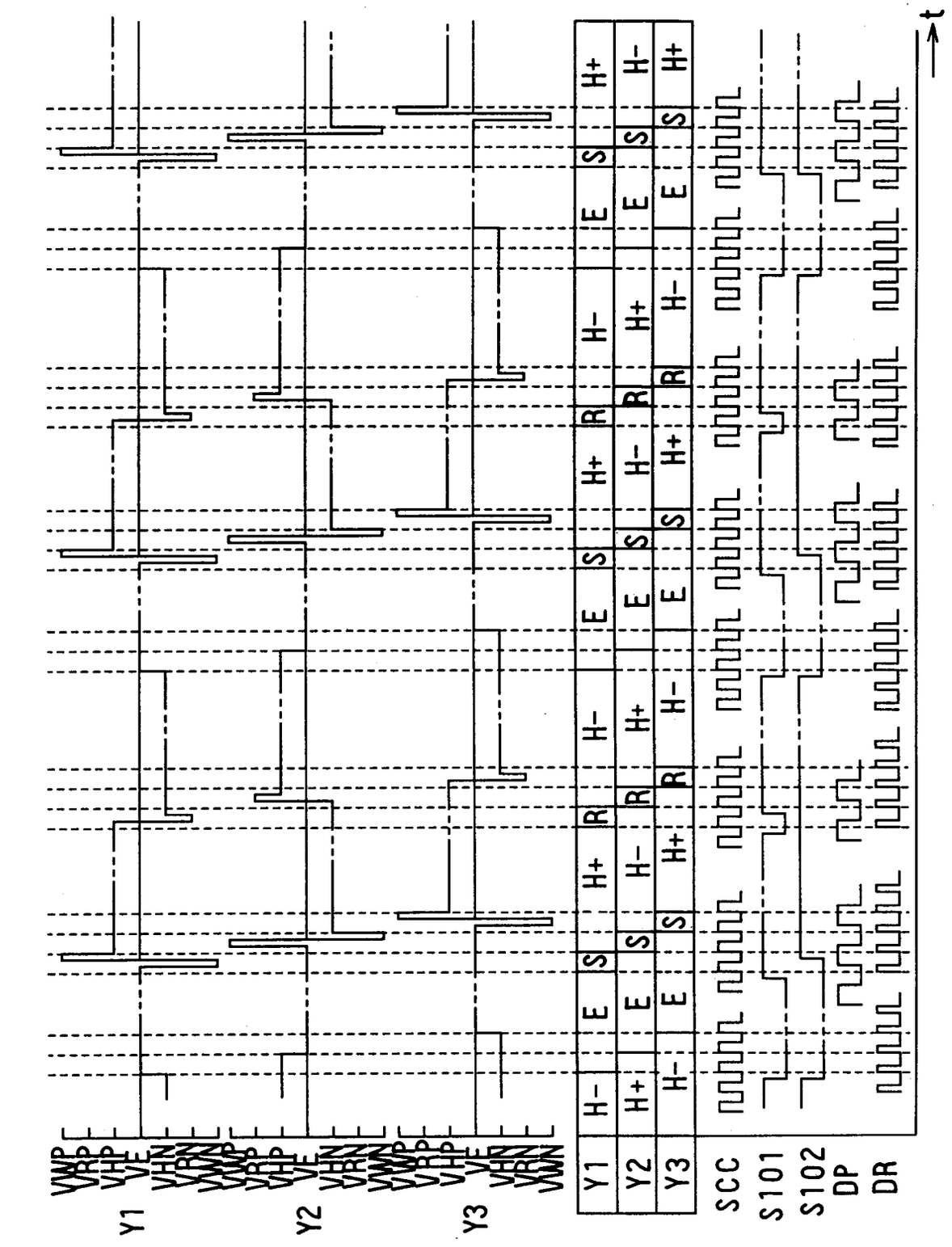


FIG. 16

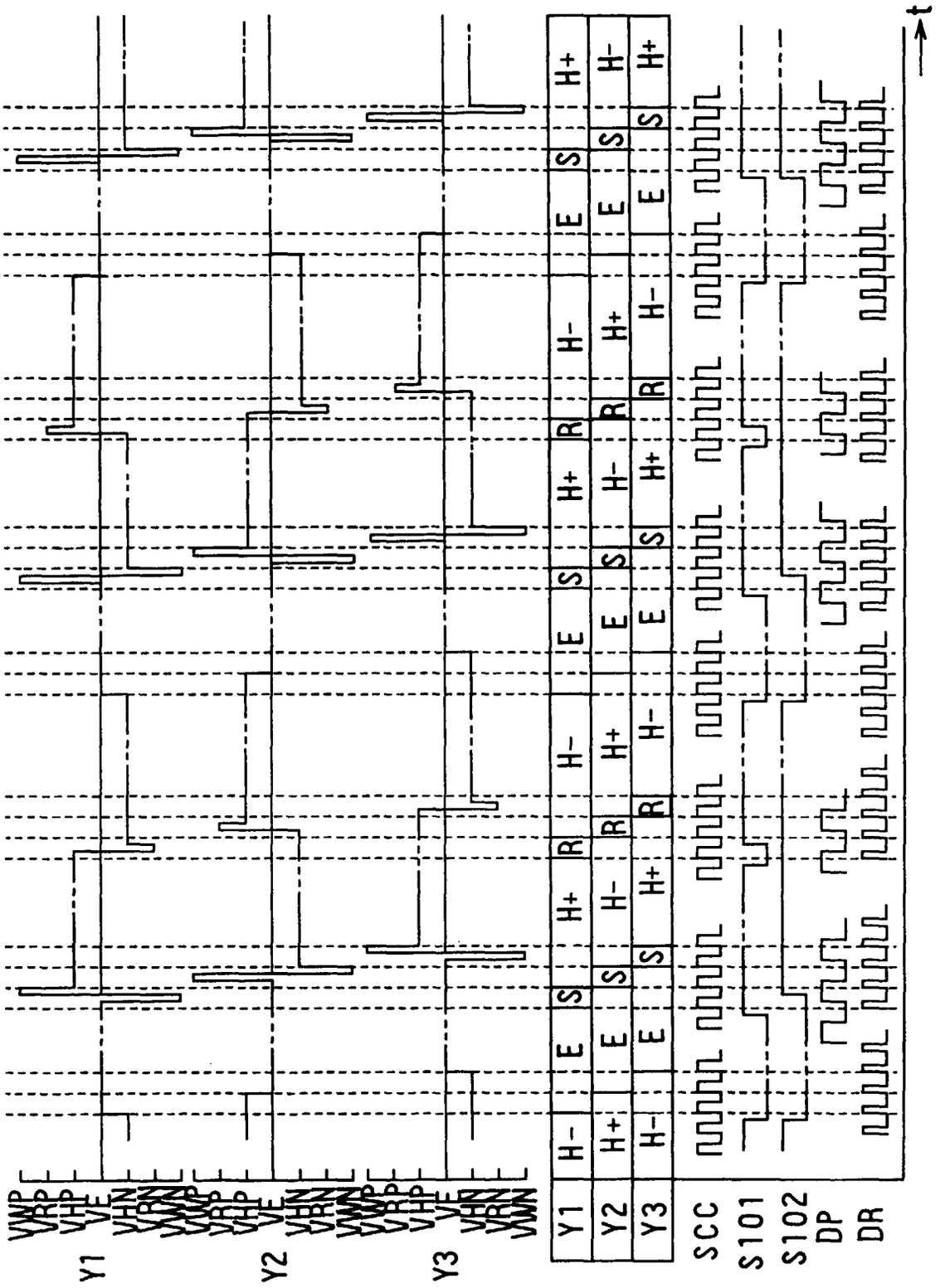


FIG. 17

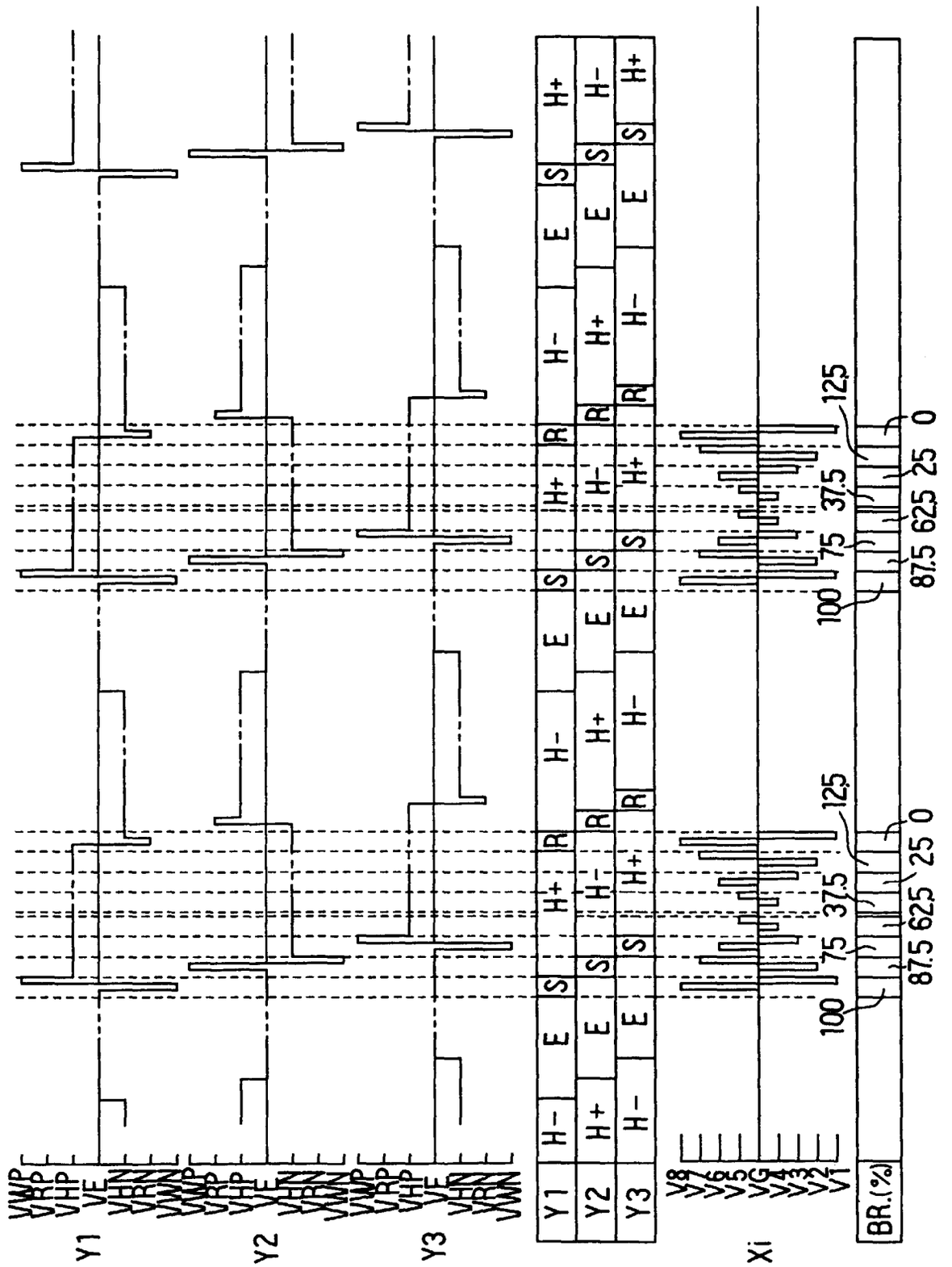


FIG. 18

FIG. 19

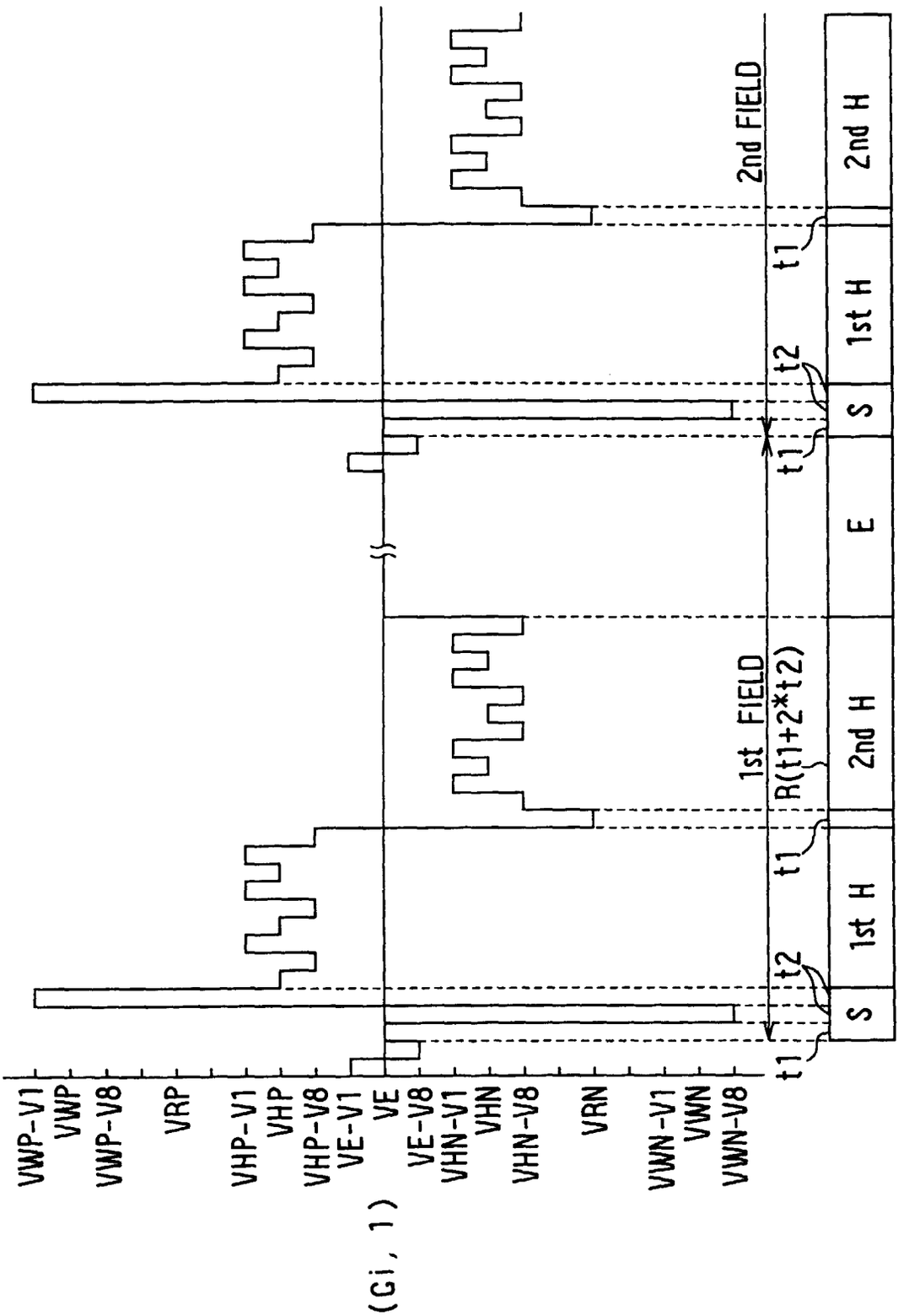

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
(Gi, 1)
1st FIELD
2nd FIELD
t1
t2
R(t1+2*t2)
S
1st H
2nd H
E

FIG. 20

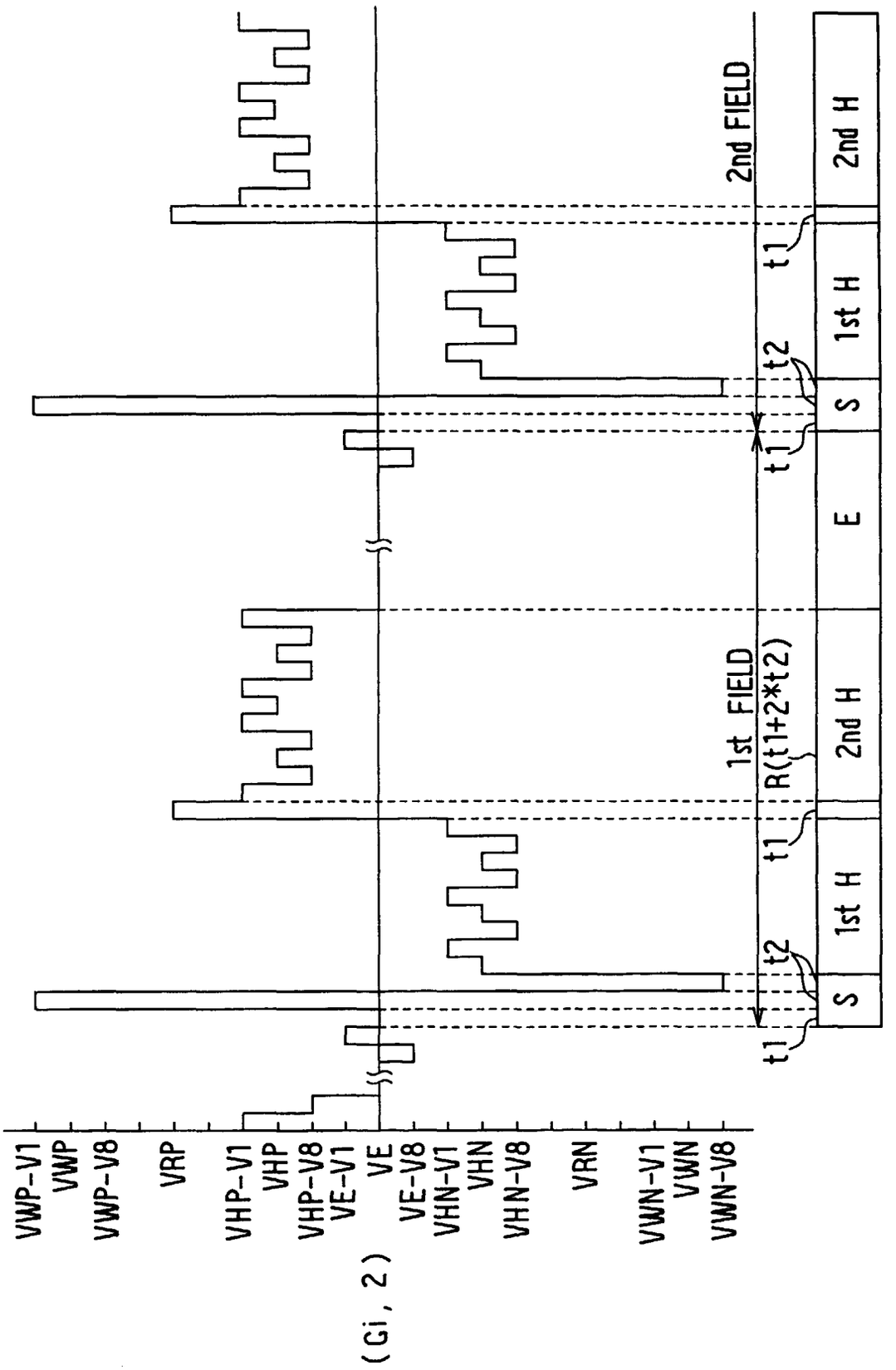
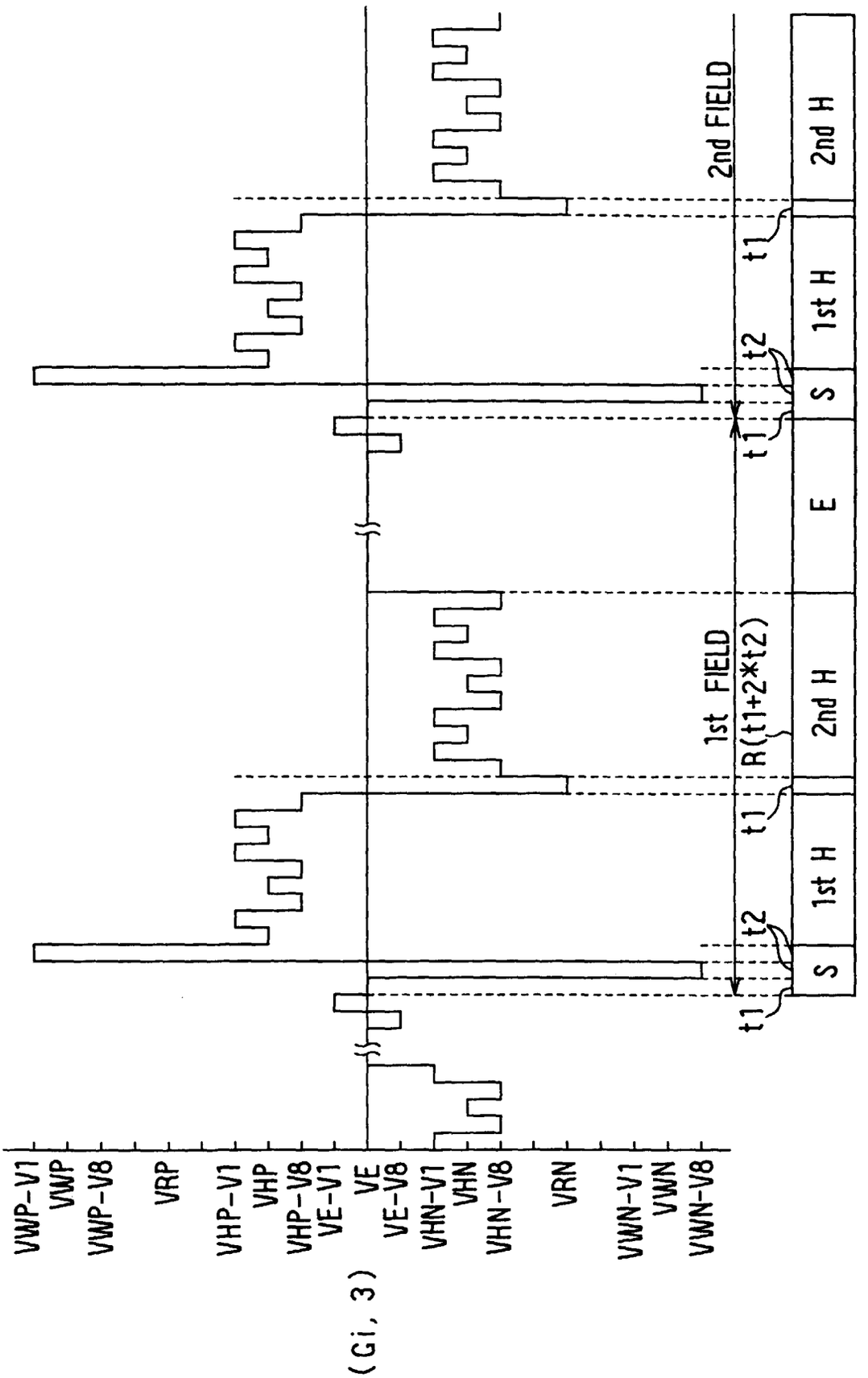

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
(Gi, 2)
1st FIELD
2nd FIELD
R(t1+2*t2)
t1
t2
S
1st H
2nd H
E

FIG. 21


VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
(Gi, 3)
1st FIELD
2nd FIELD
R(t1+2*t2)
t1
t2
S
1st H
2nd H
E

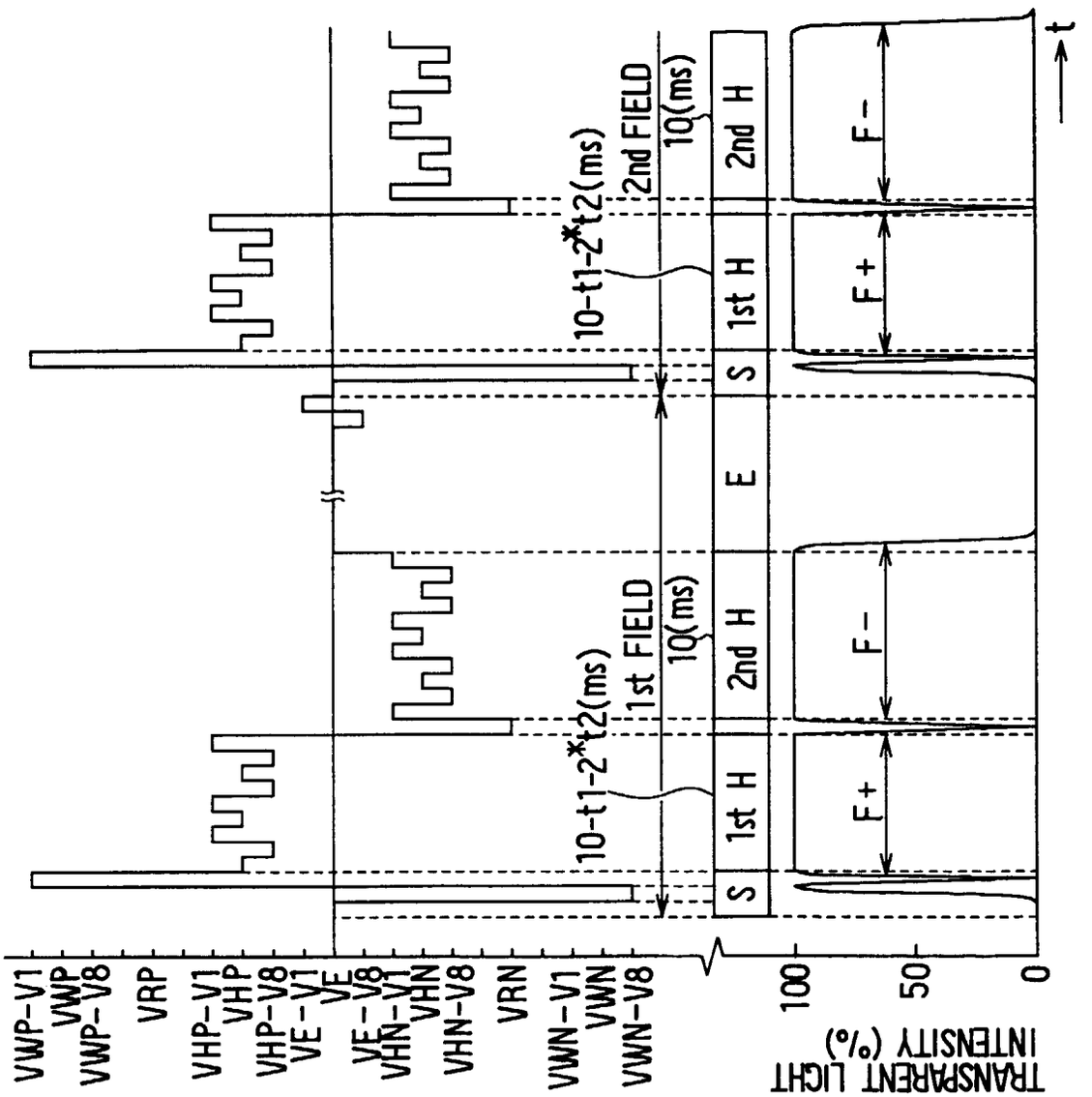

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHN-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
10-t1-2*t2(ms)
1st FIELD
10(ms)
10-t1-2*t2(ms)
2nd FIELD
10(ms)
S
1st H
E
2nd H
S
1st H
2nd H
F+
F-
F+
F-
100
50
0
TRANSPARENT LIGHT INTENSITY (%)
t

FIG. 22

FIG. 23

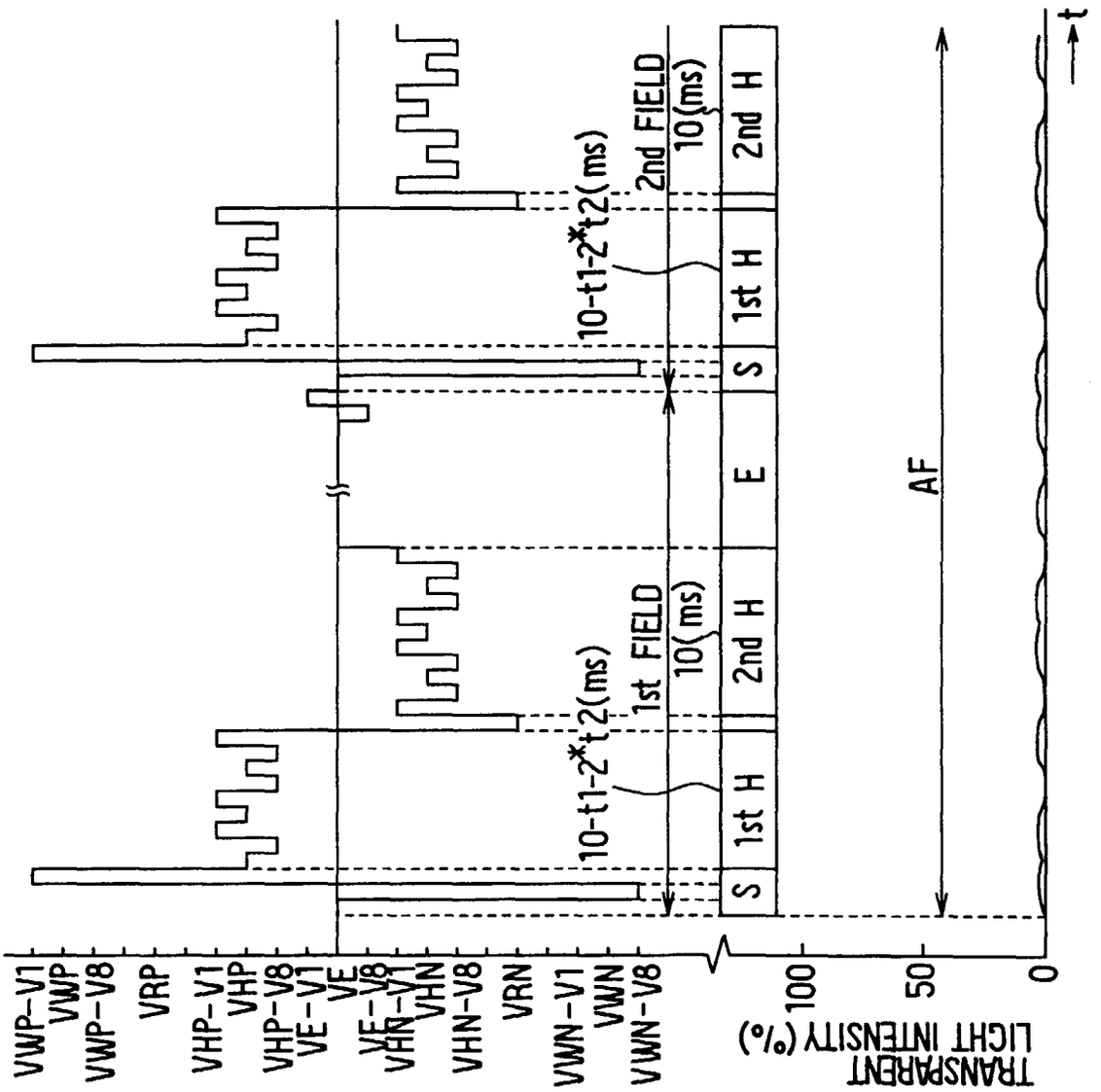

VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE-V1
VE
VE-V8
VHR-V1
VHN
VHN-V8
VRN
VWN-V1
VWN
VWN-V8
10-t1-2*t2(ms)
1st FIELD
10(ms)
10-t1-2*t2(ms)
2nd FIELD
10(ms)
S
1st H
2nd H
E
S
1st H
2nd H
AF
100
50
0
TRANSPARENT LIGHT INTENSITY (%)
t

FIG. 24

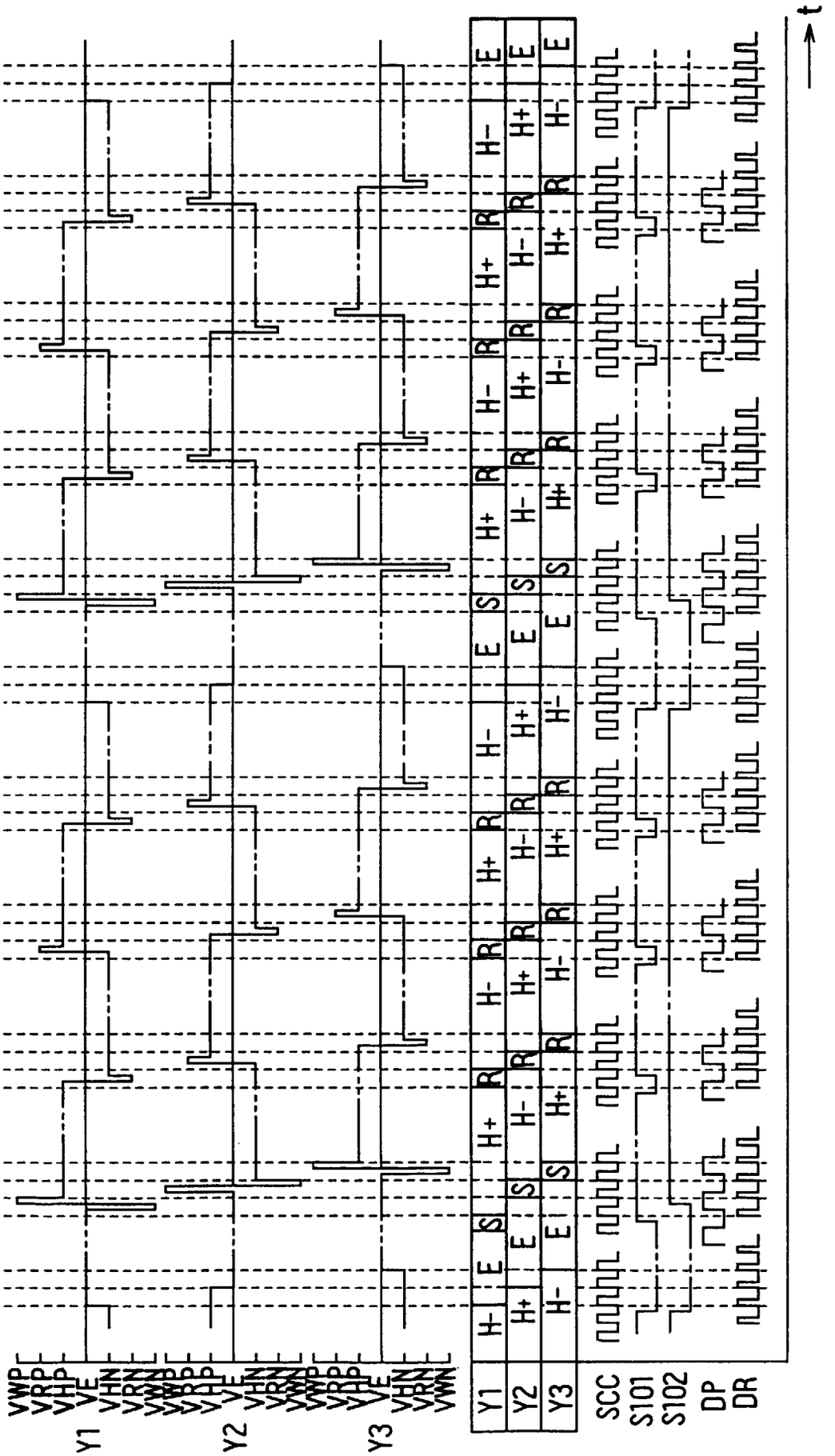
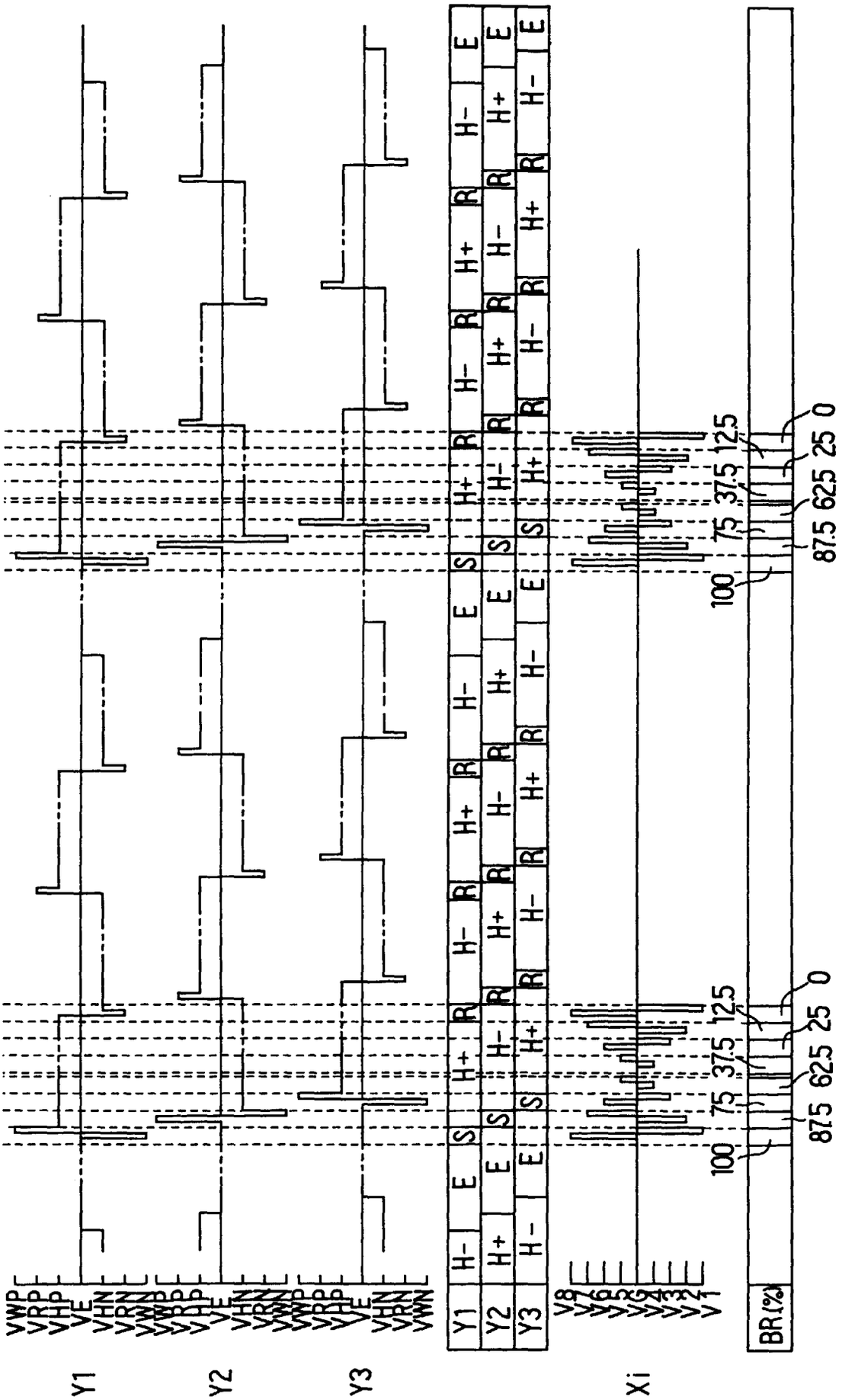


FIG. 25



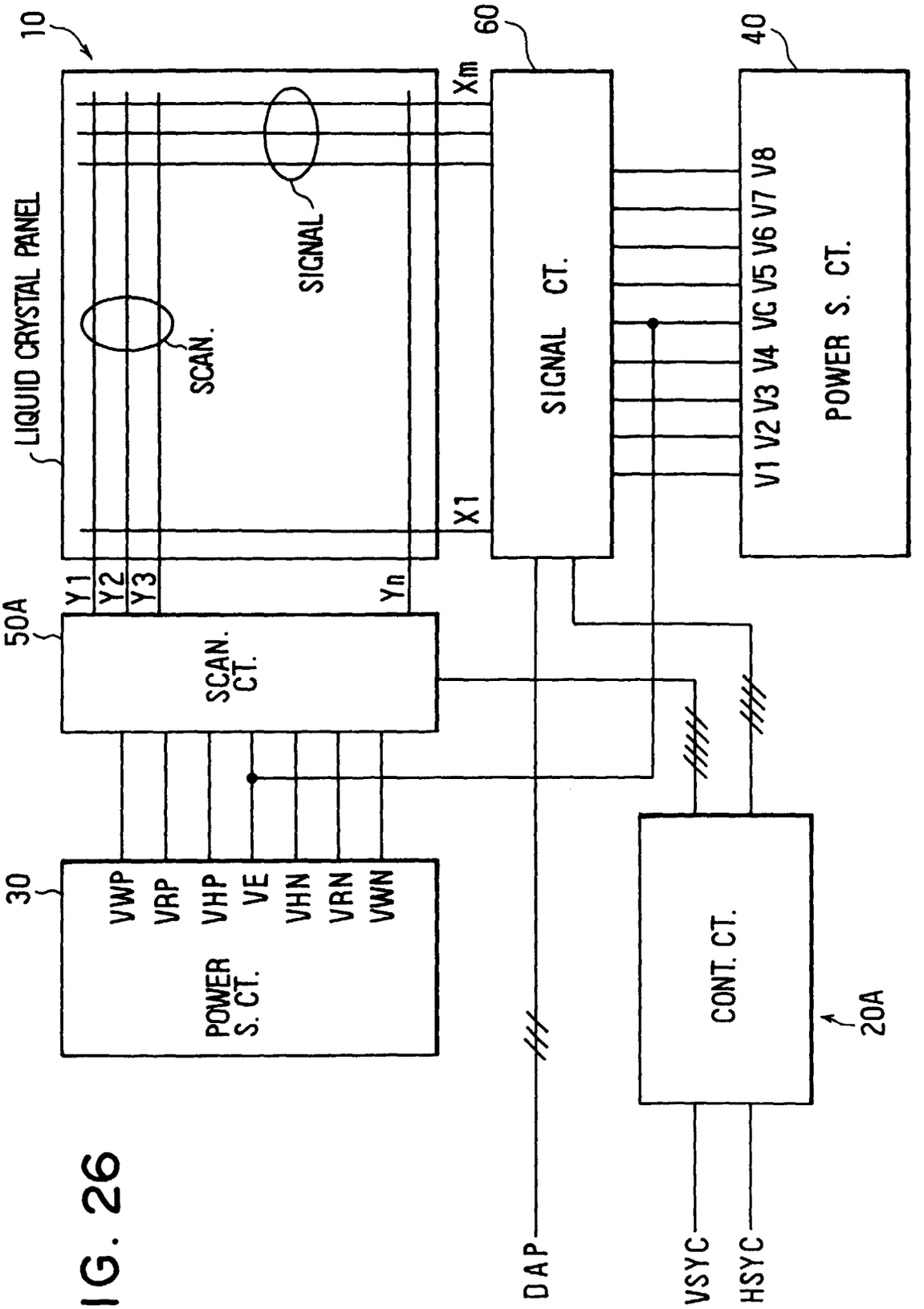

10
LIQUID CRYSTAL PANEL
SCAN.
SIGNAL
Xm
X1
Y1
Y2
Y3
Yn
60
SIGNAL CT.
40
POWER S. CT.
V1 V2 V3 V4 VC V5 V6 V7 V8
50A
SCAN. CT.
30
POWER S. CT.
VWP
VRP
VHP
VE
VHN
VRN
VWN
CONT. CT.
20A
DAP
VSYC
HSYC

FIG. 26

FIG. 27

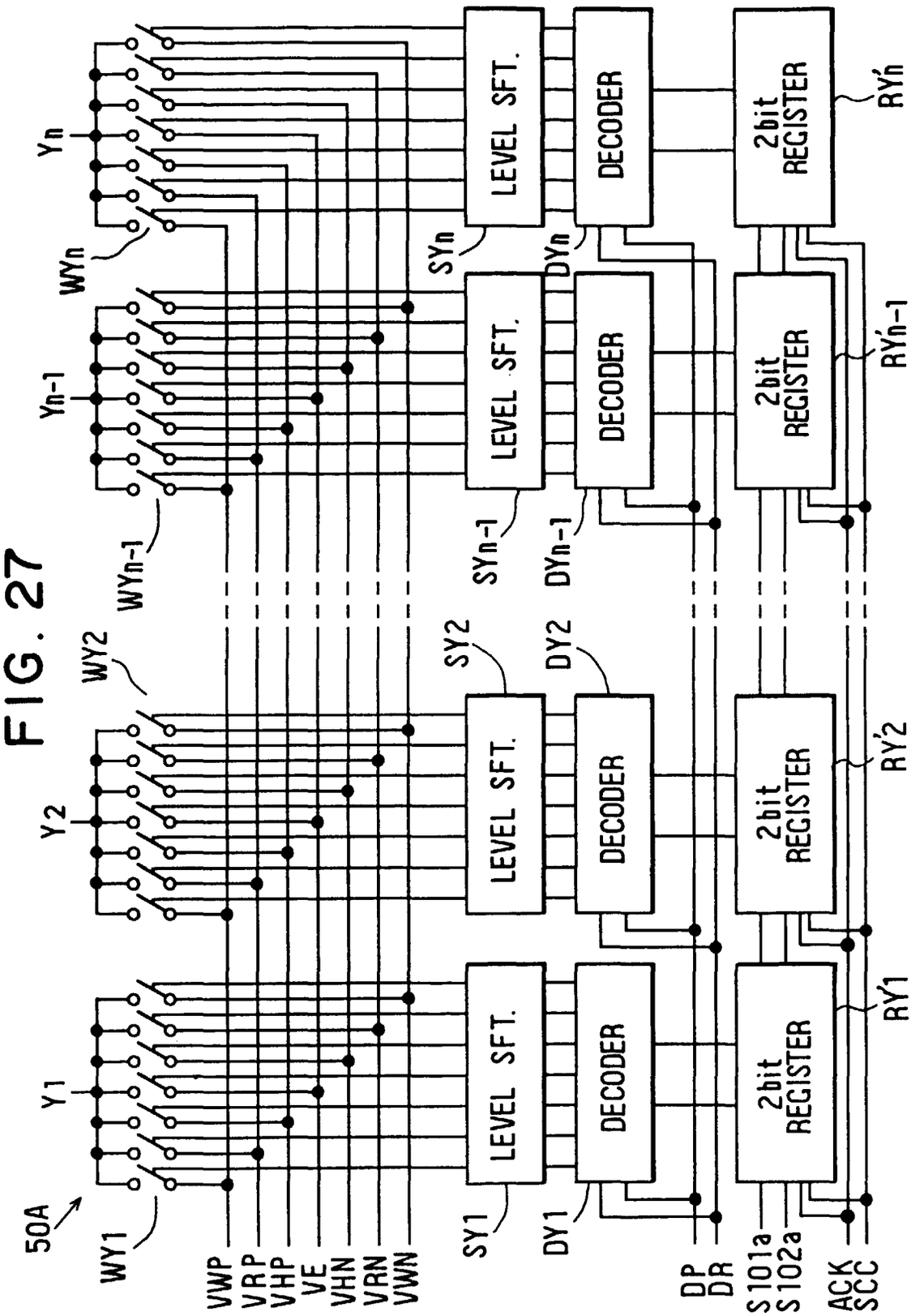

50A
WY1
WY2
WYn-1
WYn
Y1
Y2
Yn-1
Yn
VWP
VRP
VHP
VE
VHN
VRN
VWN
LEVEL SFT.
SY1
SY2
SYn-1
SYn
DECODER
DY1
DY2
DYn-1
DYn
2bit REGISTER
RY'1
RY'2
RY'n-1
RY'n
DP
DR
S101a
S102a
ACK
SCC

FIG. 28

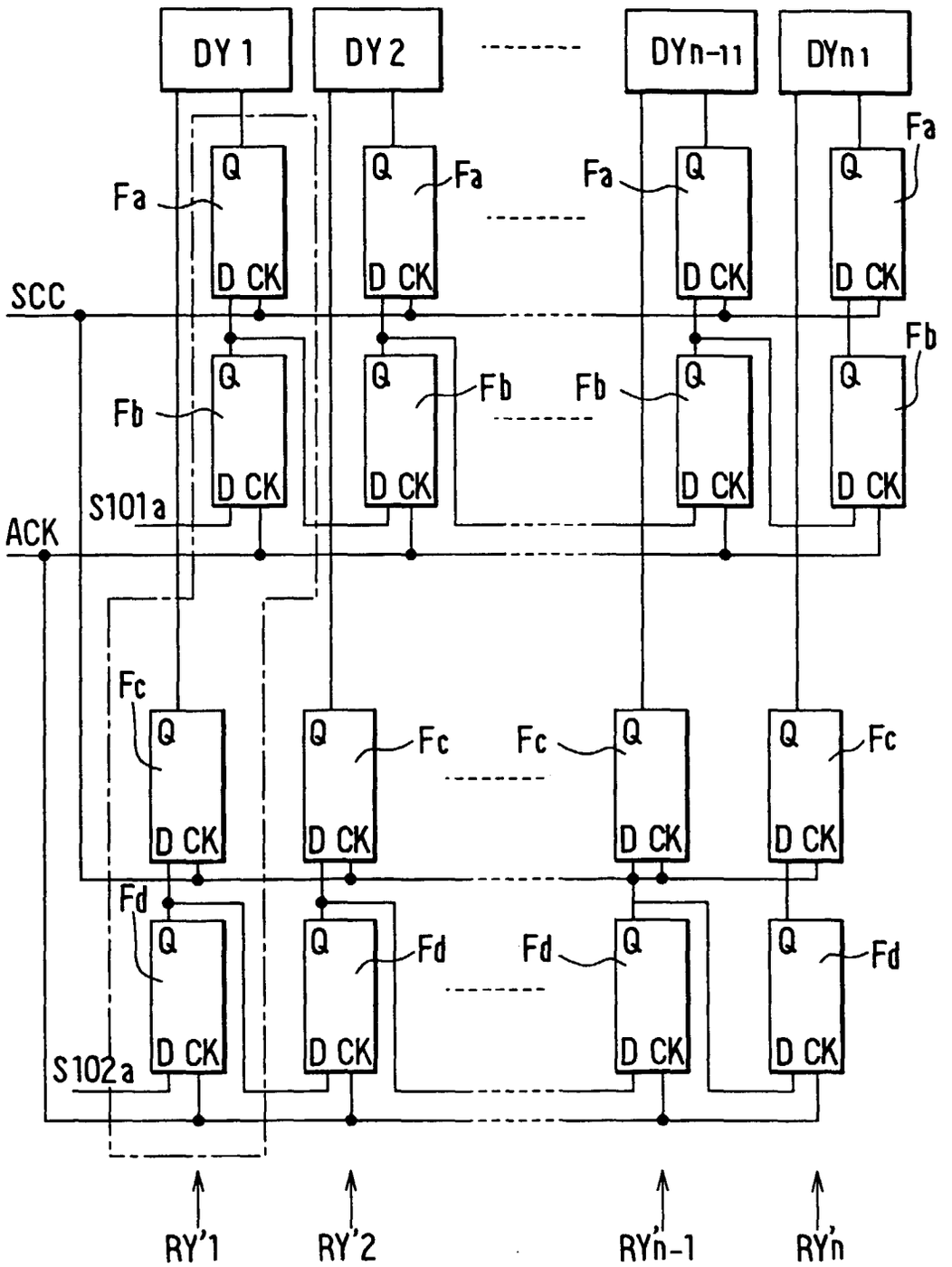

DY 1
DY 2
DYn-11
DYn1
Fa
Fb
Fc
Fd
Q
D CK
SCC
ACK
S101a
S102a
RY'1
RY'2
RY'n-1
RY'n

FIG. 29

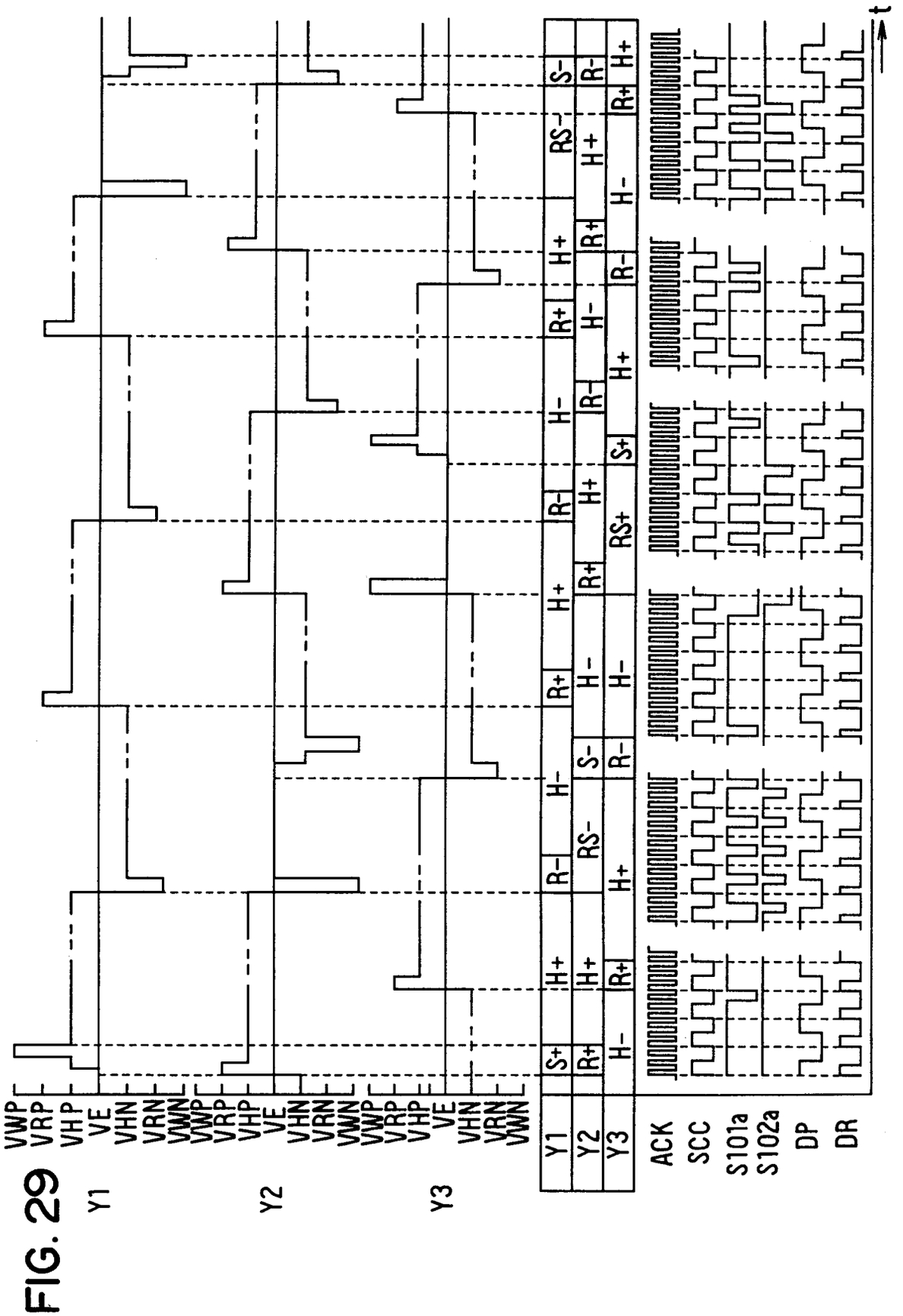

Y1
Y2
Y3
VWP
VRP
VHP
VE
VHN
VRN
VWN
S+
R+
H+
H-
R-
RS-
S-
RS+
S+
H-
R+
H+
H-
R-
S-
ACK
SCC
S101a
S102a
DP
DR
t

FIG. 30

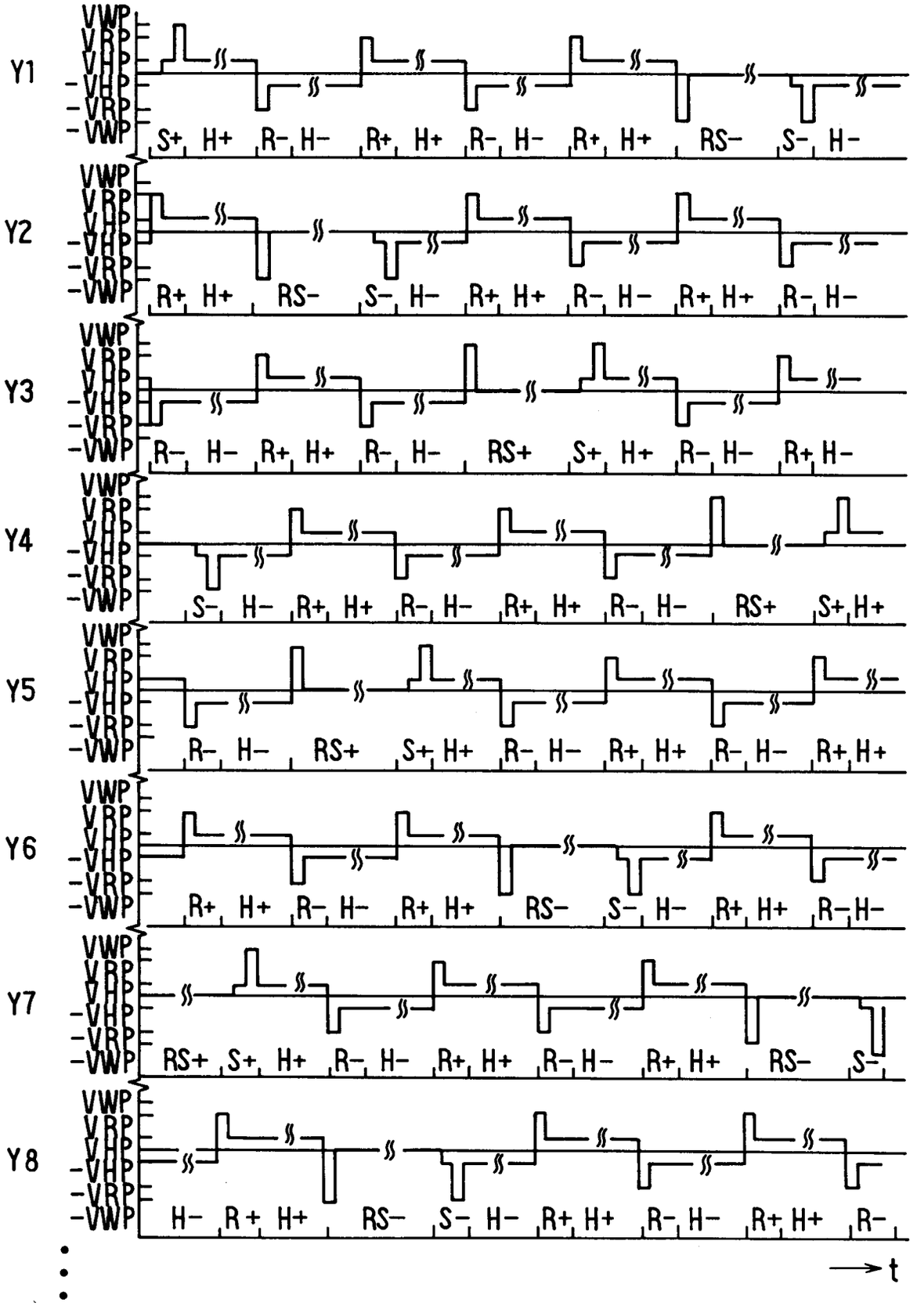

Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
VWP
VRP
VHP
-VHP
-VRP
-VWP
S+ H+ R- H- R+ H+ R- H- R+ H+ RS- S- H-
R+ H+ RS- S- H- R+ H+ R- H- R+ H+ R- H-
R- H- R+ H+ R- H- RS+ S+ H+ R- H- R+ H-
S- H- R+ H+ R- H- R+ H+ R- H- RS+ S+ H+
R- H- RS+ S+ H+ R- H- R+ H+ R- H- R+ H+
R+ H+ R- H- R+ H+ RS- S- H- R+ H+ R- H-
RS+ S+ H+ R- H- R+ H+ R- H- R+ H+ RS- S-
H- R+ H+ RS- S- H- R+ H+ R- H- R+ H+ R-
t

FIG. 31

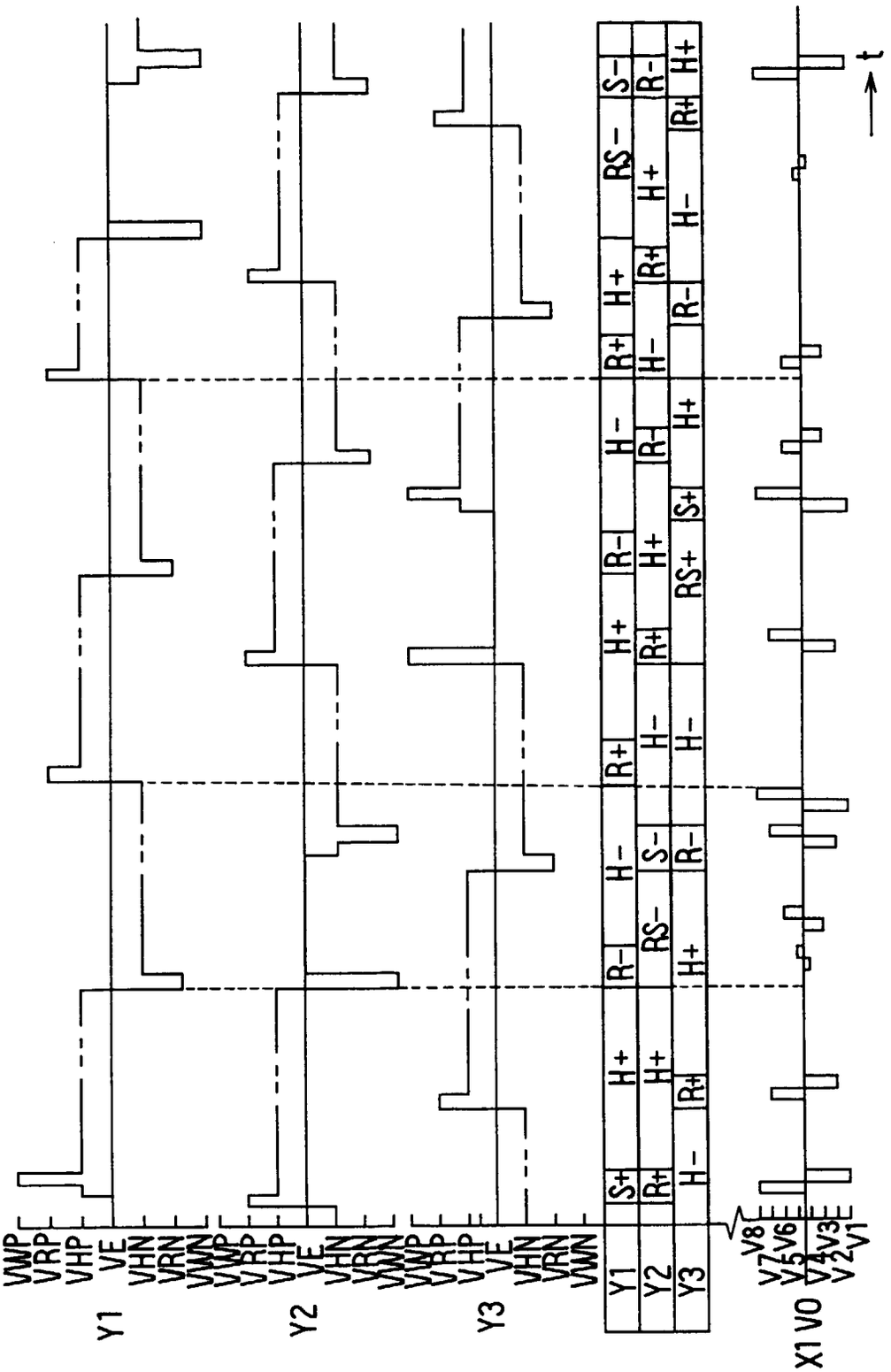

VWP
VRP
VHP
VE
VHN
VRN
VWN
Y1
Y2
Y3
S+
R+
H+
H−
R−
S−
RS+
RS−
V8
V7
V6
V5
V4
V3
V2
V1
V0
X1
t

FIG. 32

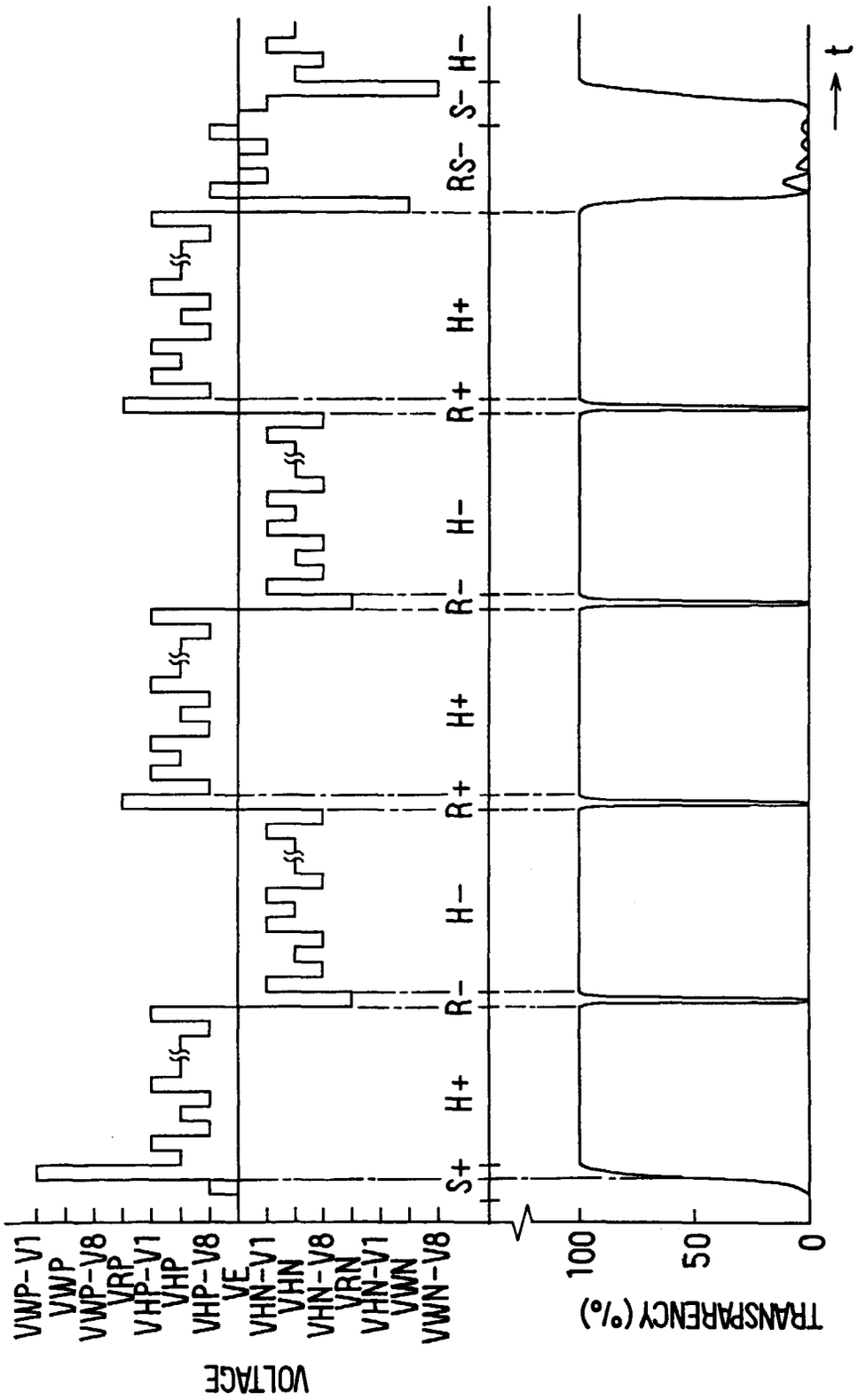

VOLTAGE
VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE
VHN-V1
VHN
VHN-V8
VRN
VHN-V1
VWN
VWN-V8
S+
H+
R-
H-
R+
H+
R-
H-
R+
H+
RS-
S-
H-
TRANSPARENCY (%)
100
50
0
t

FIG. 33

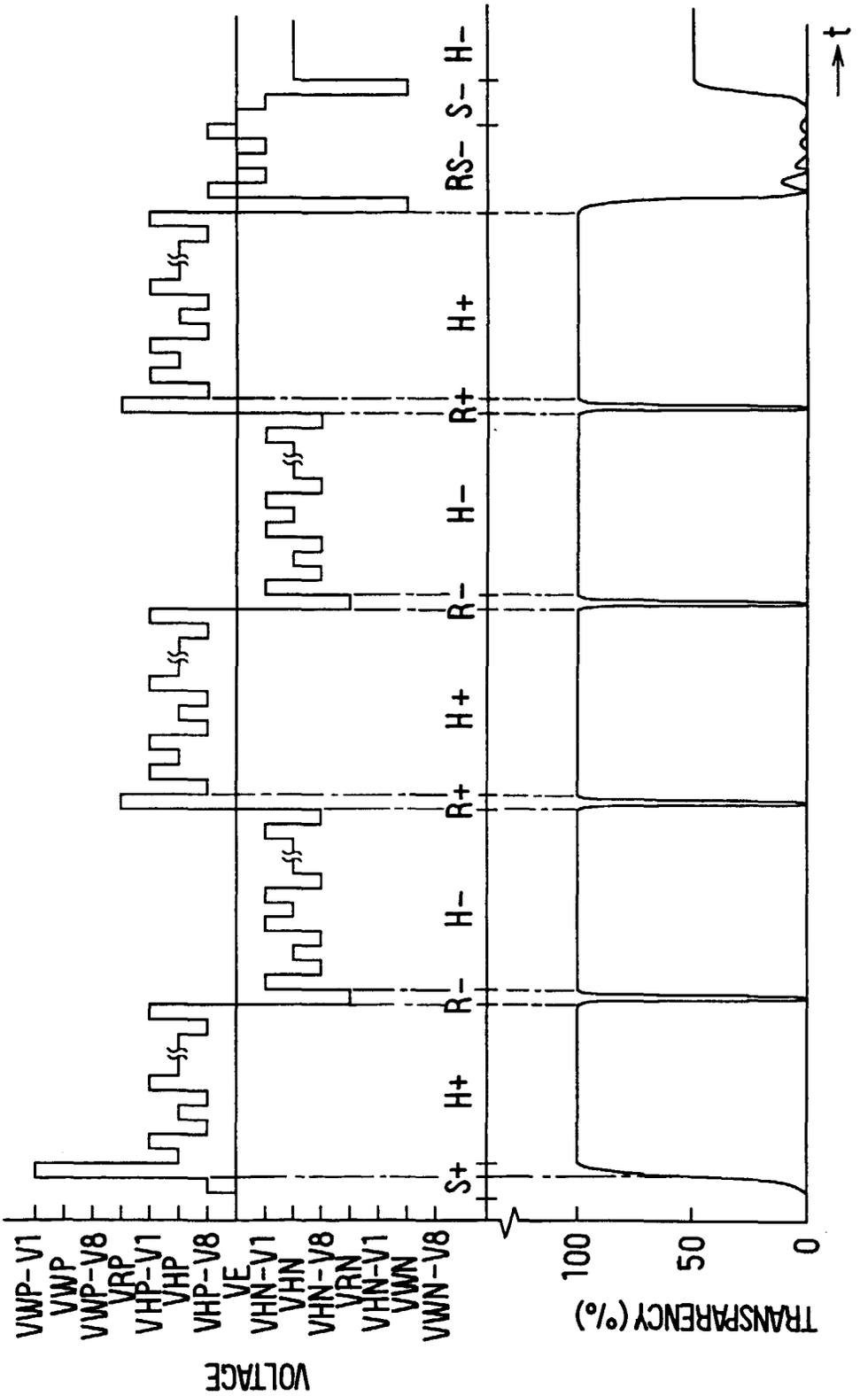
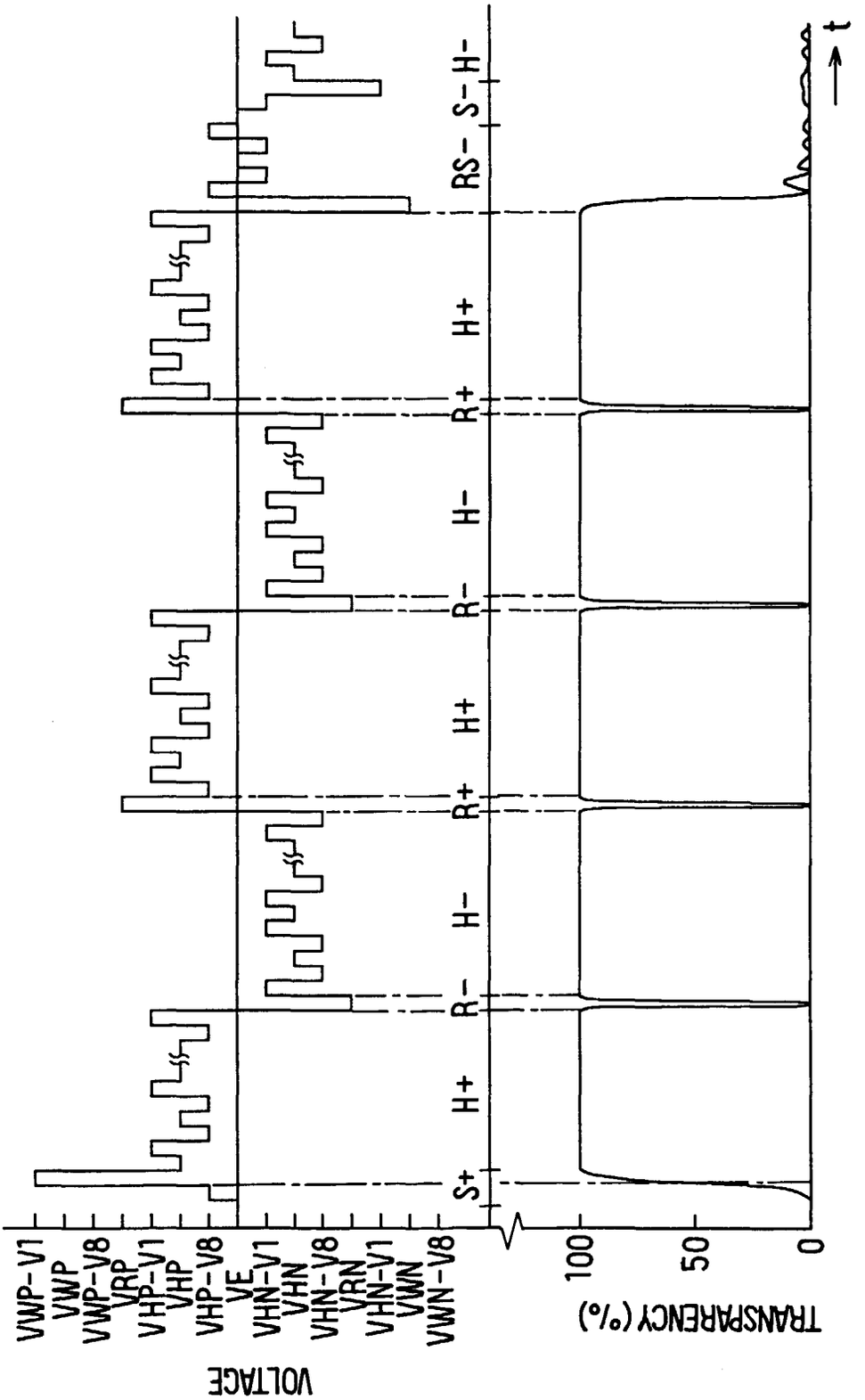

VOLTAGE
VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE
VHN-V1
VHN
VHN-V8
VRN
VHN-V1
VWN
VWN-V8
S+
H+
R-
H-
R+
H+
R-
H-
R+
H+
RS-
S-
H-
TRANSPARENCY (%)
100
50
0
t

FIG. 34


VOLTAGE
VWP-V1
VWP
VWP-V8
VRP
VHP-V1
VHP
VHP-V8
VE
VHN-V1
VHN
VHN-V8
VRN
VHN-V1
VWN
VWN-V8
S+
H+
R-
H-
R+
H+
R-
H-
R+
H+
RS-
S-
H-
TRANSPARENCY (%)
100
50
0
t

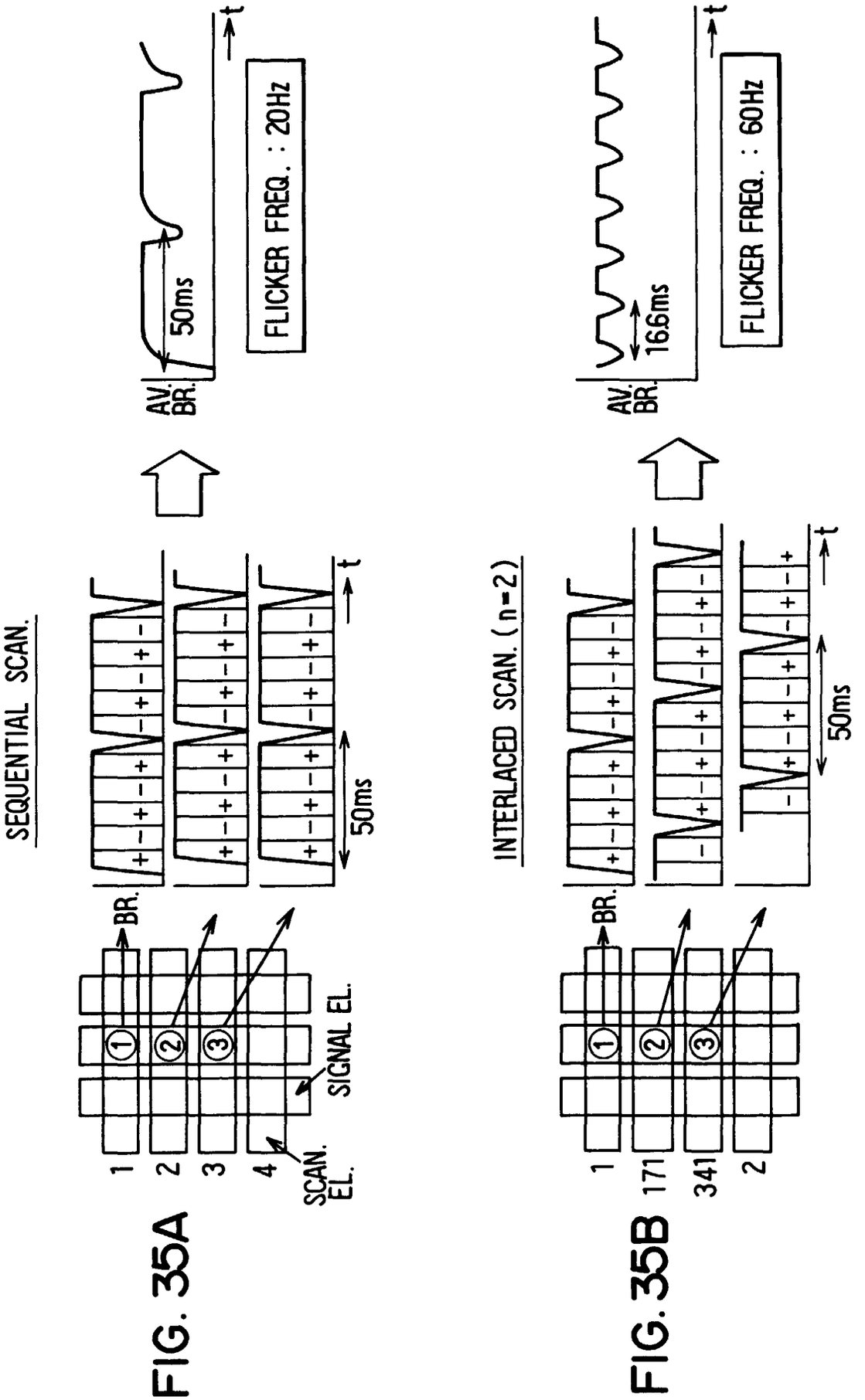


FIG. 35A

FIG. 35B

FIG. 36

n / BR. CHANGE	SEQUENTIAL					1 (FLICKER FREQ.: 40Hz)					2 (FLICKER FREQ.: 60Hz)					3 (FLICKER FREQ.: 80Hz)					4 (FLICKER FREQ.: 100Hz)				
	10%	30%	50%	80%	100%	10%	30%	50%	80%	100%	10%	30%	50%	80%	100%	10%	30%	50%	80%	100%	10%	30%	50%	80%	100%
1 %	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
2 %	×	×	×	×	×	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	△	△	△	△
3 %	×	×	×	×	×	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	△	△	△	△
5 %	×	×	×	×	×	×	×	×	×	×	○	○	○	○	○	△	△	△	△	△	△	△	△	△	△
10 %	×	×	×	×	×	×	×	×	×	×	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△

○ NO FLICKER

△ SCROLLING STRIPE

× FLICKER

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FIG. 37A

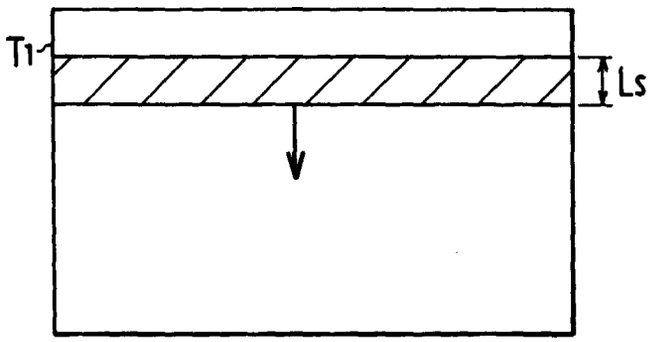


FIG. 37B

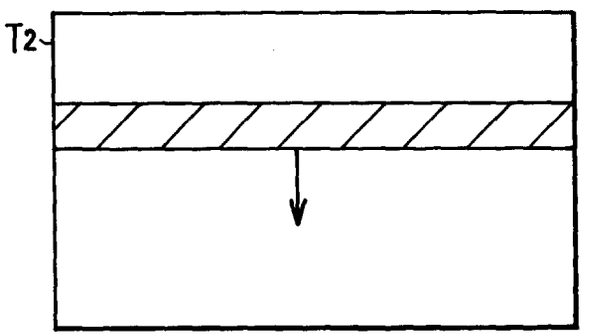


FIG. 37C

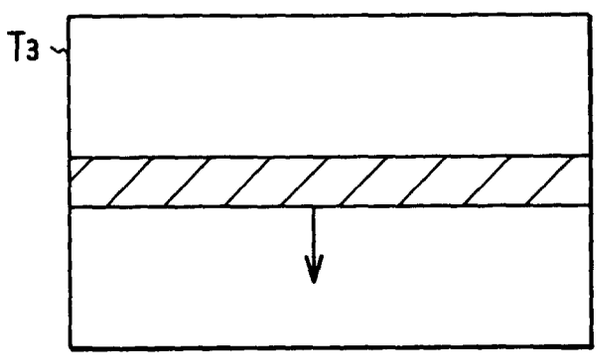


FIG. 38

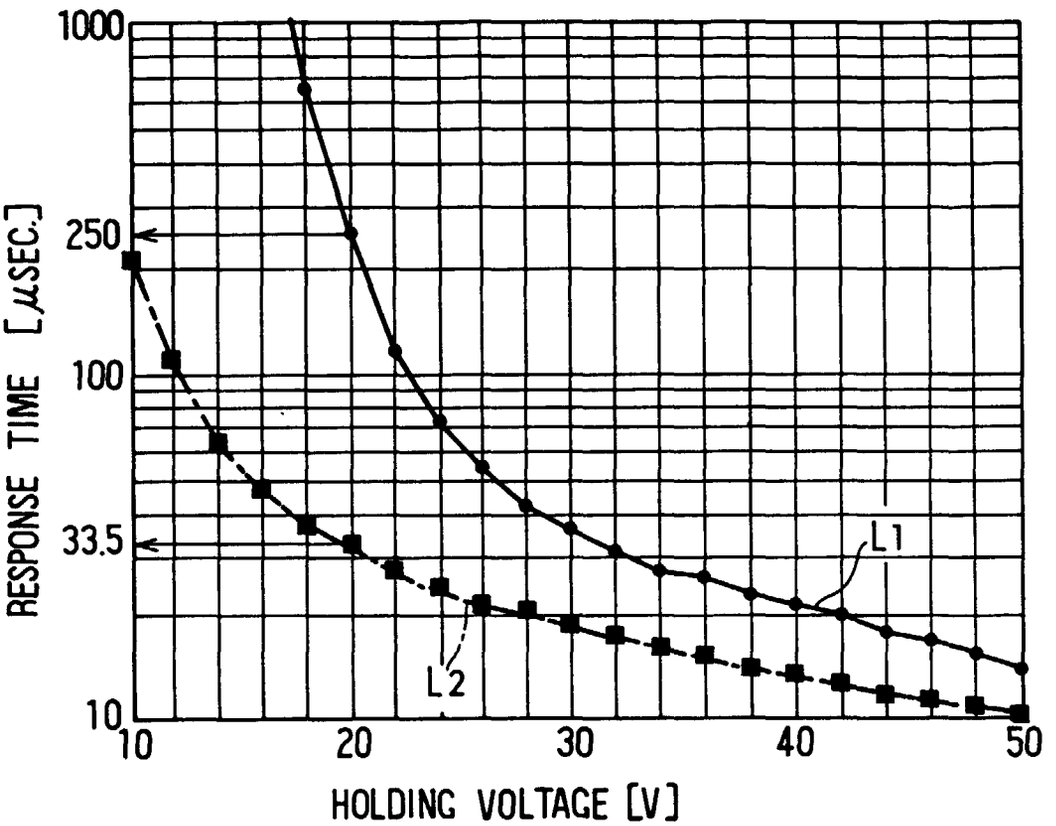
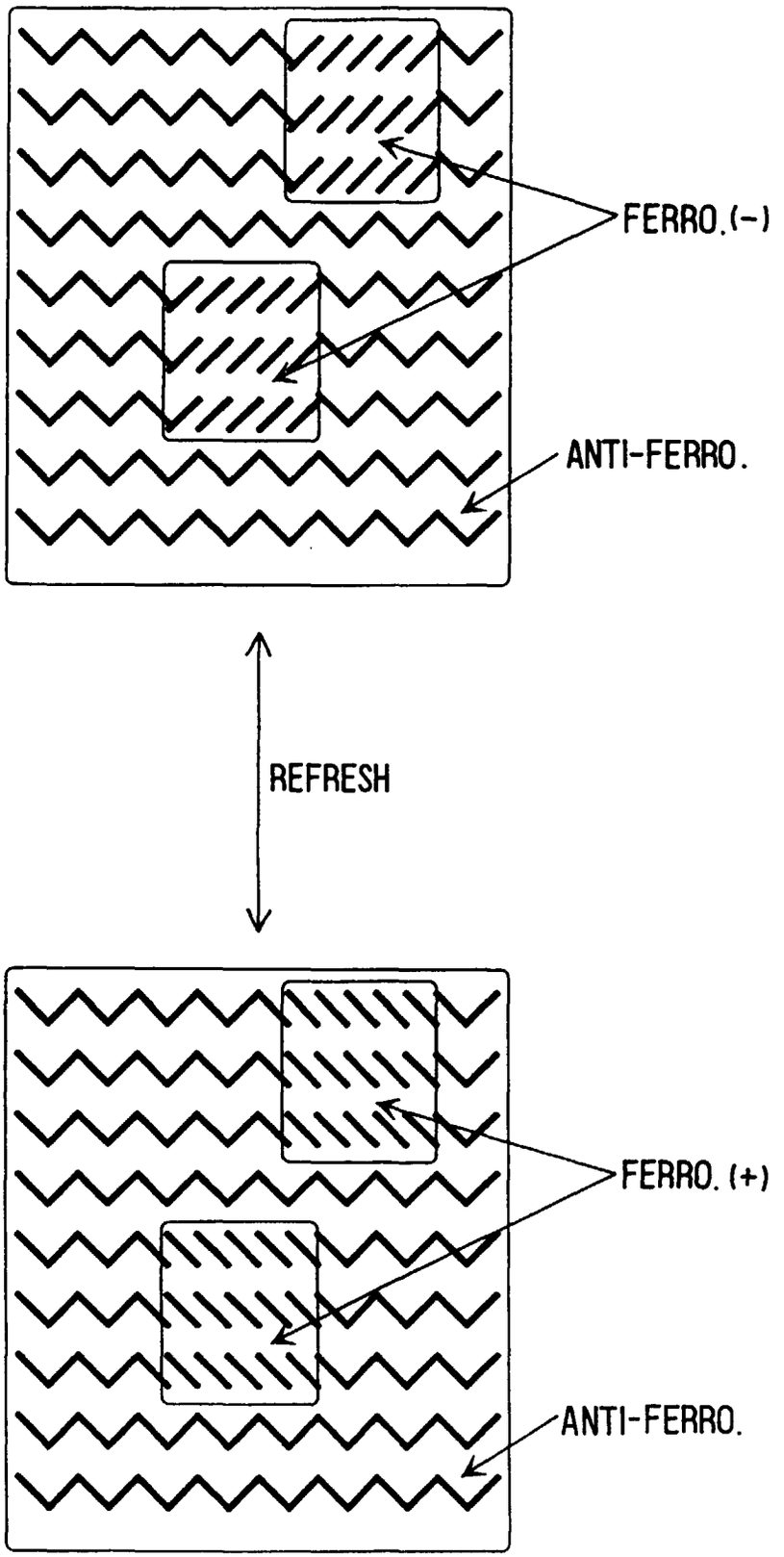

1000
250
100
33.5
10
RESPONSE TIME [μSEC.]
10
20
30
40
50
HOLDING VOLTAGE [V]
L1
L2

FIG. 39



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 11 1163

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 459 481 A (SATO YUZURU ET AL) 17 October 1995 * column 7, line 5 - column 9, line 1 * * column 12, line 15 - line 35 * * column 15, line 13 - line 37 * * figures 7-10,17,18 * * figures 25,27 * * claims 1-3 *	1-5,8,10	G09G3/36
A,P	EP 0 780 825 A (DENSO CORP ;NIPPON SOKEN (JP)) 25 June 1997 * column 2, line 43 - column 4, line 6 * * figures 6,10 *	1,2,8,10	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 September 1998	Farricella, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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