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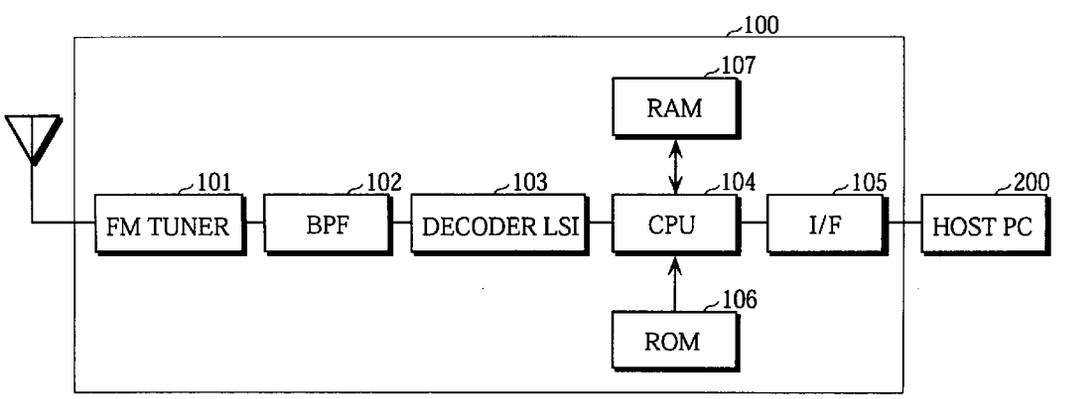
(54) Data broadcasting receiver

(57) A receiver unit receives control-information-program data indicative of program-data-reception permission/inhibition given to each receiver and transfers such received data to a host device. The host device analyzes the control-information-program data supplied from the receiver unit and sends back an analysis result to the receiver unit. The receiver unit stores the analysis result from the host device and determines whether or not to transfer received data to the host device for transfer of only received data that is determined to be transferred to the host device.

FIG. 1



EP 0 893 892 A2

Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a data broadcasting receiver for receiving data transmitted through the data broadcasting such as FM multiplex broadcasting, teletext broadcasting and the like.

Related Art

The FM multiplex broadcasting is for transmission of signals representative of sound, characters, graphics and the like in combination with stereophonic sound signals. That is, the FM multiplex broadcasting is adapted to multiplex the signals representative of sound, characters, graphics and the like onto the normal FM broadcast signals for providing services in a multiplexed fashion.

Typical standards for the FM multiplex broadcasting include the DARC (Data Radio Channel) system, the fixed receiver system and the RDS (Radio Data System). Of these, the DARC system has been organized latest and adopted as the international standard specifications. The DARC system complies with ITU-R807 (International Telecommunication Union Recommendation) "Reference Model for Data Broadcasting".

The DARC system is designed such that characters and graphics are converted into digital information while a 76-kHz subcarrier is modulated to be multiplexed onto a frequency of a stereo baseband signal whereby a multiplexed signal of the FM system is obtained for broadcasting.

Fig.6 diagrammatically illustrates a layered structure representing a character/graphic encoding system according to DARC.

Layer 1 is for specification of transmission path characteristics wherein the multiplex signal is superimposed on a domain of higher frequencies than those of L+R and L-R signals used in the typical FM stereophonic broadcasting. This signal superimposition adopts the LMSK (Level Controlled Minimum Shift Keying) system in consideration of the fact that interference of the multiplex signal with the sound signal becomes significant when a modulation factor of the sound signal is small. The LMSK system is adapted to control the level of multiplex signal based on the modulation factor of the L-R signal.

Layer 2 is for specification of a data frame structure including an error-correcting system. Each data frame consists of 272 columnwise blocks, each block having a 16-bit block identification code (BIC) affixed to its head. The data frame synchronization and data block synchronization are performed based on the block identification codes. Of the 272 columnwise blocks, packets for data transmission account for 190 blocks whereas parity packets for transmission of parities account for 82 blocks. Each packet consists of a 176-bit data portion, a 14-bit CRC (Cycle Redundancy Code) as an error detecting code and a 82-bit parity portion, the data portion, CRC and parity portion arranged in the row direction.

Transmission data is first subject to a one-frame-basis error correction process at this layer. In practice, the data transmission is carried out based on the frame structure in which the packets and the parity packets are rearranged in a predetermined order along the vertical direction.

Layer 3 is for specification of a data packet structure. In each row of the data frame, the data packet excludes the BIC, CRC and parity, accounting for 176 bits. The data packet consists of a prefix and a data block.

Layer 4 is for specification of structure of a data group. The data group consists of one or more than one data blocks. The data group also includes a CRC as the error-detecting code so that the transmission data is subject to the error detection process at this layer, as well. One data group corresponds to data of one page.

Layer 5 is for specification of a structure of a set of information transmitted through the FM multiplex broadcasting, or a set of program data.

Fig. 8 is a functional block diagram for schematically illustrating a construction of an FM broadcasting receiver including a receiver unit such as a PC card.

The FM multiplex broadcasting receiver has a PC card 1 and a personal computer 2 (hereinafter referred to as "host PC") in which the PC card 1 is installed. The PC card 1 includes a tuner 301, a decoder LSI 302 and a data-reception processing section 303. The host PC 2 includes a program-data reconstructing section 304, a program-data analyzing section 305, a display processing section 306, an plotting section 307, and a display 308.

The decoder LSI 302 serves to perform LMSK decoding and error correction processes based on an output from the tuner 301. The decoder LSI 302 converts Layer-1 data into Layer-3 data.

The data-reception processing section 303 captures only necessary data selected from those supplied from the LSI 302 on a block-by-block basis.

The program-data reconstructing section 304 serves to reconstruct program data, converting the Layer-3 data to Layer-4 data.

The program-data analyzing section 305 performs a decoding process based on the 8-bit coding system. The program-data analyzing section 305 converts the Layer-4 data into Layer-6 data (according to the 8-bit coding system).

The display processing section 306 acquires a plotting pattern and performs various processings on the plotting pattern. The plotting section 307 supplies the display 308 with the plotting pattern established by the display processing section 306.

Some FM multiplex broadcasting stations have started to provide a pay-program service and a paging service besides a free program service. There exists a concern about such services. That is, if a pay-program is received by a host PC without a reception permission or if a host PC 2 receives paging data directed to a different destination, the availability of such data, though illegal, may be provided. In order to prevent the host PC without the reception permission from receiving the pay-program service or the paging data from being delivered to somewhere other than its original destination, the PC card 1 is required to determine whether received data may be transferred to the host PC 2 or not.

Some broadcasting stations put on the air control information on reception permission of the pay-program as specific program information. In this case, however, the PC card requires a high speed CPU and a memory of large capacity for making analysis, registration, deletion and the like of the control information. This results in higher costs.

SUMMARY OF THE INVENTION

It is therefore, an object of the invention to provide a data broadcasting receiver wherein the receiver unit is adapted to determine whether or not to transfer received data to the host PC and is less costly.

A first data broadcasting receiver in accordance with the invention comprises a receiver unit for performing processes of channel selection, decoding, error correction and data reception, and a host device supplied with received data from the receiver unit and performing processes of program data reconstruction, program data analysis and program data display, the receiver unit serving to receive control-information-program data indicative of program-data-reception permission/inhibition to each receiver for transfer thereof to the host device, the host device, in turn, analyzing the control-information-program data supplied from the receiver unit and transferring an analysis result to the receiver unit, the receiver unit storing the analysis result supplied from the host device and determining whether or not to transfer received data to the host device based on the analysis result thus stored for transfer of only received data that is determined to be transferred to the host device.

The analysis result may include, for example, data indicative of permission or inhibition of data transfer on a program-by-program basis. Otherwise, the analysis result may include, for example, data indicative of permission or inhibition of data transfer with respect to a pay-program.

The host device may be comprised of, for example, a personal computer. The receiver unit may be comprised of, for example, a PC card installed in the host device. Alternatively, the receiver unit may be of the board type or the box type.

A second data broadcasting receiver in accordance with the invention comprises a receiver unit for performing processes of channel selection, decoding, error correction and data reception, and a host device supplied with received data from the receiver unit and performing processes of program data reconstruction, program data analysis and program data display, which receiver unit transfers to the host device control-information-program data of layer 3 indicative of program-data-reception permission/inhibition given to individual broadcasting receivers on a station-by-station basis, which host device, in turn, converts the control-information-program data of Layer 3 from the receiver unit into control-information-program data of Layer 4 and transfers back to the receiver unit the resultant control-information-program data of Layer 4, and which receiver unit, in turn, stores the control-information-program data of Layer 4 from the host device and determines whether or not to transfer received data to the host device based on the control-information-program data of Layer 4 thus stored for transfer of only received data that is determined to be transferred to the host device.

The host device may be comprised of, for example, a personal computer. The receiver unit may be comprised of, for example, a PC card installed in the host device. Alternatively, the receiver unit may be of the board type or the box type.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating an electrical configuration of an FM multiplex broadcasting receiver in accordance with the invention;

Fig.2 is a flow chart representing steps in a processing procedure taken by a CPU of a PC card in accordance with the invention;

Fig.3 is a flow chart representing steps in a processing procedure taken by a CPU of a PC card in accordance with the invention;

Fig.4 is a block diagram illustrating another electrical configuration of the FM multiplex broadcasting receiver in accordance with the invention;

Fig.5 is a flow chart representing steps in a processing procedure taken by a CPU of a PC card in accordance with the invention;

Fig.6 is a schematic diagram illustrating a layered structure representing a character/graphic coding system in accordance with DARC;

Fig.7 is a schematic diagram illustrating a frame structure in accordance with DARC; and

Fig.8 is a functional block diagram partially illustrating a configuration of the prior-art FM multiplex broadcasting receiver.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Now, FM multiplex broadcasting receivers according to embodiments of the invention will hereinbelow be

described with reference to the drawings.

[1] First Embodiment

Fig.1 diagrammatically illustrates a configuration of an FM multiplex broadcasting receiver according to the invention.

The FM multiplex receiver includes a PC card 100 as the receiver unit and a personal computer 200 (hereinafter referred to as "host PC") in which the PC card 100 is installed.

The PC card 100 has functions corresponding to those provided by a tuner 301, a decoder LSI 302 and a data-reception processing section 303 shown in Fig.8. By installing a specific software therein, the personal computer 200 is imparted with functions provided by the program-data reconstructing section 304, program-data analyzing section 305, display processing section 306, plotting section 308 and program-data display section 308 shown in Fig.8.

The PC card 100 includes an FM tuner 101, a bandpass filter (BPF) 102, a decoder LSI 103, a CPU 104 and an interface 105. The CPU 104 includes a ROM 106 for storing a program therefor and a RAM 107 for holding data as required.

An FM multiplexed signal is received through an antenna to be supplied to the FM tuner 101. The signal is subject to synchronous detection and then supplied to the bandpass filter 102. The bandpass filter filters out signal components in a predetermined frequency band. An output from the bandpass filter 102 is applied to the decoder LSI 103 where the signal is subject to the LMSK decoding, synchronous detection and error correction.

The CPU 104 responds to a data transfer request generated by the decoder LSI 103 at predetermined time intervals (e.g., 18 msec) so as to read out the received data from the decoder LSI 103. The RAM 107 holds the data (Layer-3 data) from the CPU 104 which is supplied by one packet per predetermined time interval (e.g., 18 msec).

The packet data stored in the RAM 107 is supplied to the host PC 200 via the interface 105. A CPU (not shown) of the host PC 200 extracts a data block from the received packet data for reconstructing a data group of the data blocks and performs the error detection on the resultant data group.

The reconstructed data groups per program are sequentially stored in a storage device (not shown) in the host PC 200 on a page-by-page basis. The CPU of the host PC 200 selects predetermined page data for outputting the selected data to the display section (not shown). The display section, in turn, outputs character information or graphical information corresponding to the page data thus supplied.

Incidentally, a user selects a desired channel through an operation section of the host PC 200. When a channel is selected, the CPU 104 of the PC card 100 is supplied with a channel selection command from the host PC 200. Based the channel selection command from the host PC 200, the CPU 104 controls the FM tuner 101.

According to the first embodiment of the invention, each FM multiplex broadcasting station transmits to each receiver control information indicative of data-reception permission/inhibition as specific control- information-program data, such as, for example, control-information-program data having a service identification of "13".

The control-information-program data (hereinafter referred to simply as "control information") includes a code indicative of a broadcasting station (broadcasting station code), information indicative of whether each receiver's ID or each group ID has a reception permission of a pay-program or not, and information on a subscription period for each pay-program the reception permission of which is gained.

Such control information is analyzed by the host PC 200 so that information indicative of permission/inhibition of data transfer (hereinafter referred to as "transfer permission/inhibition information") with respect to each program identified by the service identification and a program number is stored in the storage device, such as a hard disk, of the host PC 200 as associated with each broadcasting station code, the transfer permission/inhibition information on the program being based on the control information on the receiver's ID or the group ID, for example.

When a channel is selected, the host PC 200 supplies the CPU 104 of the PC card 100 with transfer permission/inhibition information corresponding to the selected channel. The CPU 104 of the PC card 100, in turn, commits the supplied transfer permission/inhibition information to storage at the RAM 107.

Control information supplied from the broadcasting station after the channel selection is also analyzed and stored by the host PC 200. In a case where a need arises for updating the transfer permission/inhibition information in connection with availability of a new program or unavailability of a program due to the expiration of the subscription period thereof, an update command is transferred from the host PC 200 to the CPU 104 of the PC card 100 such that the transfer permission/inhibition information stored in the RAM 107 is updated.

Fig.2 illustrates steps in a processing procedure taken by the CPU 104 of the PC card 100.

The CPU 104 performs processes in response to power-up of the receiver, reception of a channel selection command from the host PC 200, reception of data from the decoder LSI 103 and reception, from the host PC 200, of a command to update the transfer permission/inhibition information.

When power is turned on or a channel selection command from the host PC 200 is received ("YES" at Step 4), transfer permission/inhibition information in the RAM 107 is deleted (Step 1). Subsequently, if transfer

permission/inhibition information corresponding to a currently selected broadcasting station is supplied from the host PC 200 within a given time period ("YES" at Step 2), the transfer permission/inhibition information thus supplied is held by the RAM 107 (Step 3).

Upon reception of data from the decoder LSI 103 ("YES" at Step 5), the CPU 104 determines whether to transfer the received data to the host PC 200 or not based on the transfer permission/inhibition information held by the RAM 107 (Step 6).

If the received data is determined to be transferred to the host PC 200, the host PC 200 is supplied with the received data via the interface 105 (Step 7). The received data is determined to be transferred to the host PC 200 in cases where received program data constitutes a free program, a control-information program for providing control information, and a pay-program a reception permission of which is gained.

In a case where the received data is determined not to be transferred to the host PC 200, the host PC 200 is not supplied with the received data.

When an update command on transfer permission/inhibition information is supplied from the host PC 200 (Step 8), the transfer permission/inhibition information in the RAM 107 is updated in accordance with the update command thus supplied (Step 9).

According to the first embodiment of the invention, the analysis on the control information is carried out by the host PC 200 and therefore, a processing load on the CPU 104 of the PC card 100 is advantageously reduced. This negates the need for installing a high-speed CPU and a RAM of large capacity in the PC card 100, thus contributing to the reduction of costs.

[2] Second Embodiment

An FM multiplex broadcasting receiver of this embodiment has a similar configuration to that of the first embodiment hereof shown in Fig.1.

According to the first embodiment hereof, transfer permission/inhibition information obtained from the control information is stored in the memory device, such as a hard disk, of the host PC 200 as associated with each broadcasting station code. On the other hand, the second embodiment hereof preliminarily specifies scopes of the free programs, the control information programs and the pay-programs. In principle, only the control information programs and the free programs are transferred to the host PC 200 immediately after the channel selection.

After reception of control information, the host PC 200 analyzes the control information and supplies the PC card 100 with permission/inhibition information on the pay-programs. The PC card 100, in turn, stores the permission/inhibition information on the pay-programs in the RAM 107 so that, upon reception of pay-program data, the CPU 104 of the PC card 100 may determine whether or not to transfer received data to the host PC 200 based on the permission/inhibition information on the pay-programs stored in the RAM 107.

Fig.3 illustrates steps in a processing procedure taken by the CPU 104 of the PC card 100.

The CPU 104 performs processes in response to power-up of the receiver, reception of a channel selection command from the host PC 200, reception of data from the decoder LSI 103 and reception, from the host PC 200, of a command to update the permission/inhibition information.

When power is turned up or a channel selection command is supplied from the host PC 200 ("YES" at Step 12), the permission/inhibition information on the pay-programs stored in the RAM 107 is deleted (Step 11).

Upon reception of data from the decoder LSI 103 ("YES" at Step 13), the CPU 104 determines whether or not to transfer the received data to the host PC 200 based on the permission/inhibition information on the pay-programs stored in the RAM 107 (Step 14). At this time, data of the free program and of the control information program are determined to be transferred. Out of the pay-programs, only that which are given the permission based on the transfer permission/inhibition information on the pay-programs are determined as the data to be transferred.

In a case where the received data is determined to be transferred to the host PC 200, the host PC 200 is supplied with the received data via the interface 105. In a case where the received data is determined not to be transferred to the host PC 200, the host PC 200 is not supplied with the received data.

When permission/inhibition information on the pay-programs or an update command thereof is supplied from the host PC 200 ("YES" at Step 16), the CPU 104 commits the supplied permission/inhibition information on the pay-programs to storage at the RAM 107 or updates the permission/inhibition information in the RAM 107 based on the update command thus supplied (Step 17).

According to the second embodiment hereof, the control information is analyzed by the host PC 200 and therefore, a processing load on the CPU of the PC card is advantageously reduced. This negates the need for installing a high-speed CPU and a RAM of large capacity in the PC card 100, thus contributing to the reduction of costs.

Additionally, the permission/inhibition information on the pay-programs, which is given as the result of the analysis on the control information, is not stored in the hard disk of the host PC 200 and therefore, there is provided an enhanced security of the receiver.

[3] Third Embodiment

Fig.4 illustrates another configuration of the FM multiplex broadcasting receiver. In the figure, like parts to those in Fig.1 are correspondingly represented by the

like reference characters and the description thereof is omitted. The FM multiplex broadcasting receiver of Fig.4 further includes an EEPROM 108 for holding Layer-4 control information.

The third embodiment hereof preliminarily specifies scopes of the free programs, the control information programs and the pay-programs. In principle, only the free programs and the control information programs are transferred to the host PC 200 immediately after the channel selection. Receiving Layer-3 control information, the host PC 200 converts the Layer-3 control information into Layer-4 control information and transfers the resultant Layer-4 control information to the PC card 100. The PC card, in turn, commits the Layer-4 control information from the host PC 200 to storage at the EEPROM 108.

In the case of reception of pay-program data, the CPU 104 of the PC card 100 determines if the reception of the incoming data is permitted or not based on the control information held by the EEPROM 108. Thus, the CPU 104 transfers to the host PC 200 only pay-program data the reception of which is permitted.

Fig.5 illustrates steps in a processing procedure taken by the CPU 104 of the PC card 100.

The CPU 104 performs processes in response to power-up of the receiver, reception of a channel selection command from the host PC 200, reception of data from the decoder LSI 203, reception of Layer-4 control information from the host PC 200 and reception of current date/time data supplied from the host PC 200 in a predetermined timing.

Upon power-up of the receiver or transfer of a channel selection command to the PC card 100, the host PC 200 supplies to the PC card 100 a broadcasting station code associated with a currently selected channel and current date/time data. Further, the host PC 200 continues to supply the current date/time data to the PC card 100 in the predetermined timing. The current date/time data supplied from the host PC 200 to the PC card 100 may be generated based on a clock function owned by the host PC 200. Otherwise, current date/time data contained in the control information may be utilized.

When power is turned on or a channel selection command is supplied from the host PC 200 ("YES" at Step 23), the CPU 104 waits for a broadcasting station code associated with the currently selected channel and current date/time data which are supplied from the host PC 200 (Step 21). Upon reception of such data, the CPU 104 commits the supplied data to storage at the RAM 107 (Step 22).

When receiving data from the decoder LSI 103 ("YES" at Step 24), the CPU 104 determines whether or not to transfer the received data to the host PC 200 based on the control information which is stored in the EEPROM 108 and corresponds to the currently selected broadcasting station (Step 25). At this time, data on the free program and the control information program are determined to be transferred. Out of the pay-programs, determined to be transferred are only those that are given the reception permission based on the control information stored in the EEPROM 108 and corresponding to the currently selected broadcasting station. At this time, whether the pay-program with the reception permission is within the subscription period or not is determined based on the current date/time data stored in the RAM 107.

If the received data is determined to be transferred to the host PC 200, the host PC 200 is supplied with the received data via the interface 105 (Step 26). If the received data is determined not to be transferred to the host PC 200, the host PC 200 is not supplied with the received data.

When the Layer-4 control information is supplied from the host PC 200 (Step 27), the supplied control information is stored in the EEPROM 108 in correspondence to the broadcasting station code (which is supplied from the host PC 200 at Step 21) associated with the currently selected broadcasting station (Step 28). It is to be noted that in a case where the control information on the currently selected broadcasting station is already stored in the EEPROM 108, the stored control information is replaced by new control information.

When the current date/time data is supplied from the host PC 200 in a predetermined timing (Step 29), the current date/time data stored in the RAM 107 is updated according to the incoming current date/time data (Step 30).

Incidentally, the CPU 104 of the PC card 100 may generate the current date/time data by counting time based on the current date/time data supplied thereto at Step 21. In this case, the processes at Steps 29 and 30 are not necessary.

According to the third embodiment of the invention, the host PC 200 converts the Layer-3 data into the Layer-4 data and therefore, a processing load on the CPU 104 of the PC card 100 is advantageously reduced. This negates the need for installing a high-speed CPU and a RAM of large capacity in the PC card 100, thus contributing to the reduction of costs. Additionally, since the control information is not stored in the hard disk of the host PC 200, there is provided enhanced security of the receiver. Furthermore, the latest control information is retained by the PC card so that there is no need to wait for the reception of new control information when power is turned on or a channel is selected.

It is to be noted that the PC card employed by the foregoing embodiments hereof may be replaced by a receiver unit such as of the board type, box type or the like.

Claims

1. A data broadcasting receiver comprising a receiver unit for performing processes of channel selection,

decoding, error correction and data reception, and a host device supplied with received data from the receiver unit and performing processes of program data reconstruction, program data analysis and program data display,

the receiver unit serving to receive control-information-program data indicative of program-data-reception permission/inhibition to each receiver for transfer thereof to the host device,
the host device, in turn, analyzing the control-information-program data supplied from the receiver unit and transferring an analysis result to the receiver unit,
the receiver unit storing the analysis result supplied from the host device and determining whether or not to transfer received data to the host device based on the analysis result thus stored for transfer of only received data that is determined to be transferred to the host device.

2. A data broadcasting receiver as set forth in Claim 1, wherein the analysis result contains data indicative of either permission or inhibition of the data transfer for each program.

3. A data broadcasting receiver as set forth in Claim 1, wherein the analysis result contains data indicative of either permission or inhibition of the data transfer for a pay-program.

4. A data broadcasting receiver as set forth in Claim 1, wherein the host device comprises a personal computer while the receiver unit comprises a PC card installed in the host device.

5. A data broadcasting receiver comprising a receiver unit for performing processes of channel selection, decoding, error correction and data reception, and a host device supplied with received data from the receiver unit and performing processes of program data reconstruction, program data analysis and program data display,

which receiver unit transfers to the host device control-information-program data of layer 3 indicative of program-data-reception permission/inhibition given to individual broadcasting receivers on a station-by-station has is, which host device, in turn, converts the control-information-program data of Layer 3 from the receiver unit into control-information-program data of Layer 4 and transfers back to the receiver unit the resultant control-information-program data of Layer 4, and which receiver unit, in turn, stores the control-information-program data of Layer 4 from the host device and determines whether or not to transfer received data to the host device based on the control-information-program data of Layer 4 thus stored for transfer of only received data that is determined to be transferred to the host device.

6. A data broadcasting receiver as set forth in Claim 5, wherein the host device comprises a personal computer while the receiver unit comprises a PC card installed in the host device.

FIG. 1

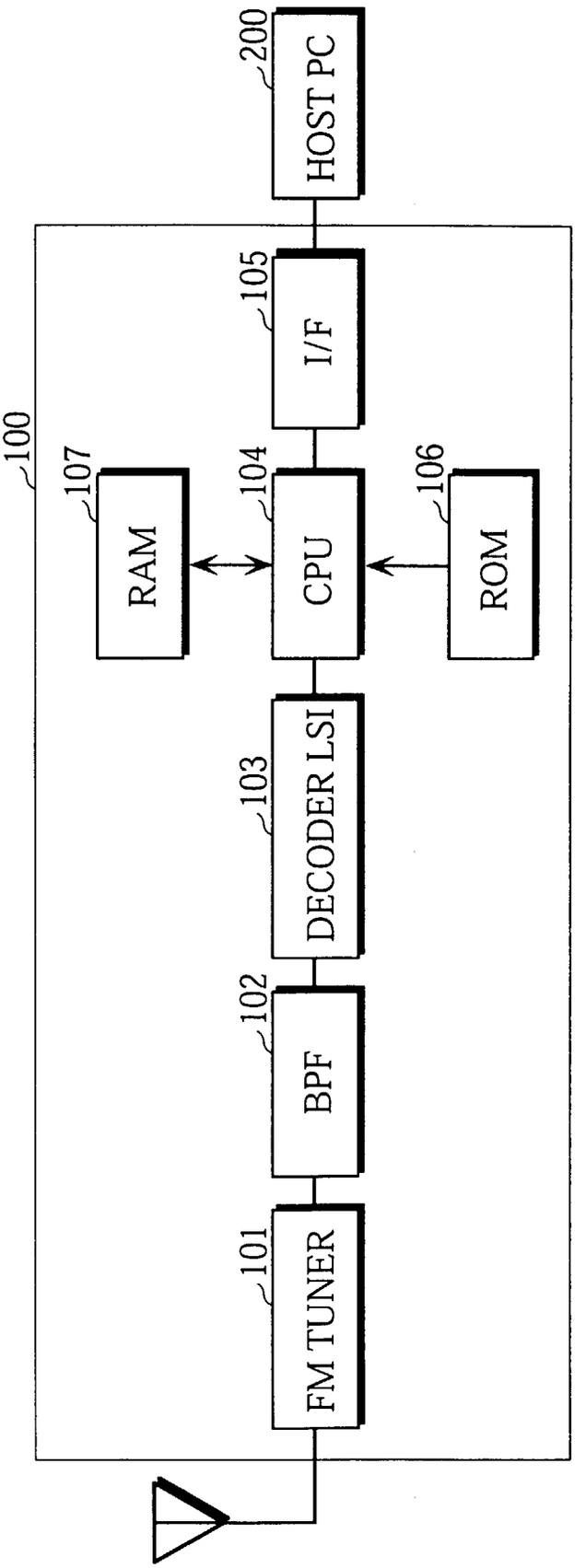

100
101
FM TUNER
102
BPF
103
DECODER LSI
104
CPU
105
I/F
106
ROM
107
RAM
200
HOST PC

FIG. 2

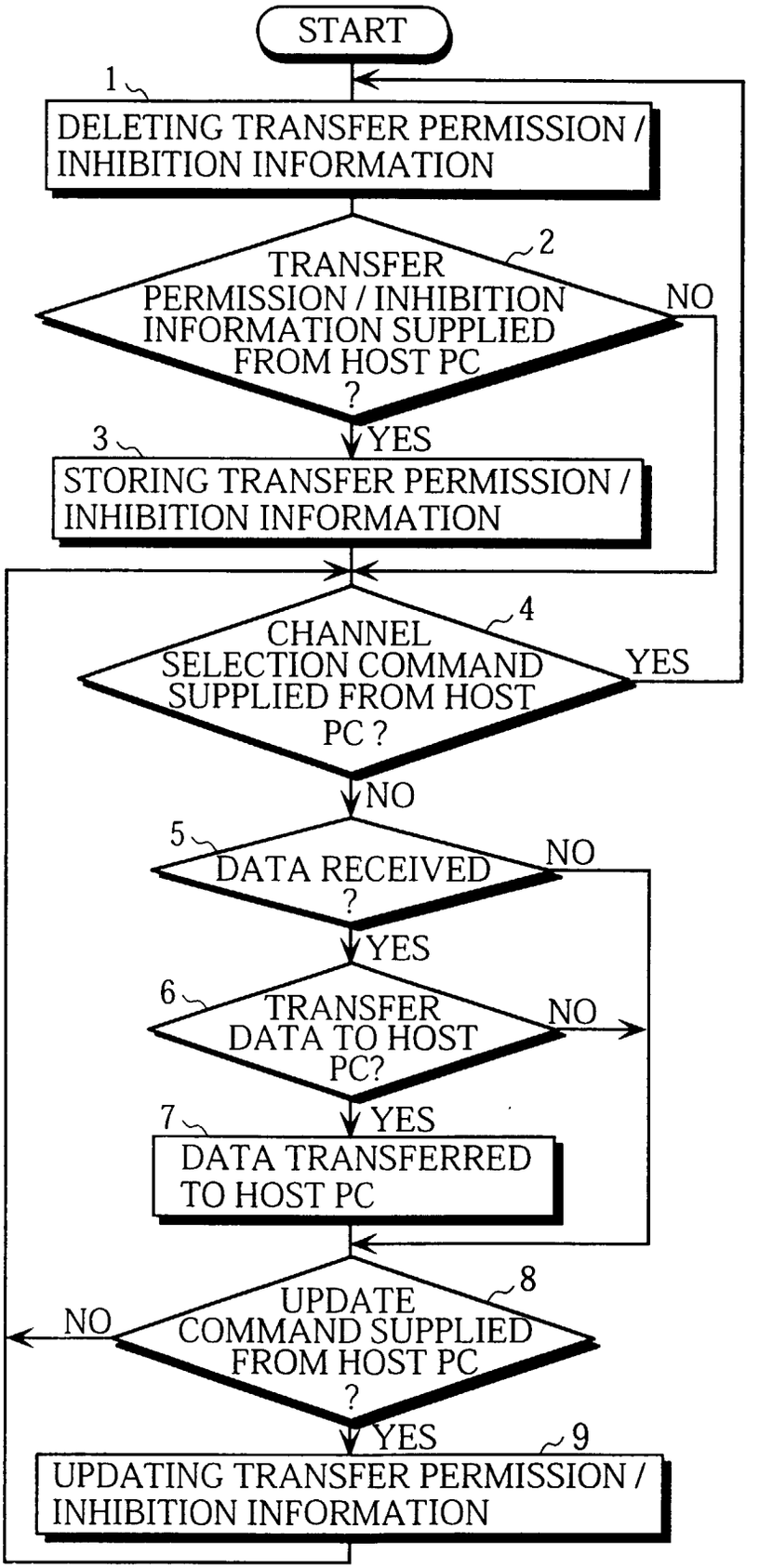

START
1
DELETING TRANSFER PERMISSION / INHIBITION INFORMATION
2
TRANSFER PERMISSION / INHIBITION INFORMATION SUPPLIED FROM HOST PC ?
NO
YES
3
STORING TRANSFER PERMISSION / INHIBITION INFORMATION
4
CHANNEL SELECTION COMMAND SUPPLIED FROM HOST PC ?
YES
NO
5
DATA RECEIVED ?
NO
YES
6
TRANSFER DATA TO HOST PC?
NO
YES
7
DATA TRANSFERRED TO HOST PC
8
UPDATE COMMAND SUPPLIED FROM HOST PC ?
NO
YES
9
UPDATING TRANSFER PERMISSION / INHIBITION INFORMATION

FIG. 3

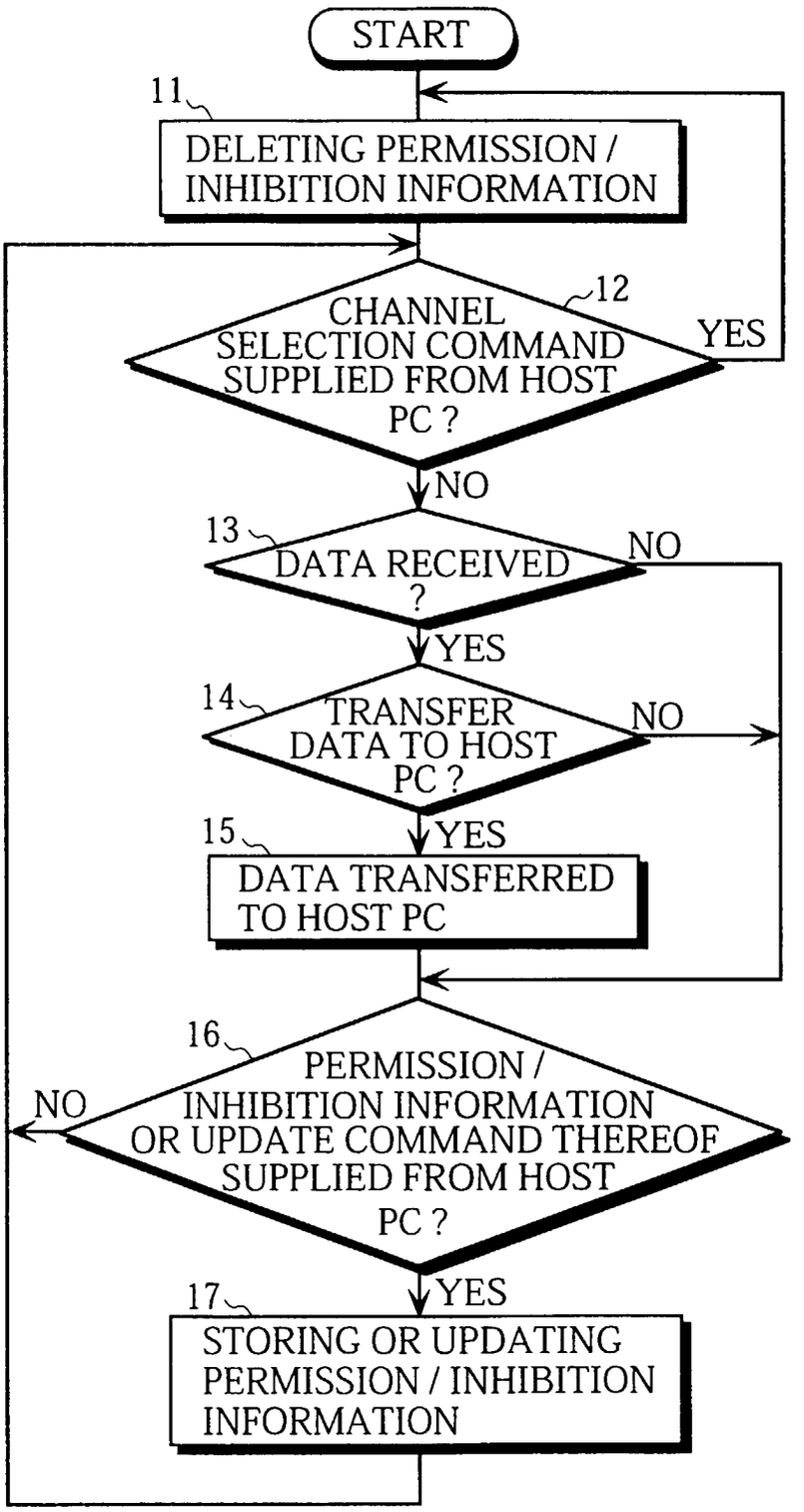

START
11
DELETING PERMISSION / INHIBITION INFORMATION
12
CHANNEL SELECTION COMMAND SUPPLIED FROM HOST PC ?
YES
NO
13
DATA RECEIVED ?
NO
YES
14
TRANSFER DATA TO HOST PC ?
NO
YES
15
DATA TRANSFERRED TO HOST PC
16
PERMISSION / INHIBITION INFORMATION OR UPDATE COMMAND THEREOF SUPPLIED FROM HOST PC ?
NO
YES
17
STORING OR UPDATING PERMISSION / INHIBITION INFORMATION

FIG. 4

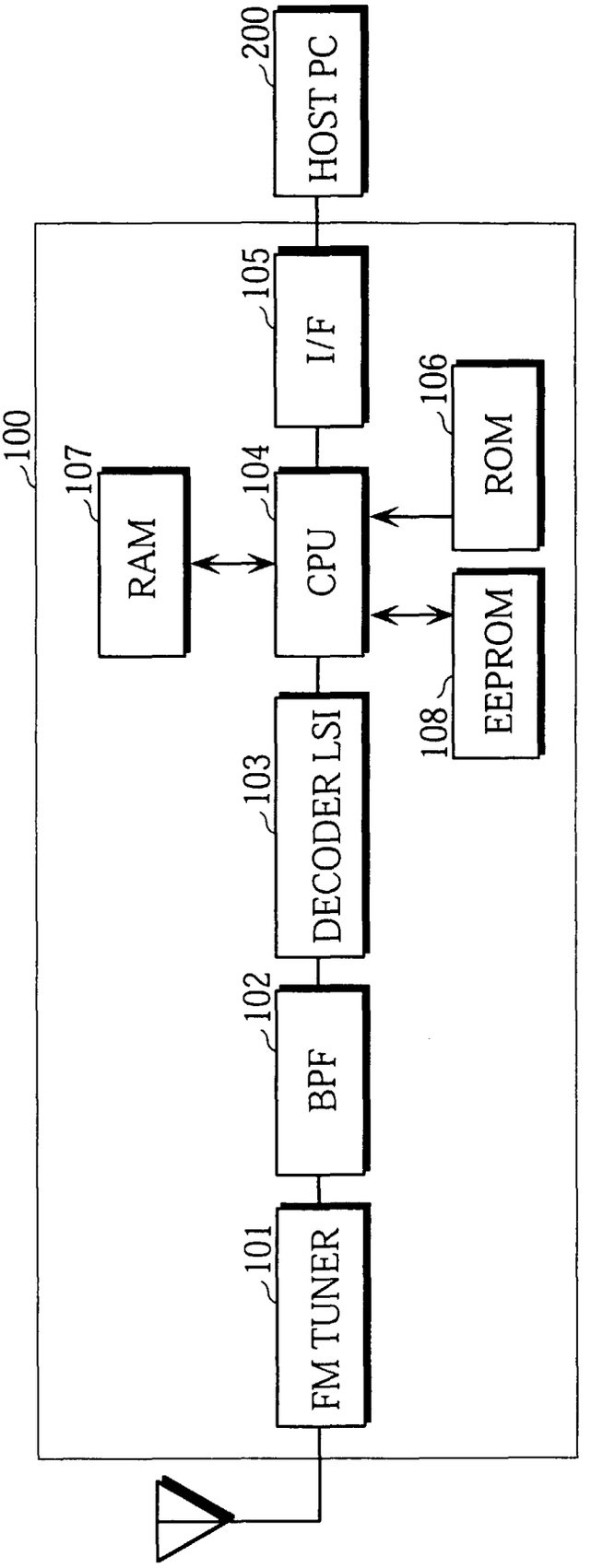

100
101
FM TUNER
102
BPF
103
DECODER LSI
104
CPU
105
I/F
106
ROM
107
RAM
108
EEPROM
200
HOST PC

FIG. 5

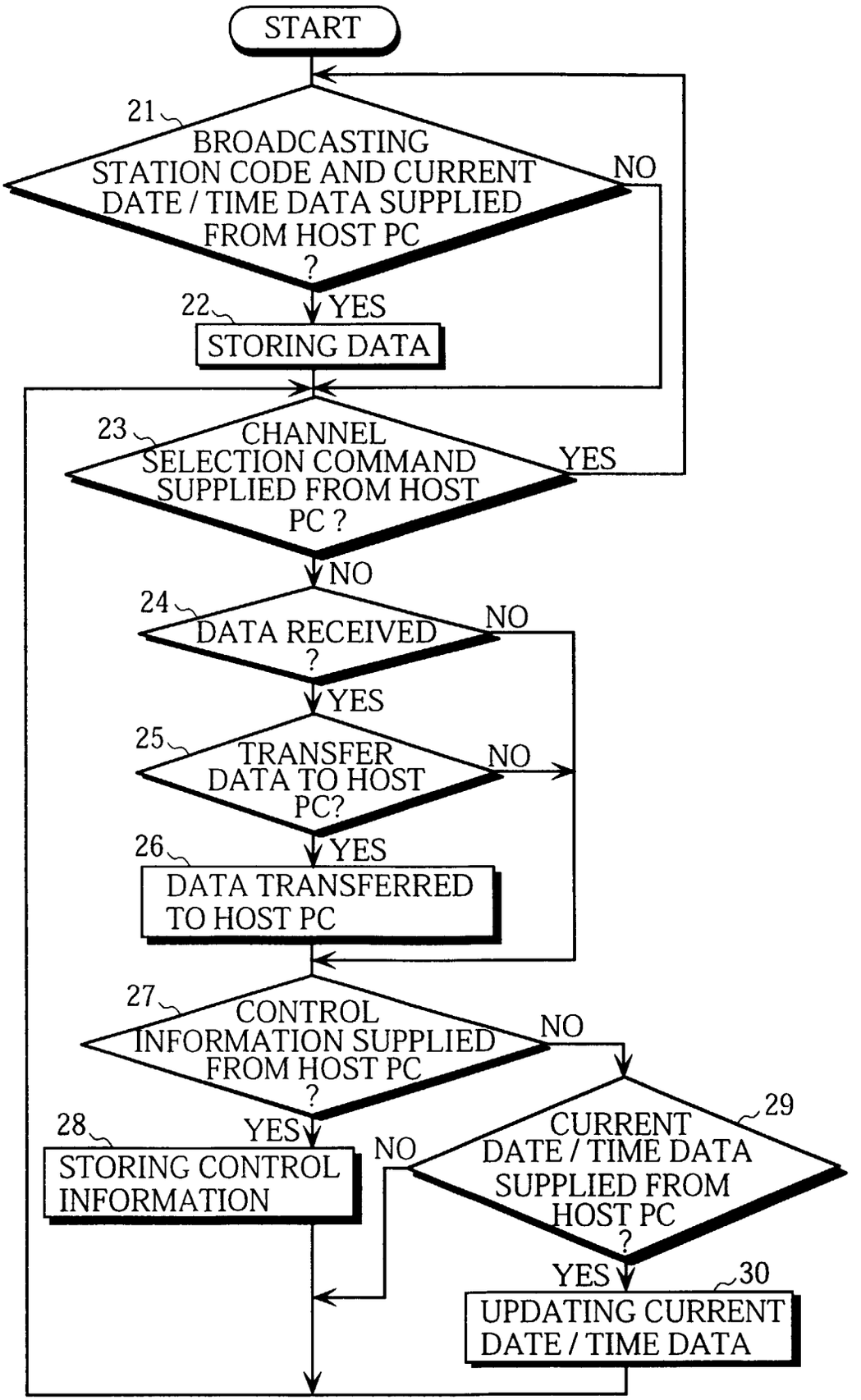

START
21
BROADCASTING STATION CODE AND CURRENT DATE / TIME DATA SUPPLIED FROM HOST PC ?
NO
YES
22
STORING DATA
23
CHANNEL SELECTION COMMAND SUPPLIED FROM HOST PC ?
YES
NO
24
DATA RECEIVED ?
NO
YES
25
TRANSFER DATA TO HOST PC?
NO
YES
26
DATA TRANSFERRED TO HOST PC
27
CONTROL INFORMATION SUPPLIED FROM HOST PC ?
NO
YES
28
STORING CONTROL INFORMATION
29
CURRENT DATE / TIME DATA SUPPLIED FROM HOST PC ?
NO
YES
30
UPDATING CURRENT DATE / TIME DATA

FIG. 6

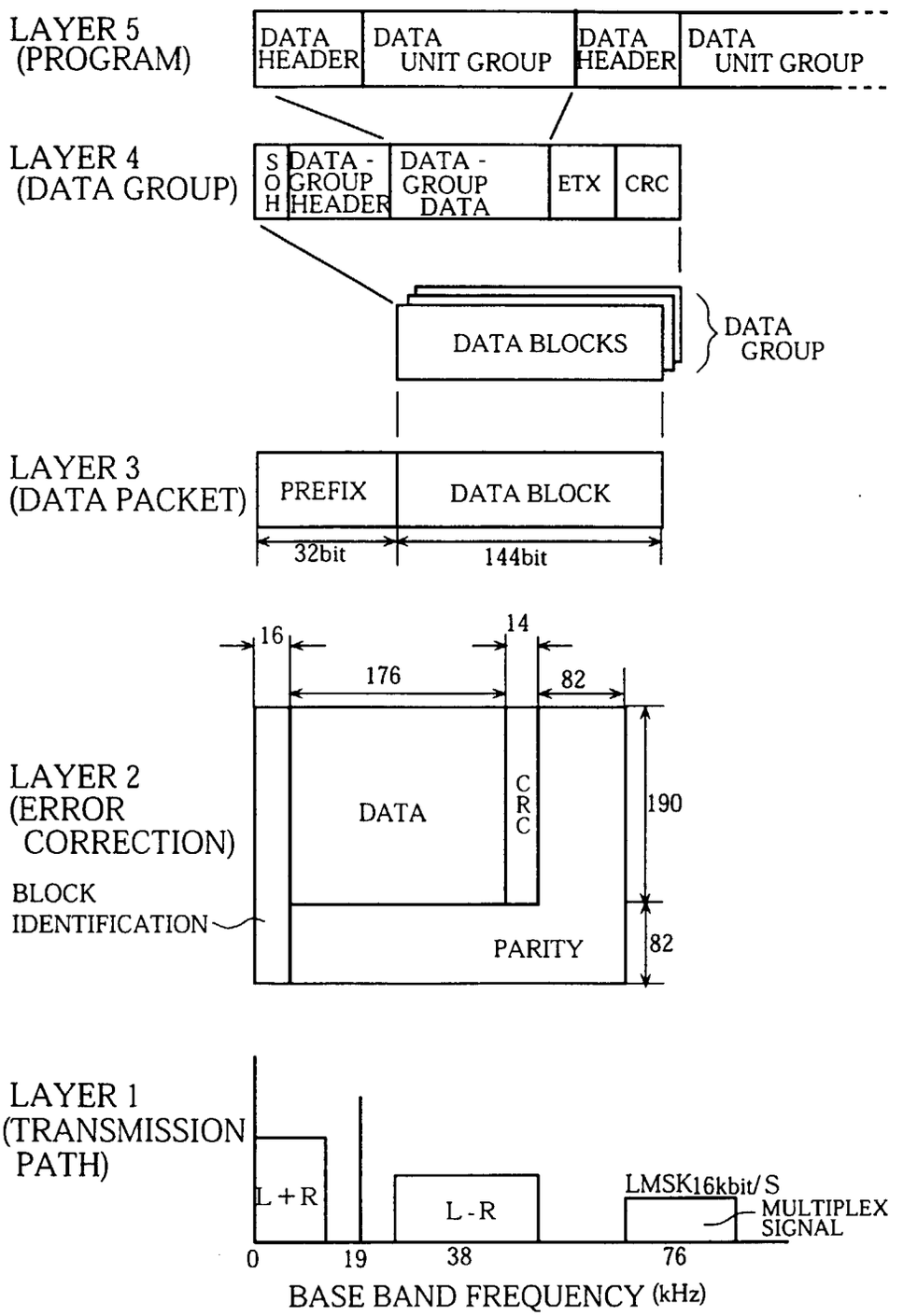

LAYER 5
(PROGRAM)
DATA HEADER
DATA UNIT GROUP
DATA HEADER
DATA UNIT GROUP
LAYER 4
(DATA GROUP)
SOH
DATA - GROUP HEADER
DATA - GROUP DATA
ETX
CRC
DATA BLOCKS
DATA GROUP
LAYER 3
(DATA PACKET)
PREFIX
DATA BLOCK
32bit
144bit
16
14
176
82
LAYER 2
(ERROR CORRECTION)
DATA
CRC
190
BLOCK IDENTIFICATION
PARITY
82
LAYER 1
(TRANSMISSION PATH)
L+R
L-R
LMSK16kbit/S
MULTIPLEX SIGNAL
0
19
38
76
BASE BAND FREQUENCY (kHz)

FIG. 7

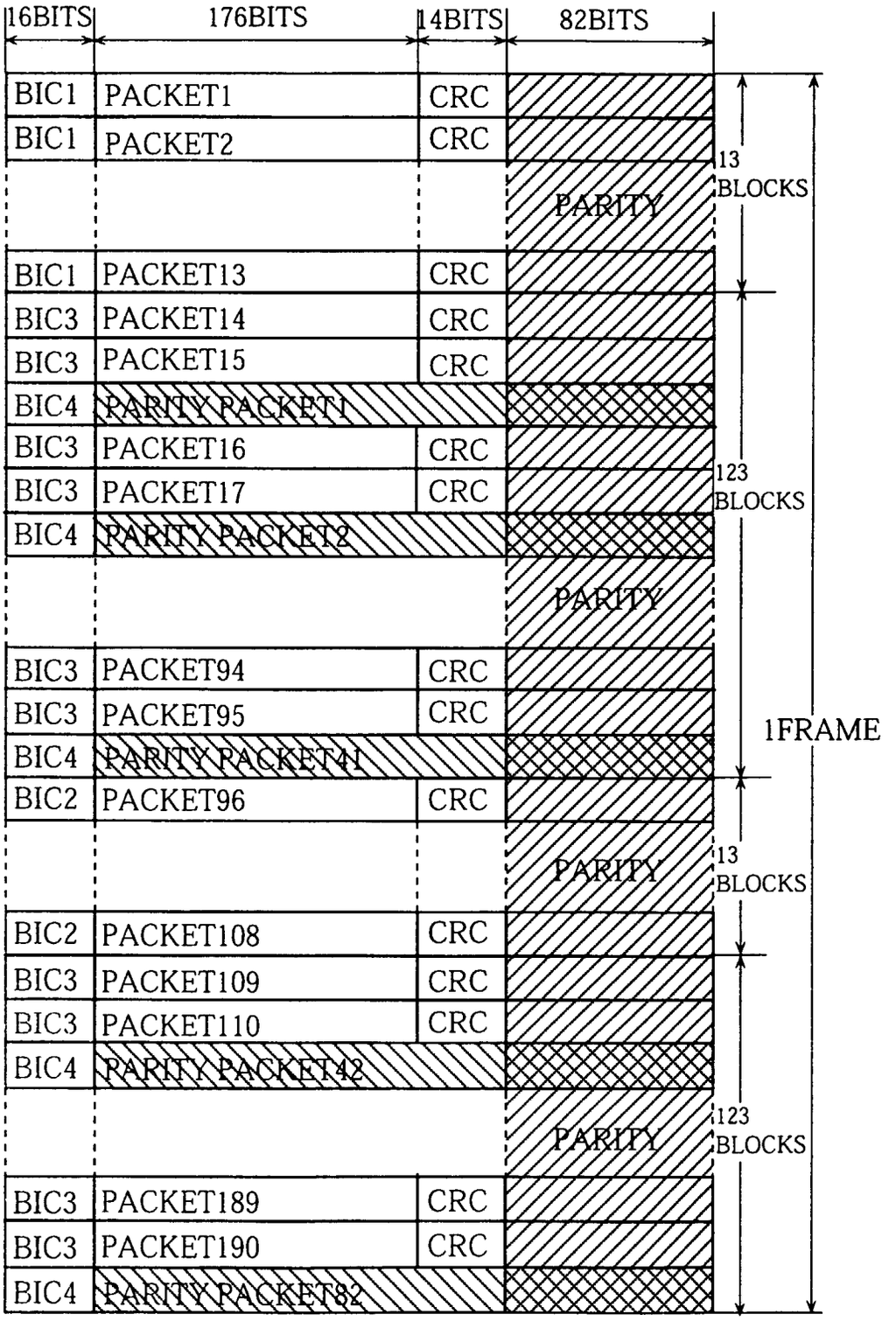
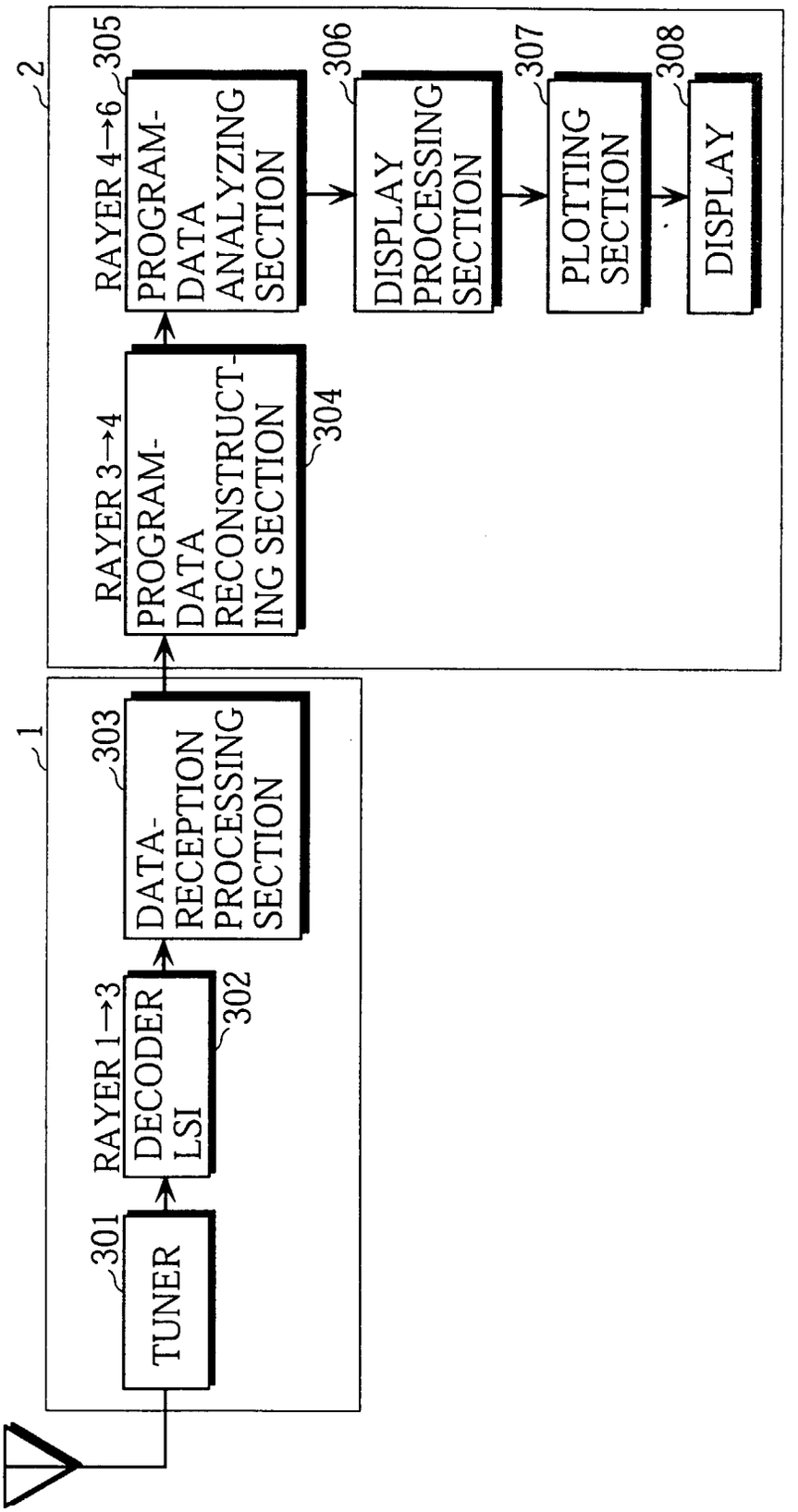

16BITS
176BITS
14BITS
82BITS
BIC1 PACKET1 CRC
BIC1 PACKET2 CRC
PARITY
13 BLOCKS
BIC1 PACKET13 CRC
BIC3 PACKET14 CRC
BIC3 PACKET15 CRC
BIC4 PARITY PACKET1
BIC3 PACKET16 CRC
BIC3 PACKET17 CRC
BIC4 PARITY PACKET2
PARITY
123 BLOCKS
BIC3 PACKET94 CRC
BIC3 PACKET95 CRC
BIC4 PARITY PACKET41
BIC2 PACKET96 CRC
PARITY
13 BLOCKS
BIC2 PACKET108 CRC
BIC3 PACKET109 CRC
BIC3 PACKET110 CRC
BIC4 PARITY PACKET42
PARITY
123 BLOCKS
BIC3 PACKET189 CRC
BIC3 PACKET190 CRC
BIC4 PARITY PACKET82
1FRAME

FIG. 8


1
2
301
TUNER
RAYER 1→3
DECODER LSI
302
303
DATA-RECEPTION PROCESSING SECTION
RAYER 3→4
PROGRAM-DATA RECONSTRUCTING SECTION
304
RAYER 4→6
PROGRAM-DATA ANALYZING SECTION
305
306
DISPLAY PROCESSING SECTION
307
PLOTTING SECTION
308
DISPLAY