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(54) Active pixel image sensor with shared amplifier read-out

(57) An image sensor having a plurality of pixels arranged in a series of row and columns comprising: a semiconductor substrate having a plurality of pixels formed in rows and columns with at least two row adjacent pixels and at least two column adjacent pixels formed within the substrate; and at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels. The electrical function can be either a contact region or an electrical circuit used in implementing either a photogate, a transfer gate, a reset gate, a row select gate, an amplifier drain, an output node, a floating diffusion contact, a reset drain, a lateral overflow gate, an overflow drain or an amplifier.

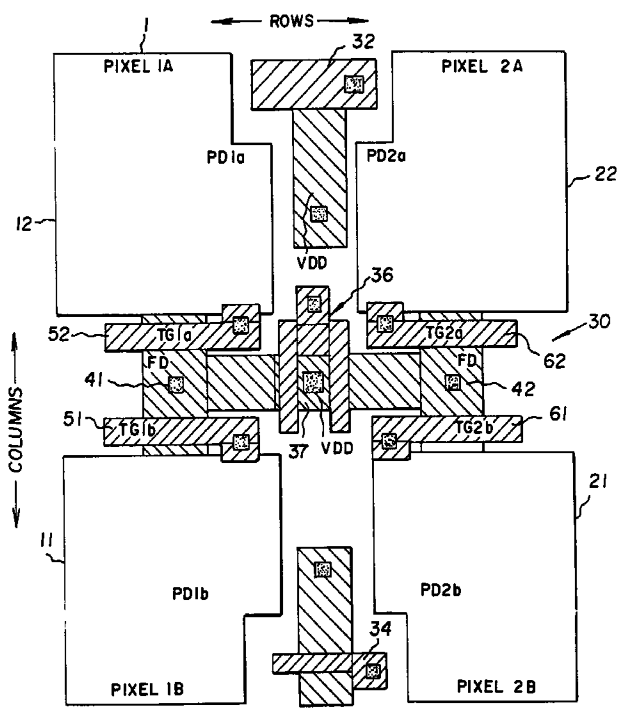

FIG. 3a

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Description

[0001] The present application is related to U.S. Application Serial Number 08/808,444 filed February 28, 1997 by Robert M. Guidash and entitled, "ACTIVE PIXEL SENSOR WITH INTER-PIXEL SHARING".

[0002] This invention relates to the field of solid state photo-sensors and imagers, and more specifically to semiconductor based imagers referred to as Active Pixel Sensors (APS).

[0003] Active Pixel Sensors (APS) are solid state imagers wherein each pixel contains a photo-sensing means with associated active circuitry elements. These active circuitry elements typically are means to perform a pixel reset function, or some means to transfer charge, means to perform a voltage conversion, or circuitry elements used in amplification. APS devices have been operated in a manner where each line or row of the imager is selected and then read out using a column select signal (analogous to a word and bit line in memory devices respectively). Prior art devices have been disclosed in which all of these components have been located entirely within a single pixel boundary.

[0004] Inclusion of these active circuit element components in each pixel reduces the fill factor for the pixel because it takes up area that could otherwise be used for the photodetector. This reduces the sensitivity and saturation signal of the sensor which in turn adversely affects the photographic speed and dynamic range of the sensor, performance parameters that are critical to obtaining good image quality. Additionally, inclusion of these active circuit elements within the pixel places a limitation on the minimum size of the pixel, which adversely affects the size and cost of the image sensor.

[0005] In order to build high resolution, small pixel APS devices, it is necessary to use sub μm CMOS processes in order to minimize the area of the pixel allocated to the row select transistor and other parts of the amplifier in the pixel. In essence, it takes a more technologically advanced and more costly process to realize the same resolution and sensitivity APS device when compared to a standard charge coupled device (CCD) sensor. However, APS devices have the advantages of single 5V supply operation, lower power consumption, x-y addressability, image windowing and the ability to effectively integrate signal processing electronics on-chip, when compared to CCD sensors.

[0006] A typical prior art APS pixel is shown in Fig. 1. The pixel comprises a photodetector 14, that can be constructed from either a photodiode or photogate technology, a transfer gate 15, a floating diffusion 16, reset transistor 18 with a reset gate 19, a row select transistor 8 with a row select gate 9, and signal transistor 7 which is a source follower amplifier. Inclusion of all these components within a single pixel results in a reduction in the fill factor, sensitivity and minimum size of the pixel.

[0007] Referring to Fig. 2A in conjunction with Fig. 2B, one approach to providing an image sensor with the sensitivity of a CCD and the advantages of an APS device, is to improve the fill factor and sensitivity of an APS device by reducing the amount of area allotted to components within a single pixel while maintaining the desired features and functionality of the pixel architecture.

[0008] Referring to Fig. 2A in conjunction with Fig. 2B, US Patent application 08/808,444, entitled "Active Pixel Sensor With Inter-Pixel Function Sharing" by Guidash discloses a manner in which fill factors for APS devices can be increased. This prior art device of Guidash teaches the sharing of various components typically employed within an Active Pixel Sensor. Sharing of the floating diffusion, source follow amplifier, row select transistor, and reset transistor between two row adjacent photodetectors and transfer gates are disclosed here to assist in increasing the fill factor of the pixel architecture. The basic concept utilized by Guidash for increasing fill factor is the fact that a row at a time is read out during operation of the sensor. Accordingly, Guidash was able to provide a single floating diffusion 26 and a single amplifier 27 for pixels located in two adjacent rows, instead of requiring one for every pixel as in the APS device shown in Fig. 1. Since only one row is read out at a time, a single floating diffusion 26, reset transistor 28, row select transistor 29 and signal transistor 27 (typically a source follower transistor) can be used for two adjacent pixels in separate rows.

[0009] While allowing for the sharing of components and increasing the fill factors within active pixel sensors, the device shown in Fig. 2 does not allow for the combining of function between both rows and columns, and accordingly the increase in fill factor that would result from such an architecture.

[0010] It should be readily apparent from the foregoing discussion that there remains a need within the art for an APS architecture that will allow for the combining of electrical functions between row as well as column pixels and the resulting increase in fill factor.

[0011] This invention addresses the aforementioned problems within prior art Active Pixel Sensor (APS) devices. It comprises a pixel and column circuitry architecture innovation that provides a higher fill factor pixel or a smaller pixel. By sharing components between adjacent columns and adjacent rows, components can be shared by four (4) separate photodetectors and transfer gates instead of two (2). This invention provides a means to further improve fill factor and further diminish the minimum pixel size by sharing the aforementioned components additionally between two column adjacent photodetectors and transfer gates, so that these components are now shared by four separate photodetectors and transfer gates, while maintaining the ability to selectively address specific pixels of the APS device.

[0012] Briefly summarized, according to one aspect of the present invention is an image sensor having a plurality of pixels arranged in a series of rows and columns comprising: a semiconductor material of a first conductivity type having at least two adjacent row pixels and at least two adjacent column pixels formed within the substrate, and at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels.

[0013] These and other aspects, objects, features, and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

[0014] The present invention has the following advantages:

[0015] High fill factor, sensitivity and saturation signal for the same pixel size.

[0016] Smaller pixel and device size for the same fill factor, providing a lower cost device.

Fig. 1A is a top view of a prior art pixel;

Fig. 1B is a schematic drawing of pixel shown in Fig. 1A.;

Fig. 2A is a top view of a prior art pixel with shared functionality;

Fig. 2B is a schematic view of the prior art pixel with shared functionality shown in Fig 2A;

Fig. 3A is a top view of the pixel architecture with shared functionality as envisioned by the present invention;

Fig. 3B is a schematic view of the pixel architecture shown in Fig 3A; and

Fig. 4 is a timing diagram illustrating the operation of the present invention.

[0017] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

[0018] I have discovered a pixel architecture wherein a smaller pixel size can be achieved by sharing functions between the adjacent pixels resulting in a smaller overall sensor device while still retaining as large a fill factor as larger sized sensor devices. This results in a lower cost device with a pixel size as large as existing prior art devices and having a higher fill factor with increased sensitivity and saturation signal is achieved.

[0019] Referring to Fig. 3a seen in conjunction with Fig. 3b, the preferred embodiment of the invention that represents one physical embodiment of the new pixel architecture can be appreciated. Other specific physical embodiments are realizable and should be readily apparent to those skilled in the art. This new architecture seen in Fig. 3a and Fig. 3b, generally referred to as 30, envisions sharing electrical functions between pixels 11, 12, 21, and 22 that are arranged as row adjacent pixels 11, 12 and 21, 22 and column adjacent column pixels 11, 21 and 12, 22. Fig. 3a illustrates a top view of pixel architecture 30 while Fig. 3b provides a schematic representation of the device shown in Fig. 3a. As can be seen, pixel architecture 30 provides a shared floating diffusion 41 between row adjacent pixels 11, 12 in row 1, and a shared floating diffusion 42 between row adjacent pixels 21, 22. Amplifier 32 is preferably a source follower transistor configuration that is shared between all four of the shared pixels 11, 12, 21, and 22, as is row select transistor 34, and reset transistor 36.

[0020] As shown in Fig. 3a and Fig. 3b, the row select signal buss 35 for both rows 1, 2 is the same, and the column output buss 37 for both columns a, b is actually the same. Image signal separation is achieved by having separate transfer gates 51, 52, 61 and 62 for each of the adjacent pixels 11, 12, 21, and 22. Separate transfer gate busses for every other pixel within a row, and a 1:2 column buss de-multiplexing scheme for each pair of columns.

[0021] Referring now to Fig. 4 which is a timing diagram detailing one mode of operation of this new architecture in conjunction with Fig. 3a and Fig. 3b, The image sensor 30 is powered up in its reset state, with all the transfer gates TG1b 51, TG1a 52, TG2b 61 and TG2a 62 as well as the reset gate 37 turned on. Integration of row 1 begins by turning TGa1 52 off, which begins the integration for the odd pixels in row 1, which includes pixel 12. A predetermined time later transfer gate TG1b 51 is turned off, which begins the integration of the even pixels within row 1 which would include pixel 12 as illustrated. Once row 1 has integrated for the desired period of time row select gate 35, and the col. A transistor 81 is turned on, (col. B transistor 91 is off). The reset level of the floating diffusion 41 is then read by turning reset gate 37 off and strobing SHR 82. Transfer gate TGa1 52 is then pulsed on and the signal charge from photodetector PD1a 72 is transferred onto the floating diffusion 41. The signal level is then read out for the odd row photodetectors in Row 1 by strobing SHS 83. While the integrated charge for pixel 12 was being transferred, pixel 11 was still allowing photodetector Pdb1 71 to integrate. The transfer of the integrated charge within pixel 11, takes place when Col. A transistor 81 is turned off and the Col. B transistor 91 is turned on. Reset gate 37 is turned on again, resetting the floating diffusion 41. The reset level is then read out by strobing SHR. Next, transfer gate Tgb1 51 is pulsed on at the appropriate time, which is determined to be that amount of time such that Pda1 72 and Pdb1 71 have the same integration time. The signal charge within photodetector PDB2 in pixel 11 is then transferred onto the floating diffusion 41 (this is the case for all of the even row photodetectors within Row 1). The signal level is then read by strobing SHS 83. Now all of the pixels in Row 1 have been read-out in to the bank of signal and reset capacitors. The line read-out is then done in the standard manner described in prior art CMOS imagers. This same sequence is then done for Row 2, where all of the signals are the same except transfer gate 62 TG2a and TG2b 61 are used. This procedure is then repeated for the remaining pairs of rows on the device.

This operation can be described conceptually as column interlaced, sample and hold, per row operation.

[0022] This architecture provides high fill factor and a resulting very small pixel size compared to prior art devices, since the active components are shared among four 4 photodetectors. One extra metal line per row is required, to provide all the required transfer gates, but this takes up much less area than that occupied by the active components in both the per pixel amplifier scheme and the per 2 pixel amplifier scheme, discussed previously. There are 3 extra timing and control signals required and 2 additional transistors per column required. However, these do not impact the pixel or image array area since they are incorporated in the CMOS logic outside of the image array. In addition to the temporal displacement of image capture on a per row basis, this architecture also has a temporal displacement of image capture of odd and even pixels within a given row. This time is very short however, (especially compared to the row to row temporal displacement), on the order of a few hundred nanoseconds, and will not produce any image capture artifacts. Because there is an extra sequence of sample and holds, (SHR and SHS strobes), the minimum line time is slightly longer for this new architecture, which will incrementally diminish the maximum frame rate for video applications.

1	row 1
2	row 2
3	row 3
4	row 4
7	signal transistor
8	row select transistor
9	row select gate
10	prior art pixel
11	pixel
12	pixel
14	photodetector
16	floating diffusion
18	reset transistor
19	reset gate
20	
21	pixel
22	pixel
24	
26	floating diffusion
27	signal transistor
28	reset transistor
29	select transistor
30	shared row and column circuit pixels
32	floating diffusion amplifier
34	row select transistor
35	row select gate
36	reset transistor
37	reset gate
38	column output buss
40	
41	floating diffusion
42	floating diffusion
51	transfer gate
52	transfer gate
61	transfer gate
62	transfer gate
71	photodetector
72	photodetector
80	column sample hold
81	transistor
82	sample and hold reset
83	sample and hold signal
90	column sample hold
91	transistor
92	sample and hold reset

Claims

1. An image sensor having a plurality of pixels arranged in a series of row and columns comprising:

   a semiconductor material of a first conductivity type;
   at least two row adjacent pixels and at least two column adjacent pixels formed within the substrate; and
   at least one electrical function integrated within the adjacent pixels that is shared between the adjacent pixels.

2. The image sensor of claim 1 wherein the shared electrical function further comprises a shared contact region.

3. The image sensor of claim 2 wherein the electrical contact is selected from one of the following components (a photogate contact, a transfer gate contact, a reset gate contact, a row select gate contact, an amplifier drain contact, an output node contact, a floating diffusion contact, a reset drain contact, a lateral overflow gate contact, an overflow drain contact or an amplifier contact).

4. The image sensor of claim 1 wherein the shared function further comprises a shared electrical component

5. The image sensor of claim 1 wherein the shared function further comprises a shared contact region but not a shared electrical component between the adjacent pixels.

6. The image sensor of claim 1 wherein the shared function further comprises both a shared contact region and a shared electrical component.

7. The image sensor of claim 6 wherein the electrical

component is selected from one of the following components (a transfer gate, a reset transistor, a row select transistor, an amplifier drain, an output node, a floating diffusion, a lateral overflow gate, an overflow drain or an amplifier).

8. A method of making solid state image sensing devices comprising the steps of:

providing a semiconductor substrate having a plurality of pixels formed in columns and rows; and

further providing within at least two row adjacent and two column adjacent pixels one electrical function that is shared between the adjacent pixels.

9. The method of claim 8 wherein the step of further providing further comprises providing the shared function such that it is shared essentially equally between the adjacent pixels.

10. The method of claim 8 wherein the step of further providing includes providing the shared function such that it performs a first function for one of the adjacent pixels and a second function for the other adjacent pixel.

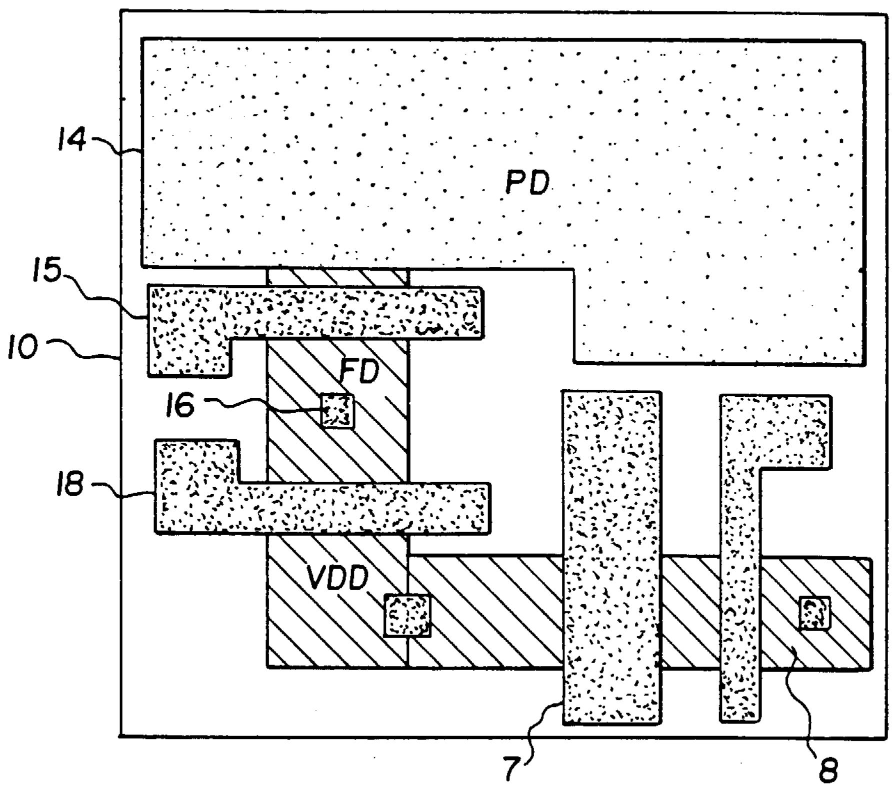

FIG. 1A PRIOR ART

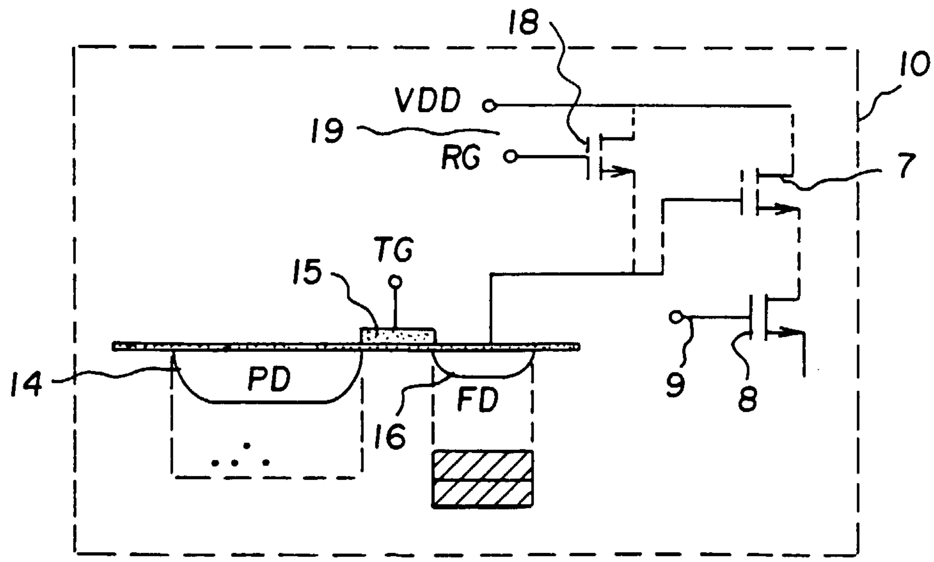

FIG. 1B

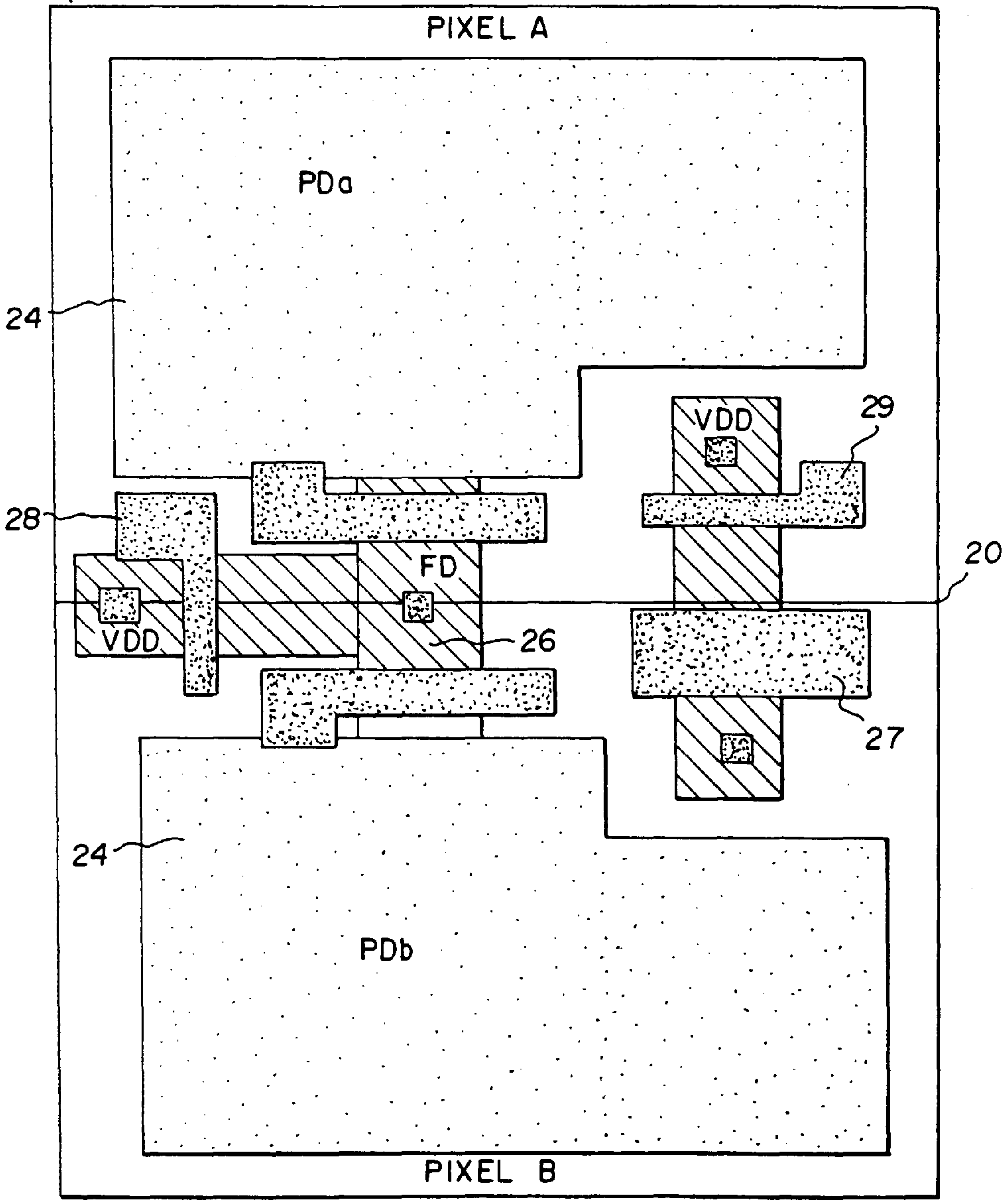

FIG. 2A PRIOR ART

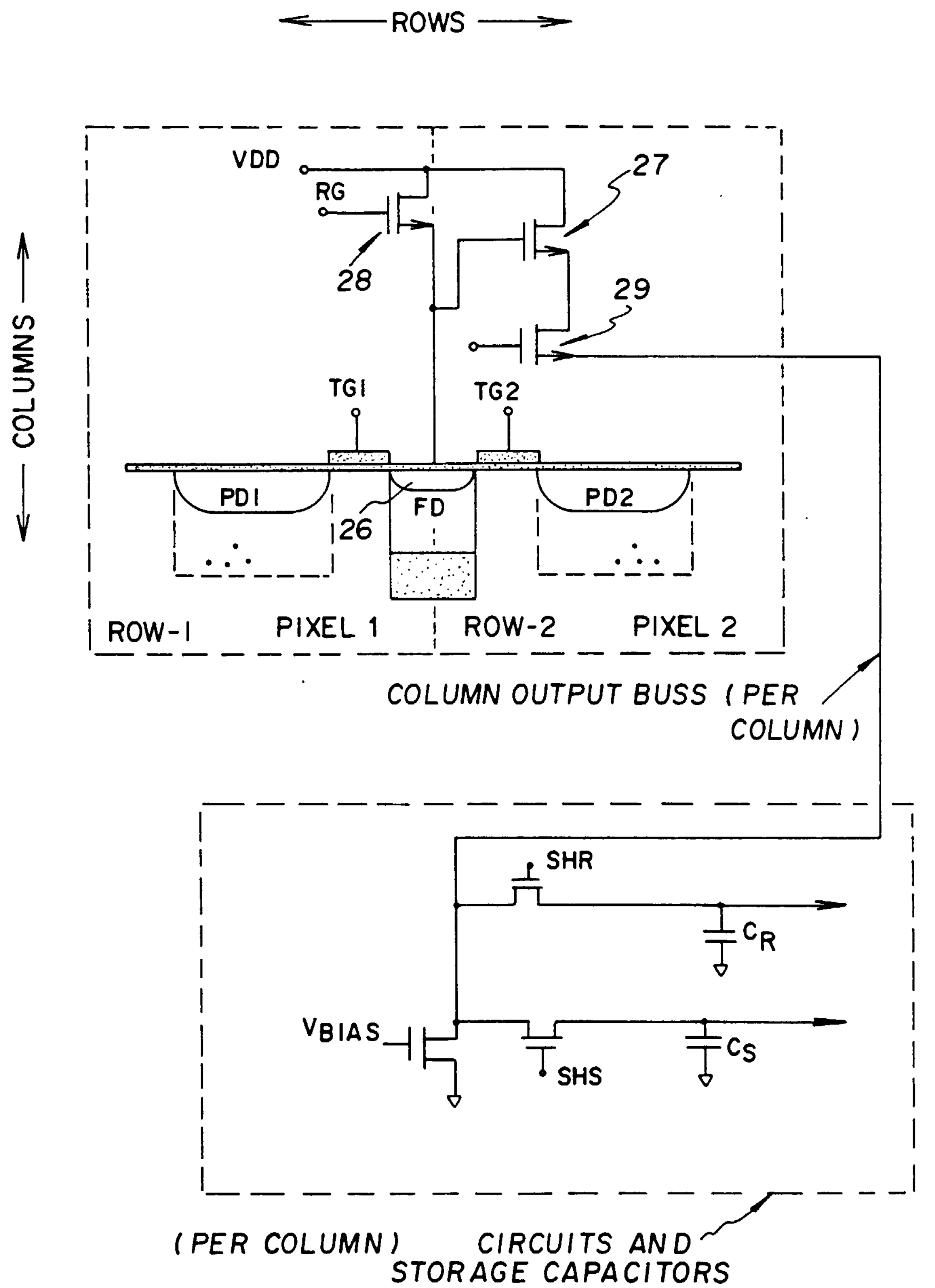
ROWS
COLUMNS
VDD
RG
27
28
29
TG1
TG2
PD1
FD
26
PD2
ROW-1
PIXEL 1
ROW-2
PIXEL 2
COLUMN OUTPUT BUSS (PER COLUMN)
SHR
C_R
V_{BIAS}
SHS
C_S
(PER COLUMN) CIRCUITS AND STORAGE CAPACITORS

FIG. 2B

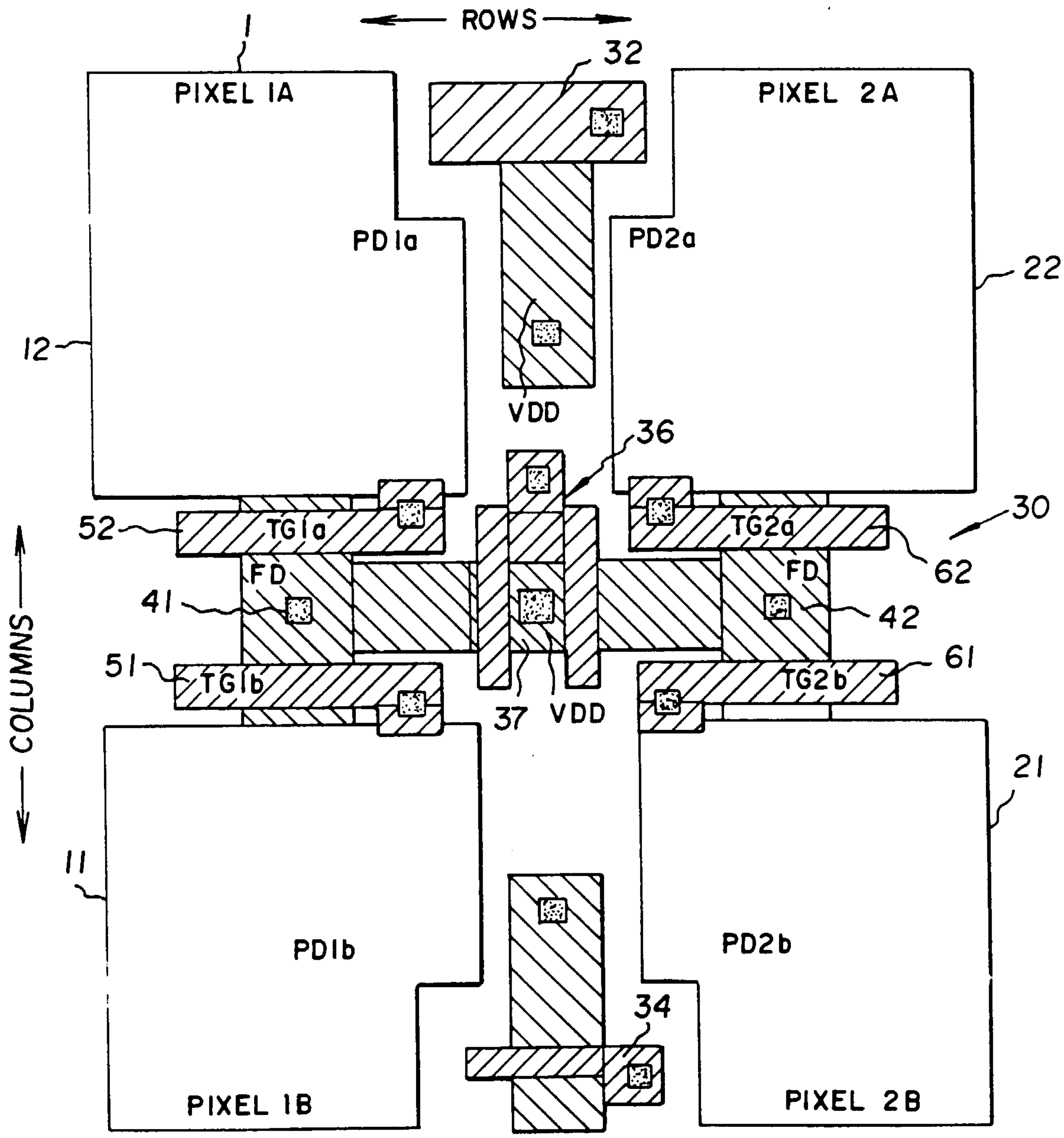
ROWS
COLUMNS
PIXEL 1A
PIXEL 2A
PIXEL 1B
PIXEL 2B
PD1a
PD2a
PD1b
PD2b
VDD
VDD
TG1a
TG1b
TG2a
TG2b
FD
FD
1
12
11
22
21
30
32
34
36
37
41
42
51
52
61
62

FIG. 3a

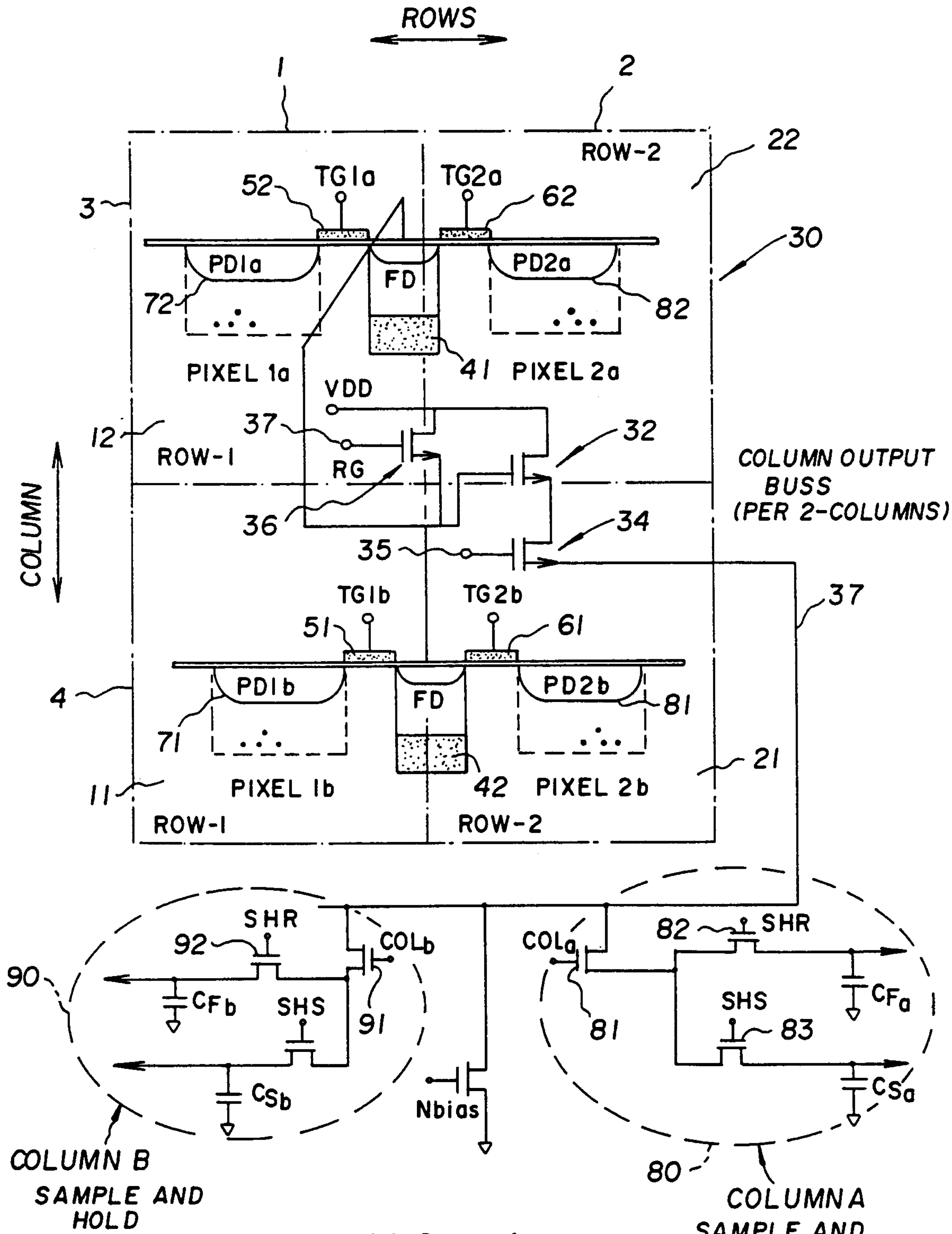
ROWS
1
2
ROW-2
22
3
52
TG1a
TG2a
62
30
PD1a
FD
PD2a
72
82
41
PIXEL 1a
PIXEL 2a
VDD
37
32
12
ROW-1
RG
COLUMN OUTPUT
BUSS
(PER 2-COLUMNS)
COLUMN
36
35
34
TG1b
TG2b
37
51
61
PD1b
FD
PD2b
81
4
71
42
21
11
PIXEL 1b
PIXEL 2b
ROW-1
ROW-2
SHR
COLb
COLa
82
SHR
92
90
CFb
SHS
91
SHS
CFa
81
83
CSb
Nbias
CSa
80
COLUMN B
SAMPLE AND
HOLD
COLUMN A
SAMPLE AND
HOLD

FIG. 3b

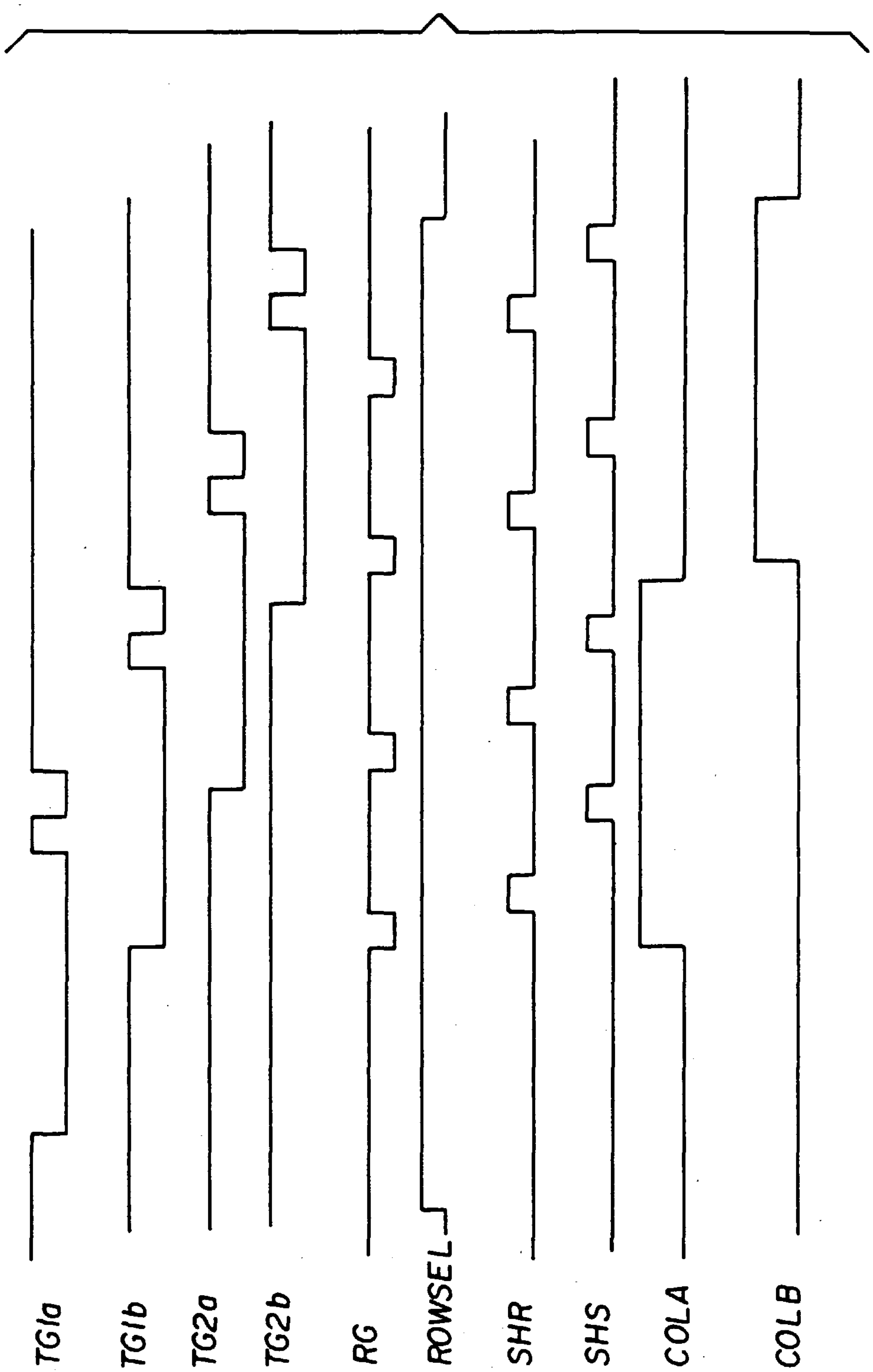

FIG. 4