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(54) Method and circuit for generating a gate voltage in non-volatile memory devices

(57) The present invention relates to a circuit for generating a regulated voltage (RV), in particular for gate terminals of non-volatile memory cells of the floating gate type, which comprises a generator circuit (OSC,CHP) adapted to generate an unregulated voltage (VCHP) on its output, a comparator circuit coupled to the output of the generator circuit (OSC,CHP), including a reference element consisting of a non-volatile memory cell (REFC) of the floating gate type and adapted to output an electric error signal (ID) tied to the difference between the unregulated voltage (VCHP) and the threshold voltage of the cell (REFC), and a regulator circuit (CSEL,CBIAS,IVC,DRV,TR) coupled to the output of the comparator circuit and operative to regulate the unregulated voltage (VCHP) based on the value of the electric error signal (ID). Through the present circuit, the regulated voltage (RV) is made programmable and tied to the parameters of the memory cell (REFC).

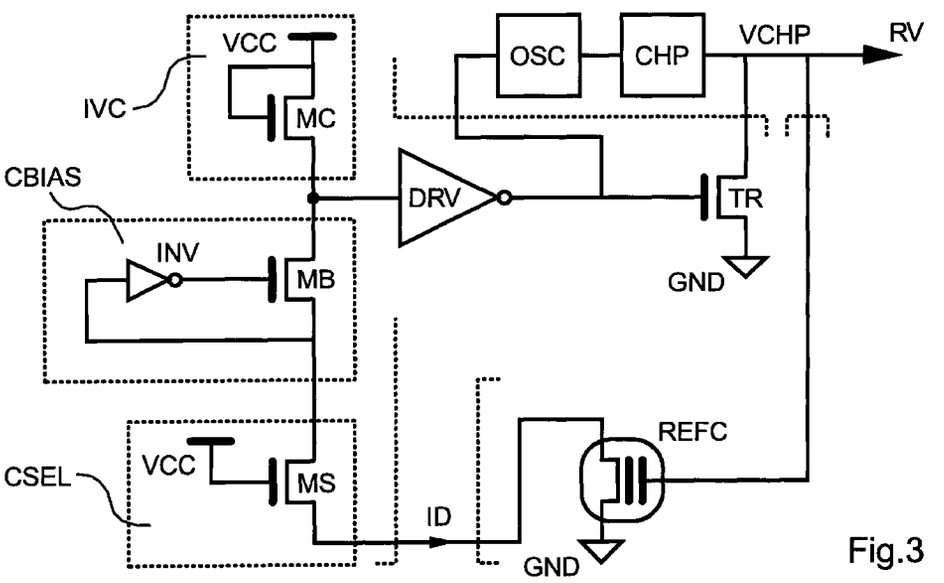

Fig.3

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Description

[0001] This invention relates to a method and a circuit for generating a regulated voltage, respectively according to the preambles of Claims 1 and 7.

[0002] Voltage regulators are circuits which have been employed for years by the electronic industry. More recently, they made their inception in non-volatile storage devices which comprise cells consisting of MOS transistors with a floating gate terminal, such as memories of the EPROM, EEPROM and FLASH types. In fact, a reducing supply voltage, expanding integration scale, and growing amount of binary information to be stored in a single cell, lead to the need of read, write and erase signals controlled with greater accuracy.

[0003] A non-volatile storage system of the multi-level type is known from Patent Application EP 394 705. This includes a gate voltage generation circuit, shown in Figure 4(a), which is formed of a clock pulse generator 40, a charge pump circuit 60, and a regulator circuit 100, all connected in cascade with one another, as well as of a voltage control circuit 80 having its input connected to the output of the circuit 60 and its output connected to a stop terminal of the circuit 40. The voltage control circuit 80 includes a comparator 86 having a negative input connected to ground through a load resistor 84, and a positive input for receiving a data voltage signal which has a value in the 0 to 5 volts range, and a Zener diode 82 having a Zener voltage of 15 volts, a cathode connected to the input of the control circuit 80, and an anode connected to the negative input of the comparator 86; the output of the comparator 86 is connected to the output of the control circuit 80.

[0004] The operation of this gate voltage generation circuit follows readily from Figure 4(b). Regulation is realized at a value equal to the combined data and Zener voltages. It should be noted, however, that during a cell reading operation, the gate of the memory cell is applied the 5 volt supply voltage VDD, as shown in Figure 9.

[0005] Another gate voltage generation circuit for use in non-volatile memories of the multi-level or the low supply voltage type is known from Patent Application EP 656 629; during the reading operation, the gate voltage is supplied by a charge pump circuit driven by an oscillator, and has a higher value than the system supply voltage in order to provide for an ample working margin between storage states. The resulting voltage is then regulated by a Zener diode, as shown in Figure 3.

[0006] Both prior regulators are based on a highly accurate reference element consisting of a Zener diode. Accordingly, the regulated voltage value is set at the designing stage, and cannot be changed either by the user or by the manufacturer at the EWS (Electrical Wafer Sort) stage, for example. Also, the Zener diodes are not always easy to integrate with CMOS technology.

[0007] In addition, the performance of memory cells changes over time, e.g. with temperature variations. Thus, for a given storage state and a given reading gate voltage value, the current flowing through a cell may take significantly different values. This sets the choice of large working margins.

[0008] This invention is directed to providing a method and a circuit for generating a regulated voltage, particularly for gate terminals of non-volatile memory cells of the floating gate type, which can obviate the drawbacks of the prior art.

[0009] This object is achieved by a method and a circuit having the functions and characteristics set forth in Claims 1 and 7, respectively. Further advantageous aspects are set forth in the subclaims.

[0010] If a non-volatile memory cell of the floating gate type is used for the regulating operation, the regulated voltage value can be programmed, and tracks automatically any changes in the performance of memory cells to be read from.

[0011] The present invention also relates to a non-volatile storage device as defined in Claim 12, whereto this method and circuit can be applied to advantage.

[0012] The invention can be better understood by reading the following description along with the accompanying drawings, in which:

Figure 1 is a schematic, fragmentary block diagram of a FLASH storage device of the multi-level type;

Figure 2 illustrates the distribution of the cell threshold voltage for four different storage states; and

Figure 3 is a mixed circuit/block diagram of a generating circuit according to the invention.

[0013] As previously mentioned, this invention is especially useful for non-volatile storage devices which comprise cells formed of MOS transistors with a floating gate terminal, such as that illustrated by the schematics of Figure 1.

[0014] This comprises a plurality MTX of memory cells MC organized into a matrix. The source terminals of the cells MC are connected to a ground GND; the gate terminals are connected together as rows and to word lines WL; and the drain terminals are connected together as columns and to bit lines BL. The word lines WL are connected to a row decoder RDEC which receives a row address RADR on its input; and the bit lines BL are connected to a column decoder CDEC which receives a column address CADR on its input.

[0015] Since the device of Figure 1 is a FLASH memory, the cells MC have no selection transistors, and the decoder RDEC is input a read voltage RV, write voltage WV, and erase voltage EV, to selectively supply them, through a switching circuit SW, to the lines WL consistently with the operation to be executed.

[0016] Associated with and connected to the decoder CDEC is a read amplifier SAMP which is effective to produce, on an output DOUT, 2 bits corresponding to

the binary coding of the storage state in the selected memory cell: this is, therefore, a multi-level storage device, specifically a four-level storage device.

[0017] A read amplifier suited for non-volatile memories of the multi-level type, and adapted for use in the device of Figure 1, is illustrated in Patent Application EP 735 542, for example.

[0018] It will be recalled that the threshold voltage Vth of floating gate MOS transistors can be controlled by injecting or extracting charges into/from the floating gate.

[0019] In a four-level device, the distribution DIS of the cell threshold voltage for the four different storage states ("11", "10", "01", "00") may be that shown in Figure 2, for example. The distributions are of bell-like shape, and their midpoint values may be, for example: 2.0 volts (virgin cell), 3.1 volts, 4.5 volts, and 6.2 volts. In general, their width increases with the midpoint value. For reliable reading at a low error rate, suitably spaced narrow distributions are needed.

[0020] With the distributions spaced apart as shown in Figure 2, and if the supply voltage VCC can be varied, according to specification, from 4.5 volts to 5.5 volts, a proper and safe discrimination between the states "01" and "00" requires that a sufficiently regulated reading gate voltage RV1 be generated and used, e.g. 5.35 volts (mean value of 4.5 and 6.2). This value is higher than the specified minimum supply voltage. With more widely spaced distributions, the value of the read voltage RV1 must be much higher than the value of the supply voltage VCC.

[0021] A similar problem to that of multi-level memories may be encountered in two-level devices if the supply voltage VCC is low, i.e. equal to or just slightly higher than the threshold voltage of the virgin cell.

[0022] It will be recalled that, with FLASH devices, it is generally necessary to effect the reading of a cell both during the reading operation proper, and during the write and/or erase operations as the result of the operation is being verified.

[0023] The invention will be illustrated hereinafter mainly with reference to Figure 3.

[0024] The method for generating a regulated voltage, according to this invention, provides for the use, as a reference element for the regulating operation, of a non-volatile memory reference cell REFC of the floating gate type.

[0025] In order for the regulated voltage value to track well the changes in performance of the memory cells, it is preferred that the cell REFC be substantially identical with the cells MC of the plurality MTX being read.

[0026] If the threshold voltage of the cell REFC has an unsuitable value, it will be necessary to program the cell REFC at a predetermined threshold voltage value before the start of the regulating operation. With the circuit of Figure 3 and the distributions of Figure 2, the cell REFC should be programmed at a threshold voltage value RV1 corresponding to a value intermediate the distributions "01" and "00", e.g. 5.35 volts. Such programming can be effected at the EWS stage with high accuracy ($\pm 1\mu A$) by accessing the cell directly.

[0027] The generation circuit of this invention comprises, therefore:

a) a generator circuit adapted to output an unregulated voltage VCHP;

b) a comparator circuit coupled to the output of the generator circuit and adapted to output an electric error signal ID tied to the difference between the voltage VCHP and an internal reference voltage; and

c) a regulator circuit coupled to the output of the comparator circuit and operative to regulate the voltage VCHP based on the value of the signal ID.

[0028] The comparator circuit includes a reference element consisting of a non-volatile memory cell REFC of the floating gate type whose threshold voltage corresponds to said internal reference voltage.

[0029] The comparator circuit can be implemented in any of several ways: for example, using a reference generator coupled to a voltage comparator.

[0030] In a very simple and effective embodiment, this circuit is only formed essentially of the cell REFC. In this case, the output of the generator circuit is coupled to the gate terminal of the cell REFC, and the regulator circuit is input, as the error signal ID, the current which is flowing through the cell, and will regulate the voltage VCHP accordingly.

[0031] There are several possible ways of implementing the regulation of a voltage. One embodiment, borrowed from linear regulators, consists of connecting the main conduction path of a transistor in series with the unregulated voltage generator, and of driving the gate terminal of the transistor such that the voltage drop across its main conduction path will compensate for the variations in the unregulated voltage.

[0032] By contrast, the method of this invention provides for the regulation to be effected by prompting, according to necessity, a current sinking from the output of the unregulated voltage generator circuit. In fact, if this generator has a sufficiently high output resistance, as would be the case where the circuit of this invention is used to drive very small loads such as the gate terminals of MOS transistors, a small current sinking brings about a fairly large voltage drop.

[0033] This can be easily implemented using a regulating transistor TR, included in the regulator circuit, with its main conduction path coupled between the output of the generator circuit and a reference of potential, e.g. the ground GND.

[0034] A typical way of implementing the generator circuit in the instance of non-volatile memories, consists of connecting an oscillator circuit OSC, adapted to gener-

ate an oscillating signal on its output, in cascade with a charge pump circuit CHP. In this case, the output resistance is bound to be fairly high.

[0035] It is advantageous to arrange for the regulation to produce, additionally to the current sinking, a discontinuance in the generation of the unregulated voltage VCHP, if a large current flows through the reference cell REFC, that is, if the unregulated voltage VCHP is high.

[0036] Where the generator circuit consists of an oscillator circuit OSC and a charge pump circuit CHP, this can be readily and effectively obtained by arranging for the charge pump circuit to be inhibited from receiving the oscillating signal on its input. For the purpose, the oscillator circuit OSCC may be provided with an activation control input coupled to an output of the regulator circuit.

[0037] When incorporated into a storage device comprising a plurality MTX of non-volatile memory cells MC of the floating gate type, the generation circuit of this invention can be utilized for powering the gate terminals of the cells MC, especially during reading operations. It will then be advantageous if the cell REFC is of the same type as the cells MC, preferably identical therewith.

[0038] For the regulated voltage value to track well the changes in the memory cell performance, the regulator circuit may include circuitry coupled to the cell REFC to mimic the operation of the circuitry coupled to the cells MC, that is the decoder CDEC and amplifier SAMP in Figure 1.

[0039] In the embodiment shown in Figure 3, the generation circuit includes an oscillator circuit OSC having an activation control input and an output for delivering an oscillating signal. Upon the control input being delivered a signal at a predetermined high logic level, the operation of the circuit OSC is de-activated.

[0040] The output of the circuit OSC is connected to an input of a charge pump circuit CHP which has an output for supplying an unregulated voltage VCHP.

[0041] The output of the circuit CHP is connected to the gate terminal of a floating gate NMOS transistor which functions as a non-volatile memory reference cell REFC; its source terminal is connected to the ground GND.

[0042] This cell can be factory programmed at the EWS (Electrical Wafer Sort) stage with great accuracy, e.g. with a current error on the order of 1μA.

[0043] The drain terminal of the cell REFC is connected to the input of the regulator circuit, specifically to the source terminal of a transistor MS of the N-MOS type whose gate terminal is connected to the power supply VCC. This transistor MS and its connections forms a circuit block CSEL intended to mimic, for the cell REFC, the effect of the decoder CDEC on the cells MC of the matrix MTX. When the cell REFC is conductive, the transistor MS is conductive and the voltage drop across the drain and source terminals is small.

[0044] The drain terminal of the transistor MS is connected directly to the source terminal of a transistor MB of the N-MOS type, and through an inverter INV, to the gate terminal thereof. The combined transistor MB and inverter INV form a circuit block CBIAS intended to bias the drain terminal of the cell REFC to about 1 volt and for emulating the biasing of the cells MC of the matrix MTX effected within the amplifier SAMP. For so doing, the inverter INV should have an input threshold of about 1 volt, and drive the transistor MB such that the transistor MB will let through the current of the cell REFC and de-couple it voltage-wise from the circuitry downstream. Its output logic levels may be, as an example, 0.0 volts and 2.5 volts for a supply voltage of 5.0 volts.

[0045] The drain terminal of the transistor MB is connected to the source terminal of a transistor MC of the N-MOS type having its gate and drain terminals connected together and to the power supply VCC. This transistor MC with its connections forms a circuit block IVC intended for emulating the current/voltage conversion stage of the amplifier SAMP. Alternatively, the block IVC could be formed of a transistor MC of the P-MOS type having its gate terminal connected to the ground GND. In this way, the action of the control circuit would be more effective, but at the expense of an inferior control precision because the potential at the drain terminal of the transistor MC would then be free to drop far below the supply potential VCC.

[0046] The source terminal of the transistor MC is connected to the input of an inverting-effect drive circuit DRV having a high input impedance. It could be either implemented by an inverter with a suitable input threshold and suitable output logic levels, or by an amplifier having a suitable transfer characteristic. The choice will be dictated by the type of regulation sought: either substantially linear or substantially digital.

[0047] The output of the circuit DRV is connected to the activation control input of the oscillator circuit OSC, and to the gate terminal of a transistor TR of the N-MOS type which has its source terminal connected to the ground GND and its drain terminal connected to the output of the charge pump circuit CHP.

[0048] When the voltage VCHP rises above the threshold voltage of the cell REFC, the latter will conduct a current ID which causes the potential at the input of the circuit DRV to decrease. The voltage at the output of the circuit DRV rises, sets the transistor TR to conduction, and may de-activate the circuit OSC, depending on its value and design options. Therefore, the voltage VCHP will be pulled down.

[0049] The regulation thus obtained is strictly dependent on design options and the circuit dimensioning. In addition, it should be noted that, at the output of the charge pump circuit CHP, there is an oscillating signal with a period on the order of 1μs, and that the duration of a reading operation is on the order of 10ns.

[0050] In the instance of storage devices, what is of interest is not regulation as such, but rather the capability to provide a reliable reading with a low error rate; for

example, ±40mV may be ample.

Claims

1. A method of generating a regulated voltage, in particular for gate terminals of a plurality (MTX) of non-volatile memory cells (MC) of the floating gate type, characterized in that, as reference element for the regulating operation, a non-volatile memory reference cell (REFC) of the floating gate type is used which is preferably substantially identical with the cells (MC) of said plurality (MTX).

2. A method according to Claim 1, wherein the reference cell (REFC) is programmed to a predetermined threshold value before the start of the regulating operation.

3. A method according to either Claim 1 or 2, comprising the steps of:

   a) causing a generator circuit (OSC,CHP) to generate an unregulated voltage (VCHP) on an output thereof;

   b) supplying said unregulated voltage (VCHP) to the gate terminal of the reference cell (REFC); and

   c) regulating said unregulated voltage (VCHP) by means of the current (ID) flowing through the reference cell (REFC).

4. A method according to Claim 3, wherein the regulating step c) consists of producing a current sinking from the output of said generator circuit (OSC,CHP).

5. A method according to Claim 4, wherein, if the current flowing through the reference cell (REFC) is large, the regulating step c) additionally consists of discontinuing the generation of said unregulated voltage (VCHP).

6. A method according to either Claim 4 or 5, wherein the generating step a) consists of causing an oscillator circuit (OSC) to generate an oscillating signal which is delivered to a charge pump circuit (CHP).

7. A circuit for generating a regulated voltage, in particular for gate terminals of non-volatile memory cells of the floating gate type, comprising:

   a) a generator circuit (OSC,CHP) adapted to generate an unregulated voltage (VCHP) on its output;

   b) a comparator circuit (REFC) coupled to the output of the generator circuit (OSC,CHP) and adapted to output an electric error signal (ID) tied to the difference between the unregulated voltage (VCHP) and an internal reference voltage; and

   c) a regulator circuit (CSEL,CBIAS,IVC,DRV,TR) coupled to the output of the comparator circuit (REFC) and operative to regulate the unregulated voltage (VCHP) based on the value of said electric error signal (ID);
   characterized in that said comparator circuit comprises a reference element consisting of a non-volatile memory cell (REFC) of the floating gate type whose threshold voltage corresponds to said internal reference voltage.

8. A circuit according to Claim 7, wherein the output of the generator circuit (OSC,CHP) is coupled to the gate terminal of the cell (REFC), and wherein the regulator circuit (CSEL,CBIAS,IVC,DRV,TR) receives on its input the current flowing through the cell (REFC).

9. A circuit according to either Claim 7 or 8, wherein the regulator circuit (CSEL,CBIAS,IVC,DRV,TR) comprises a regulating transistor having its main conduction path coupled between the output of the generator circuit (OSC,CHP) and a reference (GND) of potential.

10. A circuit according to Claim 9, wherein said generator circuit (OSC,CHP) comprises an oscillator circuit (OSC) and a charge pump circuit (CHP) coupled in cascade.

11. A circuit according to Claim 9, wherein said generator circuit (OSC,CHP) comprises an oscillator circuit (OSC) provided with an activation control input and a charge pump circuit (CHP) coupled in cascade, and wherein said regulator circuit has an output (DRV) coupled to the activation control input of the oscillator circuit (OSC).

12. A storage device of the type which comprises a plurality (MTX) of non-volatile memory cells (MC) of the floating gate type, characterized in that it comprises a cell (MC) gate voltage (RV) generation circuit according to one of the preceding claims, and that the cell (REFC) of the generation circuit is of the same type as, preferably substantially identical with, the cells (MC) of the plurality (MTX).

13. A device according to Claim 12 and of the type adapted to store more than one element of binary information per cell.

14. A device according to Claim 12 and of the type adapted to operate on a low supply voltage.

15. A device according to one of the preceding claims, comprising a switching circuit (SW,RDEC) adapted to only couple said generation circuit to the gate terminals of the cells (MC) of the plurality (MTX) only during reading operations of the device.

16. A device according to one of the preceding claims, wherein the regulator circuit (CSEL, CBIAS,IVC,DRV,TR) comprises circuitry (CSEL,CBIAS,IVC) coupled to the cell (REFC) which mimics the operation of the circuitry (CDEC,SAMP) coupled to the cells (MC) of the plurality (MTX).

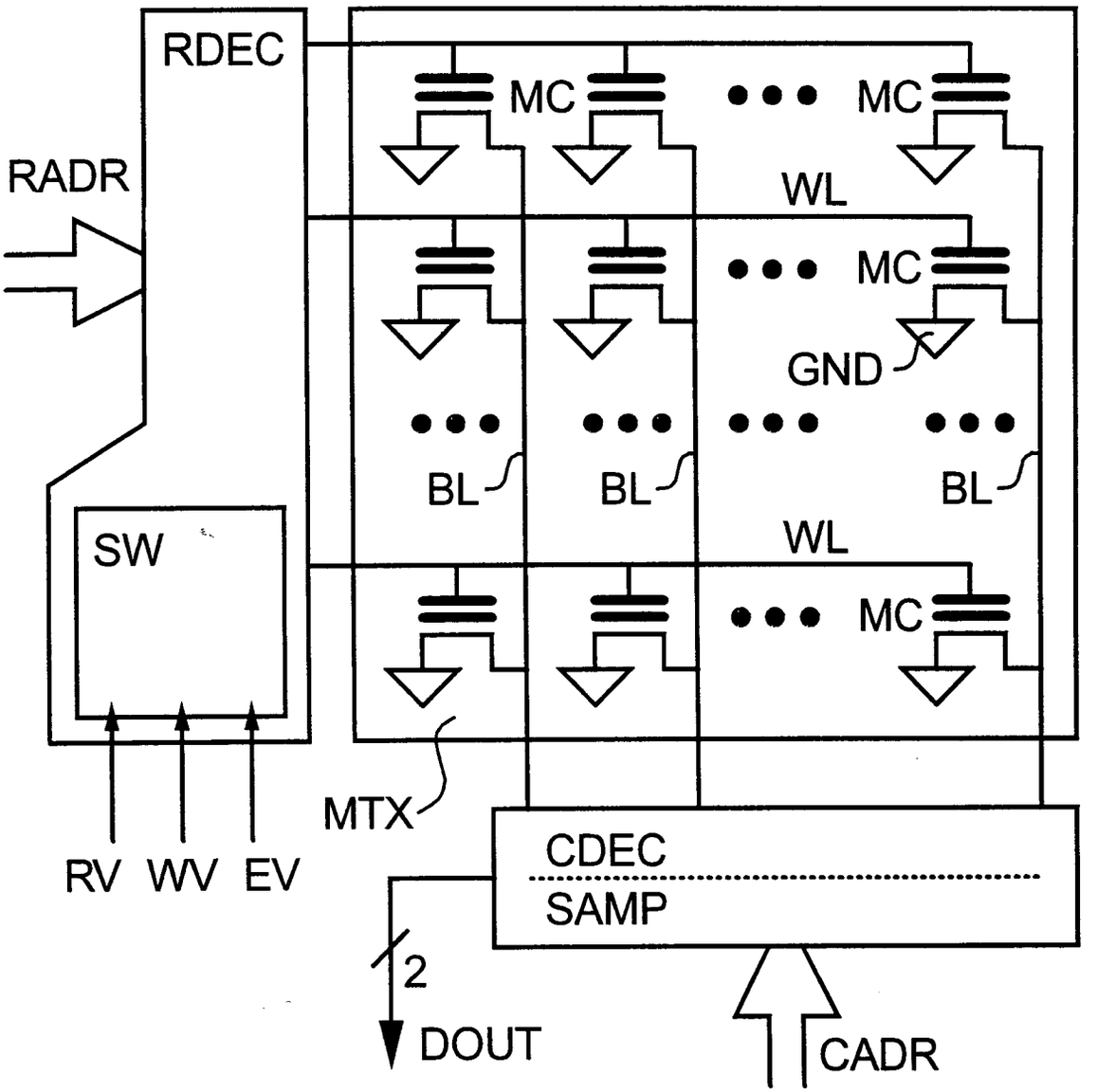
RDEC
RADR
MC
MC
WL
MC
GND
BL
BL
BL
SW
WL
MC
MTX
RV
WV
EV
CDEC
SAMP
2
DOUT
CADR

Fig.1

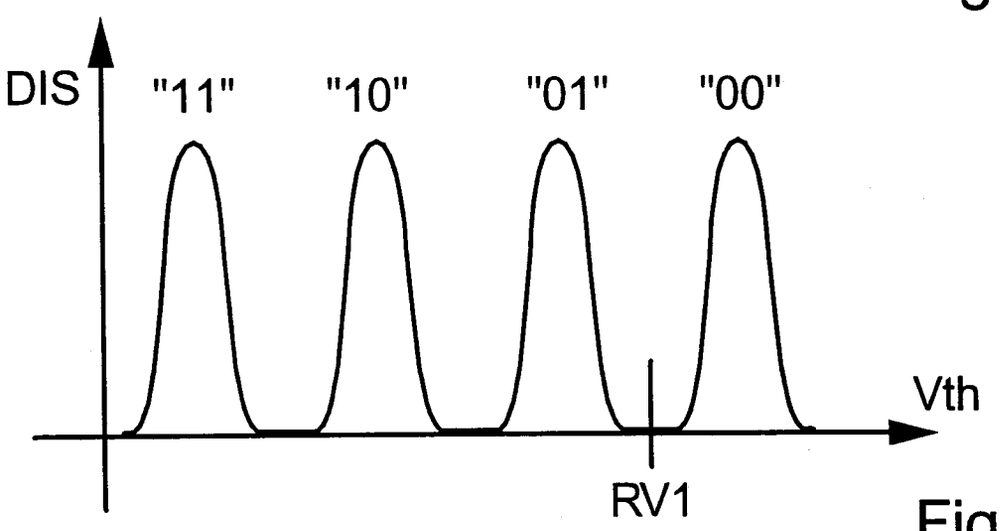
DIS
"11"
"10"
"01"
"00"
Vth
RV1

Fig.2

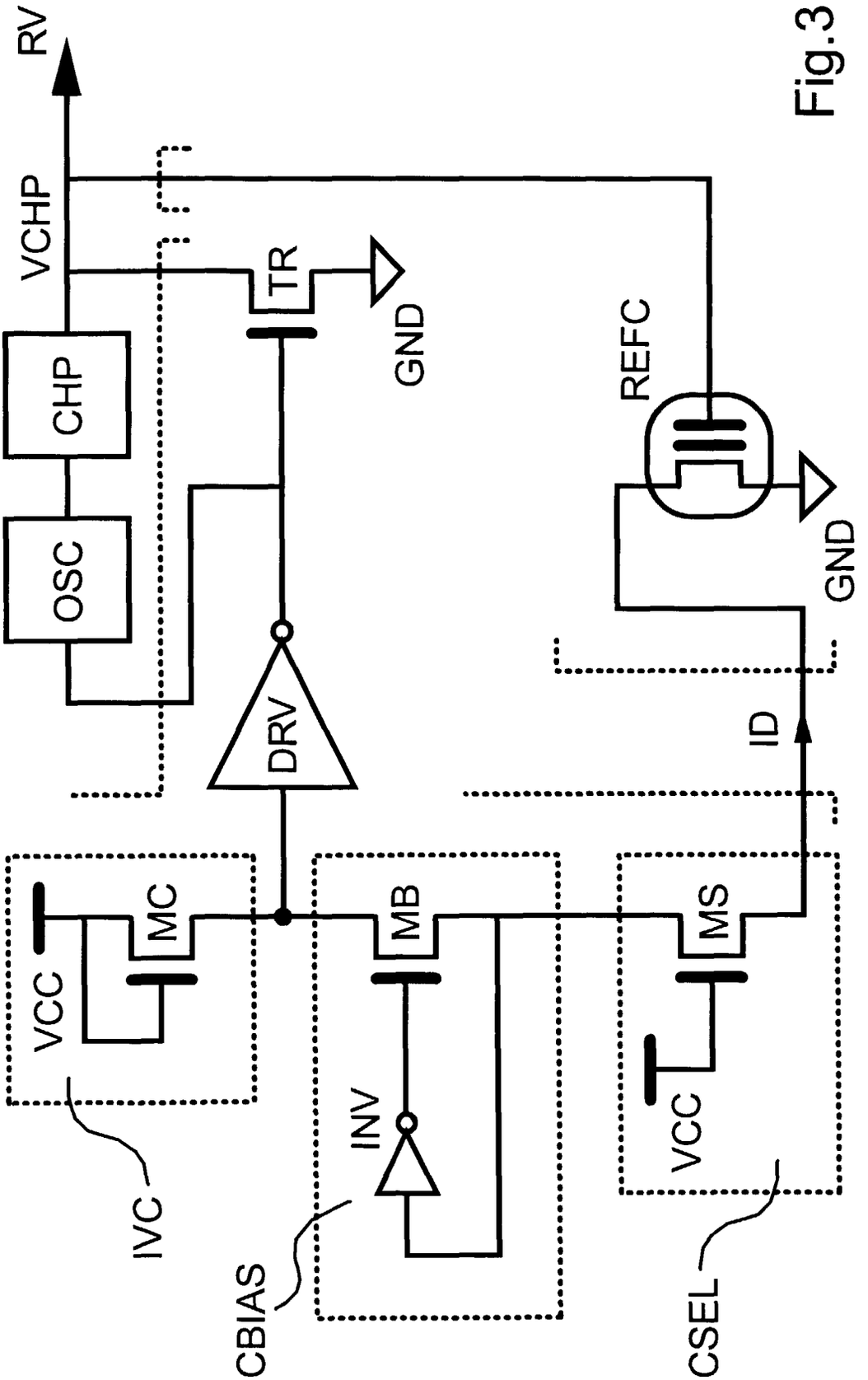
RV
VCHP
CHP
OSC
TR
GND
REFC
GND
DRV
ID
VCC
MC
MB
MS
INV
VCC
IVC
CBIAS
CSEL

Fig.3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0435

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 276 646 A (KIM ET AL)	1-4,6-8, 10-12	G11C11/00 G11C16/06
A	* the whole document *	5,9,14	G11C11/56
X	US 4 954 990 A (VIDER)	1-3,7,8, 12	
A	* the whole document *	5,9,16	
X	EP 0 786 777 A (SGS THOMSON)	1,7,8, 12,14	
A	* the whole document *	15,16	
X	US 5 559 717 A (TEDROW ET AL) * column 4, line 12 - column 5, line 13; figures 2,3 *	1,2,15	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 February 1998	Degraeve, L

CATEGORY OF CITED DOCUMENTS

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