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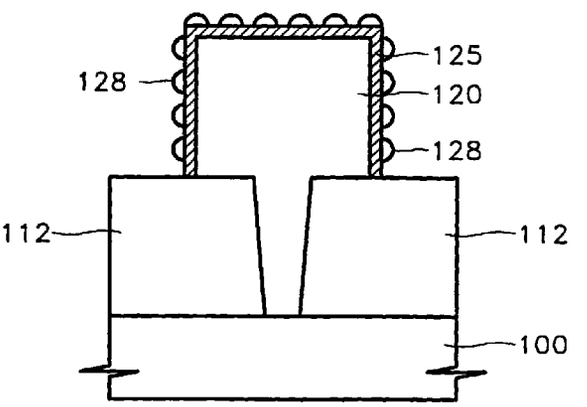
(54) A method for manufacturing a capacitor lower electrode of a semiconductor memory device

(57) In a method for manufacturing a capacitor lower electrode of a semiconductor memory device, an insulation film pattern (112) is formed on a semiconductor substrate (100) with a contact hole (h_1) to expose a predetermined area of the semiconductor substrate. An impurity-doped amorphous silicon film is deposited on the overall surface of the resultant. A lower electrode pattern (120) is formed by patterning the amorphous silicon film. Contaminants and a surface oxide film are removed from the surface of the resultant by cleaning the resultant. An amorphous silicon thin layer (125) is deposited on the surface of the lower electrode pattern (120) by loading the cleaned resultant into the process chamber maintained in vacuum, and supplying a predetermined gas into the process chamber for a predetermined time. A plurality of silicon crystal nuclei (128) are formed and grown on the amorphous silicon thin layer (125) to form a lower electrode (130) having a rugged surface.

FIG. 5



EP 0 902 462 A1

Description

[0001] The present invention relates to a semiconductor device manufacturing method, and more particularly, to a method for manufacturing a capacitor lower electrode of a semiconductor memory device which increases capacitor capacitance by increasing the surface area of the electrode in a dynamic random access memory (DRAM).

[0002] In DRAMs, with a decrease in the surface area of a unit memory cell, cell capacitance is reduced, resulting in a lowered reading performance of the memory cell and an increased soft error rate. Therefore, the cell capacitance should be kept at an acceptable level to realize high integration of semiconductor memory devices.

[0003] The cell capacitance of a semiconductor memory device is an important factor in determining the memory capacity thereof. Along with the increase in the integration level of semiconductor memory devices, many methods have been suggested for increasing capacitance in a given cell area. The capacitor capacitance C is given by

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}$$

where ε_0 is the dielectric constant of free space, ε_r is the relative dielectric constant of a dielectric film, A is the effective area of an electrode, and d is the thickness of the dielectric film. As noted from the above equation, the capacitance can be increased by varying three parameters, i.e., the dielectric constant of a dielectric film, the effective area of a capacitor, or the thickness of the dielectric film.

[0004] As typical methods for increasing the capacitor capacitance by increasing effective area of an electrode, a hemispherical grain (HSG) silicon film is formed as a rugged surface on the surface of a lower electrode, or a three-dimensional capacitor structure is used, including a stack, a trench, and a cylindrical structure.

[0005] Tatsumi discloses in U.S. Patent No. 5,385,863 that , in order to increase the effective area of the capacitor electrode, a capacitance electrode made of a polysilicon film is formed, the polysilicon film being formed by depositing an amorphous silicon film on an insulating film covering a semiconductor substrate, generating a plurality of crystal nuclei at a plurality of the amorphous silicon film, respectively, and growing each of the plurality of crystal nuclei into a mushroom or hemisphere shaped crystal grain to thereby convert the amorphous silicon film into the polysilicon film. However, it is difficult to maintain the face of the amorphous silicon film deposited on the insulating film clean. Even crystallization of a extremely small area in the amorphous silicon film or contamination of the surface of the extremely small area by foreign materials suppresses the surface migration of the silicon atoms in the amorphous silicon film and thus prevents crystal nucleation and growth. As a result, a HSG film of an irregular configuration is produced.

[0006] FIGS. 1A and 1B are scanning electron microscope (SEM) photos showing the result of forming HSGs on a partially crystallized amorphous silicon film on a semiconductor substrate. As noted from the figures, HSGs are normally formed on amorphous silicon, while no growth of nuclei is observed in a crystallized portion due to the absence of activation energy of silicon.

[0007] Similarly, when the amorphous silicon surface is contaminated by foreign materials and thus the amorphous silicon atoms are combined with foreign atoms, it is difficult for the silicon to make a surface migration, the amorphous silicon surface is further contaminated, and crystal nucleation and growth is terminated if the foreign materials are accumulated to a predetermined thickness.

[0008] According to the present invention, a method for manufacturing a capacitor lower electrode of a semiconductor memory device, the lower electrode formed by thin film deposition equipment provided with a process chamber including a susceptor for mounting a wafer thereon, comprises the steps of:

(a) forming an insulation film pattern on a semiconductor substrate, said insulation film having a contact hole to expose a predetermined area of said semiconductor substrate;
(b) depositing an impurity-doped amorphous silicon film on the overall surface of said resultant;
(c) forming a lower electrode pattern by patterning said amorphous silicon film;
(d) removing contaminants and a surface oxide film from the surface of said resultant by cleaning said resultant;
(e) depositing an amorphous silicon thin layer on the surface of said lower electrode pattern by loading said cleaned resultant into said process chamber maintained in a high vacuum, and supplying a predetermined gas into said process chamber for a predetermined time; and
(f) forming and growing a plurality of silicon crystal nuclei on said amorphous silicon thin layer to form a lower electrode having a rugged surface.

[0009] Preferably, the supply of the predetermined gas is performed while heating the semiconductor substrate, and the step of heating the semiconductor substrate comprises the steps of: (a) maintaining the temperature of the susceptor at 700-1000°C for 5-40 seconds; and (b) maintaining the temperature of the susceptor at 500-800°C in the process chamber, immediately after the step (a).

[0010] Preferably, the predetermined gas is one of SiH_4, Si_2H_6, SiH_2Cl_2, and a mixture thereof. More pref-

erably, the predetermined gas further comprises an inert gas.

[0011] It is preferable that the amorphous silicon thin layer is selectively deposited only on the surface of the lower electrode pattern in the step of (e).

[0012] It is preferable that the step of (f) is performed without vacuum breakdown subsequent to the step of (e), and the step of (f) is performed at a pressure of 10^{-7}torr or below.

[0013] It is preferable that the step of (f) comprises the sub steps of: continuously supplying the predetermined gas during the silicon crystal nuclei formation; and blocking the supply of the predetermined gas during the silicon crystal nuclei growth. The supply of the predetermined gas is simultaneously controlled in the step of supplying a predetermined gas.

[0014] An example of the present invention will now be described in detail with reference to the accompanying drawings, in which:

FIGS. 1A and 1B are SEM photos showing the result of forming HSGs on a partially crystallized amorphous silicon film on a semiconductor substrate;

FIG. 2 illustrates surface tensions of a crystal nucleus formed on the surface of a lower electrode;

FIGS. 3 through 6 are sectional views sequentially showing the steps in a method for manufacturing a capacitor of a semiconductor memory device according to a preferred embodiment of the present invention;

FIG. 7 illustrates variations of a process temperature in a process chamber in fabricating a capacitor according to the present invention;

FIGS. 8A through 8D are SEM photos showing rugged surface structures obtained by varying the temperature stabilizing time and the process gas supply time;

FIG. 9 is a graph showing the result from an estimation of capacitance and Cmin/Cmax characteristics of samples under each test condition;

FIG. 10 is a graph showing the result from an estimation of capacitance and Cmin/Cmax characteristics with respect to the grain height with a long enough temperature stabilizing time given;

FIG. 11 is a graph showing the result from an estimation of capacitance characteristics of a capacitor manufactured according to the method of the present invention; and

FIG. 12 is a graph showing the result from an estimation of Cmin/Cmax characteristics of the capacitor manufactured according to the method of the present invention.

[0015] Generally, the formation of HSG silicon film to increase the effective area of the electrode relies on the mechanism of surface migration of silicon atoms. According to such a mechanism, crystal nuclei are formed on the surface of an amorphous silicon film using a silicon source gas, e.g., silane (SiH_4) or disilane (Si_2H_6) gas, and annealed so that silicon atoms of the amorphous silicon film migrate to the crystal nuclei and form a HSG silicon film having hemispherical grains of a predetermined size on the surface of the amorphous silicon film. Here, to allow the crystal nuclei to continuously grow for a specified period of time, the migration time of the silicon atoms to the crystal nuclei should exceed the crystallization time of a bulk area of the amorphous silicon film being an underlayer. Therefore, the migration time and the crystallization time should be stably controlled to ensure the increase of the effective area of the electrode by the above mechanism.

[0016] The mechanism of forming the HSG silicon film as a rugged surface on the surface of the amorphous silicon film is affected by two factors during processing: the characteristics of the amorphous silicon film itself and contamination caused by foreign materials adsorbed on the surface of the underlayer before or after crystal nucleation.

[0017] Specifically, the amorphous silicon film used as an underlayer to form the rugged surface should be kept amorphous and completely free of crystal grains. The possible existence of the crystal grains in the underlayer prevents silicon atoms of the crystal grains from migrating to the crystal nuclei during formation of the rugged surface. On the other hand, foreign material-induced contamination may occur in cleaning the surface of the underlayer or exposing a resultant including the crystal nuclei to the atmosphere. Thus, it is essential to keep the surface of the underlayer clean before silicon crystal nucleation.

[0018] FIG. 2 illustrates a typical crystal nucleus 12 formed of crystal silicon on the surface of a lower amorphous silicon electrode pattern 10 in a gaseous atmosphere.

[0019] Generally, the mechanism in which crystal nuclei formed on an amorphous silicon surface grows with phase transition as activation energy can be expressed as the sum of phase transition-related Gibbs free energy and interface energy, i.e., surface energy generated during crystal nucleation and growth. Referring to FIG. 2, such a relationship is given by

$$G = (4/3)\pi r^2 \Delta G_{tr} f(\theta) + 4\pi r^2 \gamma f(\theta)$$

where ΔG is the total Gibbs free energy, r is the radius of a crystal nucleus, and ΔG_{tr} is the Gibbs free energy of phase transition per unit volume ($\Delta G_{tr} = \Delta G_{crystal} - \Delta G_{amorphous}$). γ is the vector sum of γ_{mg}, γ_{nm}, and γ_{ng}, which are the surface tensions between gas and amorphous silicon, between crystal silicon and amorphous silicon, and between gas and crystal silicon, respectively. $f(\theta)$ is a configuration factor.

[0020] As described above, the silicon atoms on the surface of the amorphous silicon migrate to the crystal silicon, that is, the crystal nucleus 12, with activation

energy given by the above equation so that crystal nuclei are grown. The above equation represents the minimum activation energy needed for the growth of the silicon atoms in the amorphous silicon film into crystal silicon through the phase-transition to the crystal silicon nucleus. In practice, the silicon atoms of the amorphous silicon film should migrate to the crystal silicon for the growth of the crystal nucleus. To allow the silicon atoms in the amorphous silicon film to migrate to the crystal silicon, the amorphous silicon should be kept amorphous condition and have a free surface in which silicon atoms are not combined with other atoms.

Embodiment

[0021] In the present invention, a semiconductor substrate having an amorphous silicon layer formed thereon is loaded in a process chamber and an amorphous silicon thin layer of high purity and few defects is formed on the amorphous silicon layer in an ultrahigh vacuum state. Subsequently, crystal nucleation and growth are performed on the amorphous silicon thin layer, thereby forming an intended rugged surface.

[0022] FIGS. 3 through 6 are sectional views sequentially showing the steps in a method for manufacturing a capacitor of a semiconductor memory device according to a preferred embodiment of the present invention.

[0023] Referring to FIG. 3, an insulation layer is formed on a semiconductor substrate 100 including an underlying structure such as a transistor to insulate the underlying structure. Then, a photoresist pattern (not shown) is formed on the insulation layer by photolithography. The insulation layer is etched using the photoresist pattern as an etching mask, thereby forming an insulation pattern 112 and a contact hole h_1 for exposing a portion of the semiconductor substrate 100.

[0024] After the photoresist pattern is removed, an impurity-doped amorphous silicon film is deposited on the overall surface of the resultant having the contact hole h_1. A lower electrode pattern 120 of amorphous silicon is formed by patterning the deposited amorphous silicon film.

[0025] Thereafter, contaminants and a surface oxide film, i.e., a natural oxide film are removed from the surface of the lower electrode pattern 120 by wet-cleaning the resultant. Subsequently, to form a rugged surface, the resultant is loaded in the process chamber (not shown) kept in a ultrahigh vacuum state, preferably, below or at a pressure of 10^{-7}torr.

[0026] FIG. 7 is a graph showing a temperature variation in each stage during processing in the process chamber to form the rugged surface on the lower electrode pattern 120 of the semiconductor substrate 100. In FIG. 7, reference character (a) indicates a variation in a setting temperature of a heater installed in the chamber to control the temperature of a susceptor in the process chamber. Reference character (b) indicates a variations in semiconductor substrate temperature actually observed. Reference character (c) indicates a variation in susceptor temperature.

[0027] Referring to FIG. 7, in stage 1, the susceptor is heated to 700-1000°C, preferably about 850°C, by increasing the heater temperature to approximately 1000°C for about 5-40 seconds, preferably 20 seconds, so as to rapidly increase the temperature of the semiconductor substrate 100 having the lower electrode pattern 120 formed thereon loaded in the process chamber. Then, the susceptor temperature is reduced to a predetermined temperature, for example, 500-800°C, preferably 720°C, by decreasing the heater temperature to about 765°C, and then the heater temperature is maintained at about 765°C. The semiconductor substrate 100 is kept in the process chamber for a predetermined time until the surface of the lower electrode pattern 120 is set at a temperature appropriate for depositing an amorphous silicon thin layer thereon in a subsequent process. Such a standby time, that is, time required to reach a temperature suitable for the deposition of the amorphous silicon thin layer, is referred to as a temperature stabilizing time.

[0028] In stage 2 of FIG. 7, when the substrate temperature reaches a predetermined temperature lower than a temperature appropriate for the deposition of the amorphous silicon thin layer, that is, a rugged surface forming temperature, preferably 550°C or below, the process chamber is supplied with a process gas needed to form crystal nuclei for rugged surface formation, for example, one of SiH_4, Si_2H_6, and SiH_2Cl_2, so as to deposit the amorphous silicon thin layer on the surface of the lower electrode pattern 120. Here, an inert gas such as nitrogen (N_2) or argon (Ar) can be simultaneously supplied into the process chamber.

[0029] FIG. 4 illustrates the amorphous silicon thin layer 125 deposited on the surface of the lower electrode pattern 120.

[0030] The amorphous silicon thin layer 125 is deposited to a thickness of several tens of angstroms, preferably, only on the surface of the lower electrode pattern 120 by controlling the process gas supply time. Here, since the process chamber is kept at near vacuum conditions of 10^{-3}torr or below even during the deposition of the amorphous silicon thin layer 125, the adsorption of impurities on the surface of the lower electrode pattern 120 is prevented, thus suppressing contamination of the surface of the semiconductor substrate.

[0031] While the amorphous silicon thin layer 125 is being deposited in stage 2 of FIG. 7, the substrate temperature is heated to a temperature to allow crystal nuclei formation, for example, 570°C or above. Thus, a plurality of crystal nuclei can be formed on the surface of the amorphous silicon thin layer 125.

[0032] In stage 3 of FIG. 7, as the semiconductor substrate 100 is gradually heated to a crystallization temperature or above, a plurality of crystal nuclei are successively formed on the amorphous silicon thin layer 125 (see FIG. 4). That is, the crystal nuclei are formed

on the amorphous silicon thin layer 125 without vacuum breakdown, subsequent to the deposition of the amorphous silicon thin layer 125 in high vacuum. During the silicon crystal nucleation, the aforementioned process is continuously provided. When necessary, the flow of gas may be simultaneously controlled. Thus, adsorption and generation of impurities at their interface can be prevented by sequential formation of the amorphous silicon thin layer 125 and the silicon crystal nuclei without vacuum breakdown. Therefore, crystal nuclei of a uniform configuration can be formed in the method of the present invention.

[0033] In stage 4 of FIG. 7, supply of the process gas is terminated, and the pressure of the process chamber is maintained again in ultrahigh vacuum, for example, below or at 10^{-7}Torr, and a process for crystal nuclei growth is performed. That is, as the temperature of the semiconductor substrate 100 reaches a steady-state temperature in the process chamber, crystal nuclei 128 are in effect subjected to heat treatment at the silicon crystallization temperature or above. In practice, it takes approximately 150 seconds for the semiconductor substrate 100 to reach a steady state, i.e., about 600°C in the process chamber. At this time period, silicon atoms in the amorphous silicon thin layer 125 migrate to the crystal nuclei 128 so that crystal nuclei 128 can be grown. If the crystal nuclei continue to grow, mutual cohesion takes place between adjacent crystal grains, resulting in reduction of the effective area of a capacitor. Therefore, the growth of the grains should be controlled by adjusting the heat treatment temperature and time to allow a rugged surface having grains of an appropriate size to be formed.

[0034] FIG. 6 is a sectional view of a completed lower electrode 130 having a rugged surface. In FIG. 6, reference numeral 120A indicates the outline of the lower electrode pattern 120 before completing the rugged surface on the lower electrode 130.

[0035] After the lower electrode 130 having the rugged surface is completed in stage 4 of FIG. 7, the semiconductor substrate 100 is unloaded from the process chamber and cooled to room temperature.

[0036] Then, a capacitor insulation film is formed on the above resultant and a conductive material is deposited on the capacitor insulation film to form an upper electrode.

[0037] In the present invention, a series of processes for forming the amorphous silicon thin layer on the surface of the lower electrode pattern, forming crystal nuclei and forming the rugged surface are successively performed in the process chamber without vacuum breakdown, thus enabling processing in a highly clean state. Accordingly, the drawbacks encountered in the prior art such as failure of growth of the crystal grains can be overcome and uniformity of crystal grain size and density can be increased. Furthermore, deposition of the amorphous layer between the lower electrode and the rugged surface decreases the ratio of the minimum value to the maximum value of a capacitance (hereinafter, referred to as Cmin/Cmax). This problem can be solved without an additional heat treatment for an ideal Cmin/Cmax, since the semiconductor substrate is subjected to heat treatment in effect in a subsequent process to the formation of a capacitor.

Estimation 1

[0038] The characteristics of a capacitor having a rugged surface on a lower electrode according to the method of the present invention are estimated as follows.

[0039] To estimate the effect of formation of an amorphous silicon thin layer on the subsequently formed rugged surface on a lower electrode pattern, a temperature stabilization time, that is, a standby time before supply of a process gas needed to form the amorphous silicon thin layer, was varied from between 30-180 seconds and a process gas supply time was varied from between 80-140 seconds, with the conditions of a heater temperature of 765°C, a crystal nuclei growth time of 180 seconds, and process gad Si_2H_6 flow rate of 18sccm kept as they are. Then, the shape of crystal grains forming the rugged surface on the lower electrode was observed.

[0040] FIGS. 8A through 8D are SEM photos showing the structures of a rugged surface obtained under variations in temperature stabilization time and process gas supply time in the above test. FIG. 8A is for a temperature stabilization time of 180 seconds and a process gas supply time of 80 seconds, FIG. 8B for 90 seconds and 100 seconds, FIG. 8C for 60 seconds and 120 seconds, and FIG. 8D for 30 seconds and 140 seconds, respectively.

[0041] As noted from the results of FIGS. 8A through 8D, when crystal nucleation and growth are performed at a silicon crystallization temperature with a long enough temperature stabilization time after a temperature increase (FIG. 8A), the crystal grains are large and very dense. On the other hand, as the temperature stabilization time after the temperature increase is reduced to 90, 60, and 30 seconds, respectively, the amorphous film is deposited before the silicon crystallization temperature is reached after supply of the process gas even though the process gas supply time is increased, leading to a reduction of the time for forming crystal grains. As a result, the structure obtained after the process is completed exhibits low density and small size of crystal grains. Therefore, it is noted that the temperature stabilization time changes the effective area of a lower electrode, thus directly affecting a capacitance value, in fabricating a capacitor.

Estimation 2

[0042] An insulation film and an upper electrode were formed on the sample formed under each condition of

Estimation 1, and then capacitor characteristics were estimated.

[0043] FIG. 9 is a graph showing the result from an estimation of capacitance and Cmin/Cmax characteristics of each sample. Cmin/Cmax is the ratio of the minimum value to the maximum value of capacitance measured by varying a capacitance measuring voltage from -1.5 to +1.5V. Cmin is the capacitance obtained by grounding an n-type impurity-doped lower electrode and applying -1.5V to an upper electrode, while Cmax is the capacitance obtained by grounding the n-type impurity-doped lower electrode and applying +1.5V to the upper electrode.

[0044] It is noted from the result of FIG. 9 that the capacitance increases with an increase of the temperature stabilizing time due to an increase in the size and density of crystal grains formed on the surface of the lower electrode, as shown in the SEM photos of FIGS. 8A to 8D. The Cmin/Cmax was also observed to be distributed in the range of 84-87%.

Estimation 3

[0045] Based on the estimation result of Estimation 2, a semiconductor substrate having an amorphous silicon lower electrode pattern formed thereon is loaded in a process chamber with a long enough temperature stabilization time. Then, characteristics of a capacitor provided with a lower electrode having a rugged surface were estimated according to the method of the present invention. Here, a temperature stabilizing time was 180 seconds, a process gas supply time, i.e., a grain forming time, was 80 seconds, a process gas flow rate was 18sccm, and grain size, that is, grain height was controlled by control of process temperature, in order to estimate capacitance and Cmin/Cmax characteristics according to grain size.

[0046] FIG. 10 is a graph showing capacitance and Cmin/Cmax characteristics as a result of the above estimation. In FIG. 10, grain height "0Å" indicates absence of crystal grains forming a rugged surface.

[0047] From FIG. 10, it can be seen that the effective area and thus capacitance of the capacitor increase with an increase of grain size. Cmin/Cmax decreases as grain size increases. As noted from the results, in the capacitor whose effective area is increased by using a rugged surface, capacitance increases and Cmin/Cmax decreases with an increase of grain size.

[0048] However, in the case of a capacitor having a rugged surface formed with a short temperature stabilization time according to the method of the present invention, the reduction of grain size increases the capacitance, not Cmin/Cmax, in contrast to the sample of FIG. 10. The reason is that when a silicon forming gas is supplied in high vacuum to form a rugged surface on an amorphous silicon lower electrode pattern doped with impurities, at a low substrate temperature, an amorphous silicon film not doped with impurities is formed before the formation of the rugged surface. Due to the amorphous silicon layer not doped with impurities formed between the lower electrode pattern and the rugged surface, serious depletion takes place in the lower electrode, thus reducing the Cmin/Cmax value.

[0049] Here, the problem of the Cmin/Cmax decrease caused by the amorphous silicon layer formed in high vacuum can be solved by a heat treatment after forming a capacitor.

[0050] As described above, partial or entire absence of the rugged surface can be prevented and a desired capacitance can be obtained by properly controlling the temperature stabilizing time, process gas supply time, and other process parameters.

Estimation 4

[0051] FIG. 11 illustrates the result of an estimation of capacitance characteristics of a capacitor manufactured according to the method of the present invention. In FIG. 11, a comparative sample, to which the method of the present invention is not applied, has no rugged surface. As noted from the result of FIG. 11, a capacitance of about 25fF/cell of a capacitor manufactured according to the method of the present invention was increased by 1.6 times or more compared with the capacitance of about 15fF/cell of a capacitor to which the method of the present invention is not applied. Further, a reproducible and stable capacitance distribution was obtained according to an application frequency.

Estimation 5

[0052] FIG. 12 illustrates the result of an estimation of Cmin/Cmax characteristics of the capacitor manufacture according to the method of the present invention. In FIG. 12, a comparative example, to which the method of the present invention is not applied, has no rugged surface formed therein. In a practical semiconductor device manufacturing process, a semiconductor substrate is thermally treated in effect without an additional heat treatment since subsequent thermal processes are followed thereafter. Thus, impurity diffusion into an amorphous silicon layer formed in high vacuum can be effected. Therefore, as noted from the result of FIG. 12, Cmin/Cmax characteristics are improved in the capacitor manufactured according to the present invention.

[0053] As described above, in the present invention, partial absence of crystal grains can be suppressed, and crystal size and density are increased compared with those of conventional HSGs. Accordingly, the effective area of a capacitor in a semiconductor memory device can be efficiently increased.

Claims

1. A method for manufacturing a capacitor lower electrode of a semiconductor memory device, the lower

electrode formed by thin film deposition equipment provided within an enclosed process chamber including a susceptor for mounting a wafer thereon, said method comprising the steps of:

(a) forming an insulation film pattern on a semiconductor substrate, said insulation film having a contact hole to expose a predetermined area of said semiconductor substrate;
(b) depositing an impurity-doped amorphous silicon film on the overall surface of said resultant;
(c) forming a lower electrode pattern by patterning said amorphous silicon film;
(d) removing contaminants and a surface oxide film from the surface of said resultant by cleaning said resultant;
(e) depositing an amorphous silicon thin layer on the surface of said lower electrode pattern by loading said cleaned resultant into said process chamber maintained in a high vacuum, and supplying a predetermined gas into said process chamber for a predetermined time; and
(f) forming and growing a plurality of silicon crystal nuclei on said amorphous silicon thin layer to form a lower electrode having a rugged surface.

2. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in claim 1, wherein said cleaning is performed by a wet cleaning process.

3. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in claim 1 or 2, wherein the supply of the predetermined gas is performed while heating the semiconductor substrate in said step (c).

4. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in claim 3, wherein said step of heating said semiconductor substrate comprises the steps of:

(a) maintaining the temperature of said susceptor at 700-1000°C for 5-40 seconds; and
(b) maintaining the temperature of said susceptor at 500-800°C in said process chamber, immediately after said step (a).

5. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein the supply of the predetermined gas is performed while maintaining the semiconductor substrate at a constant temperature in said step (e).

6. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein said predetermined gas is one of SiH_4, Si_2H_6, SiH_2Cl_2, and a mixture thereof.

7. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in claim 6, wherein said predetermined gas further comprises an inert gas.

8. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein said amorphous silicon thin layer is selectively deposited only on the surface of said lower electrode pattern in said step of (e).

9. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein said step of (f) is performed without vacuum breakdown subsequent to said step of (e).

10. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein said step of (f) is performed at a ultra high vacuum condition of a pressure of 10^{-7}torr or below.

11. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in any preceding claim, wherein said step of (f) comprises the sub steps of:

continuously supplying said predetermined gas during the silicon crystal nuclei formation; and
blocking the supply of said predetermined gas during the silicon crystal nuclei growth.

12. A method for manufacturing a capacitor lower electrode of a semiconductor memory device as claimed in claim 11, wherein the supply of said predetermined gas is simultaneously controlled in said step of supplying a predetermined gas.

FIG. 1A (PRIOR ART)

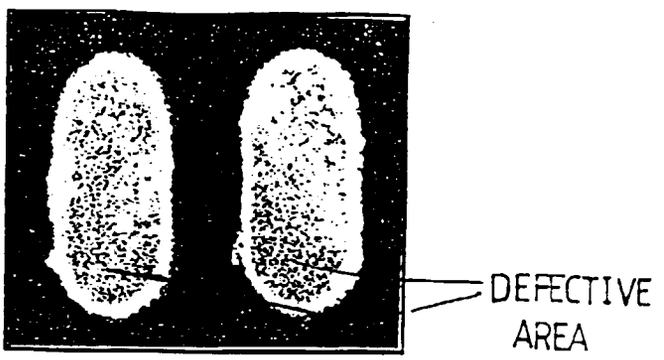


FIG. 1B (PRIOR ART)

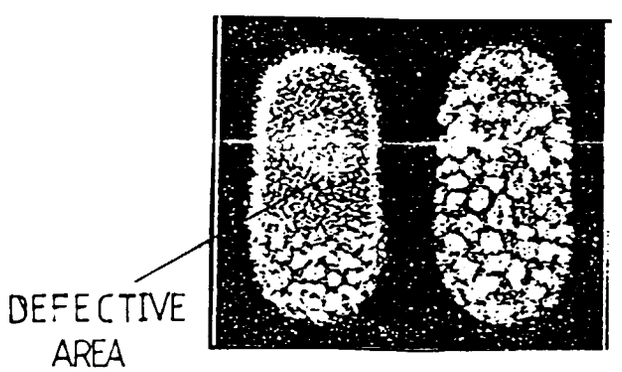


FIG. 2

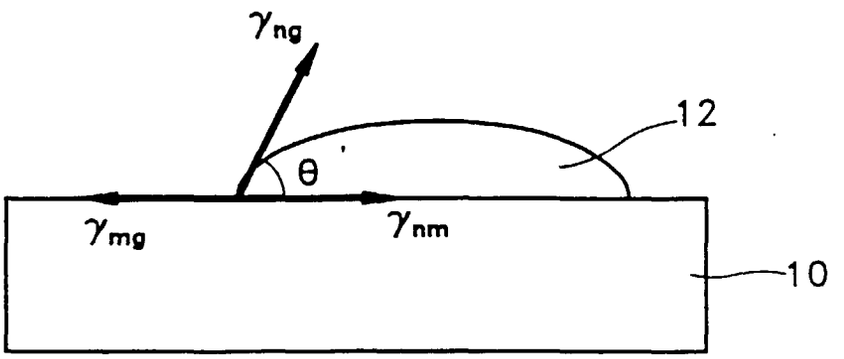


FIG. 3

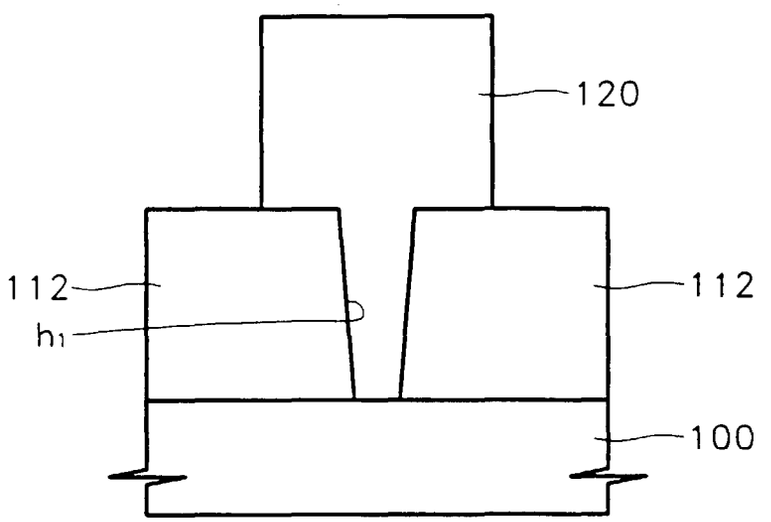


FIG. 4

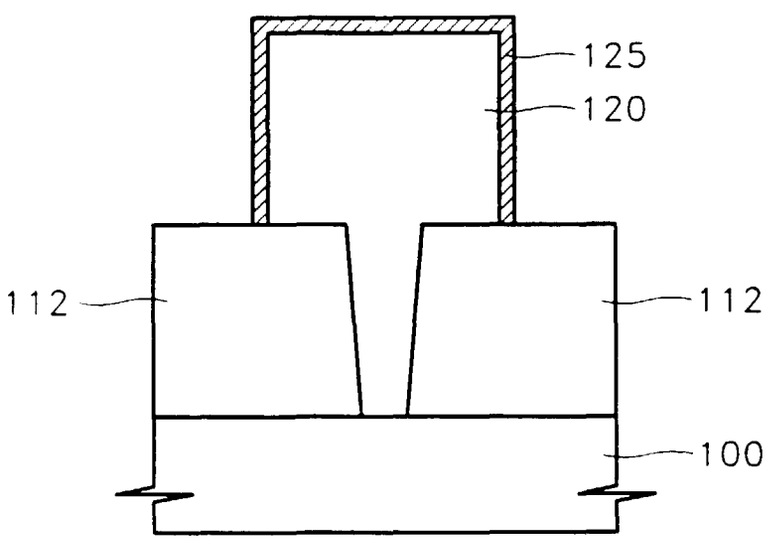


FIG. 5

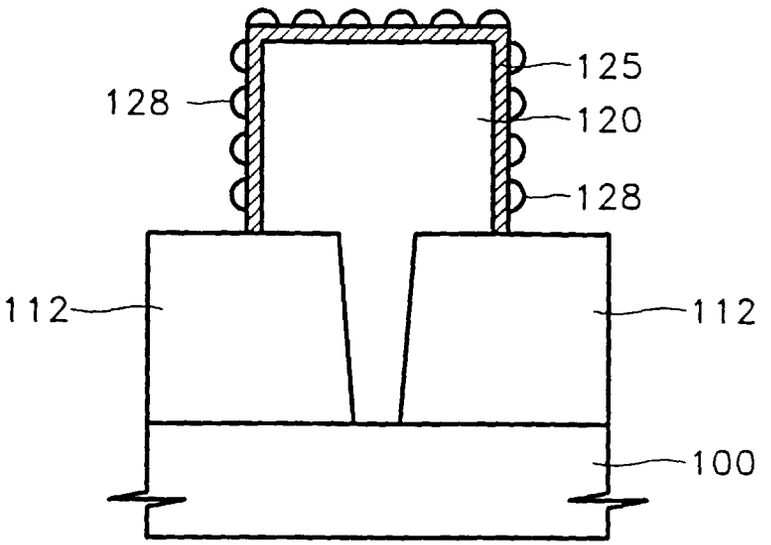
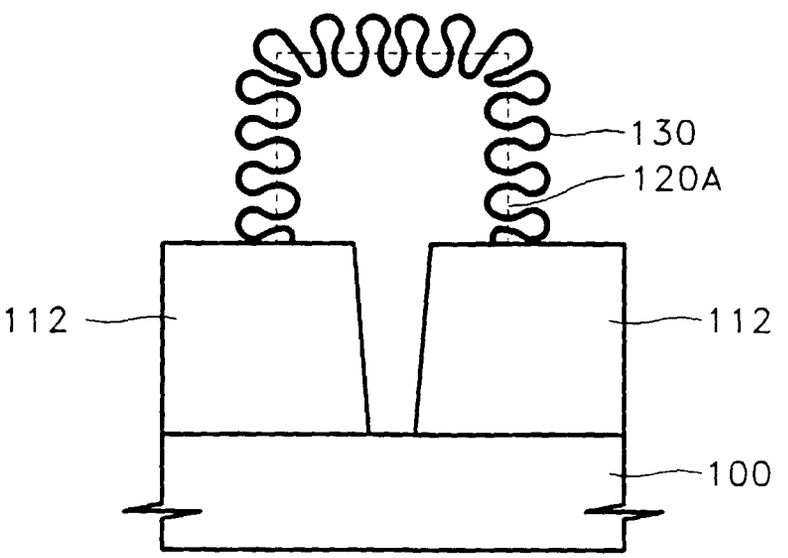
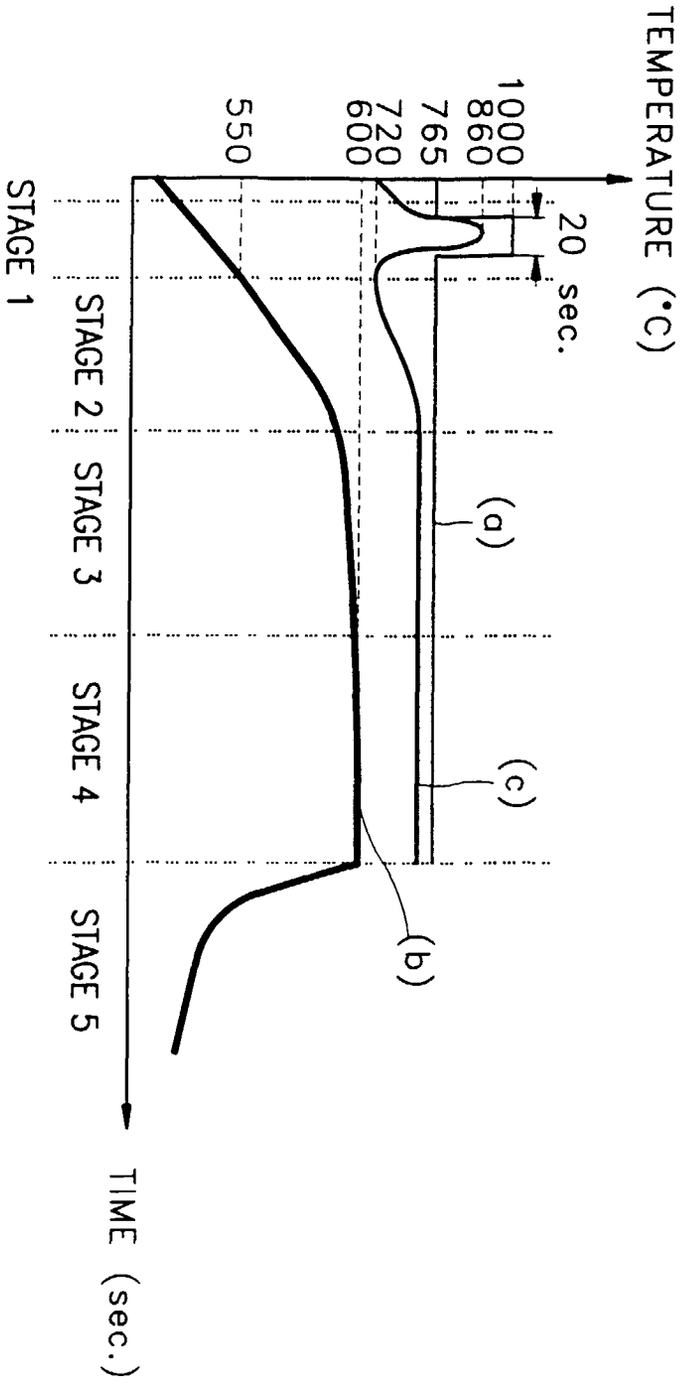


FIG. 6

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600
550
20 sec.
(a)
(c)
(b)
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
TIME (sec.)

FIG. 7

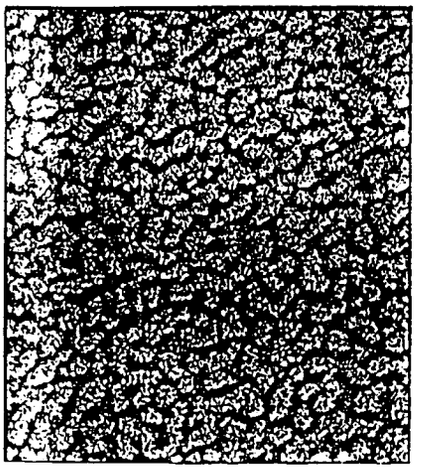


FIG. 8A

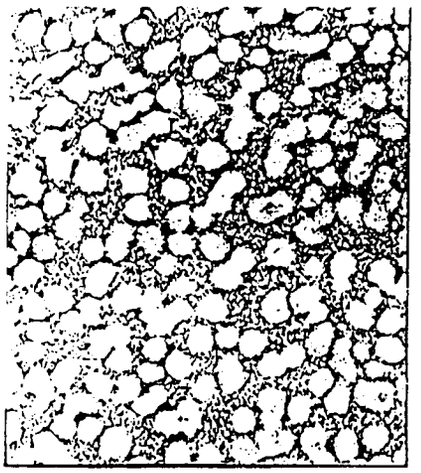


FIG. 8C

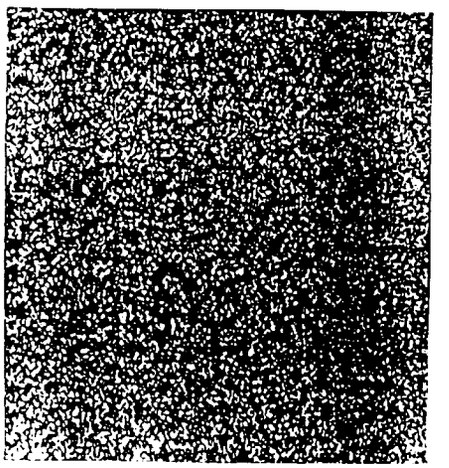


FIG. 8B

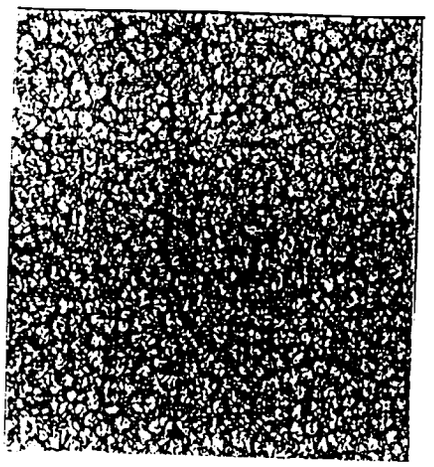


FIG. 8D

FIG. 9

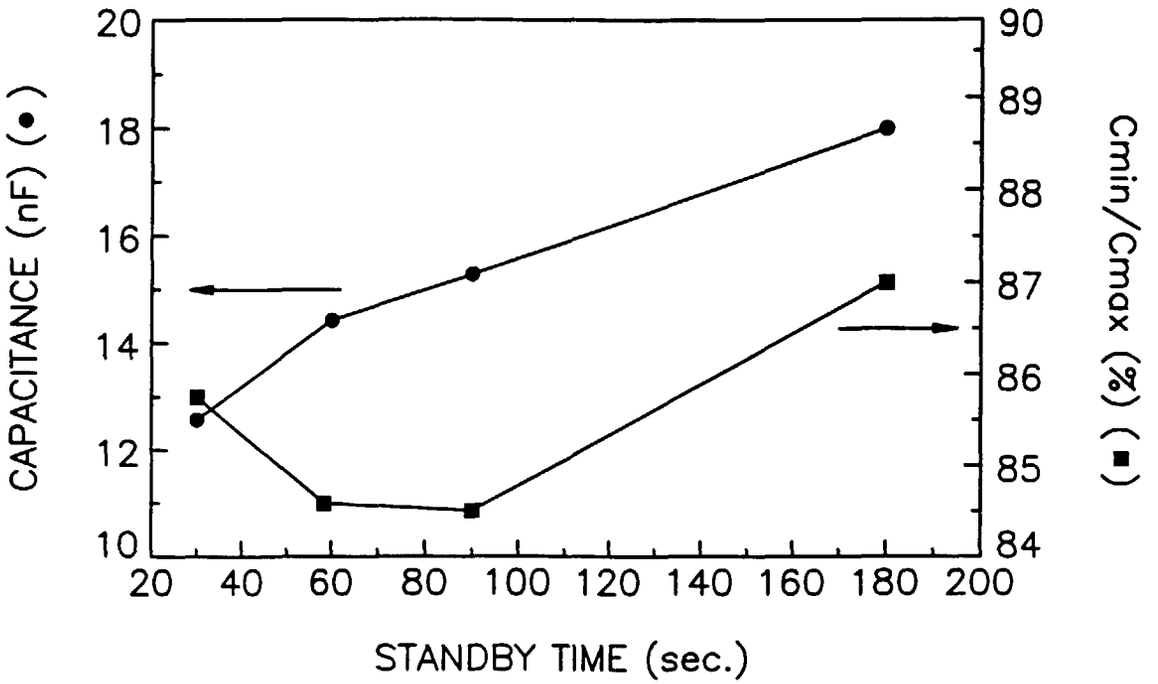

20
18
16
14
12
10
90
89
88
87
86
85
84
20 40 60 80 100 120 140 160 180 200
CAPACITANCE (nF) (•)
Cmin/Cmax (%) (■)
STANDBY TIME (sec.)

FIG. 10

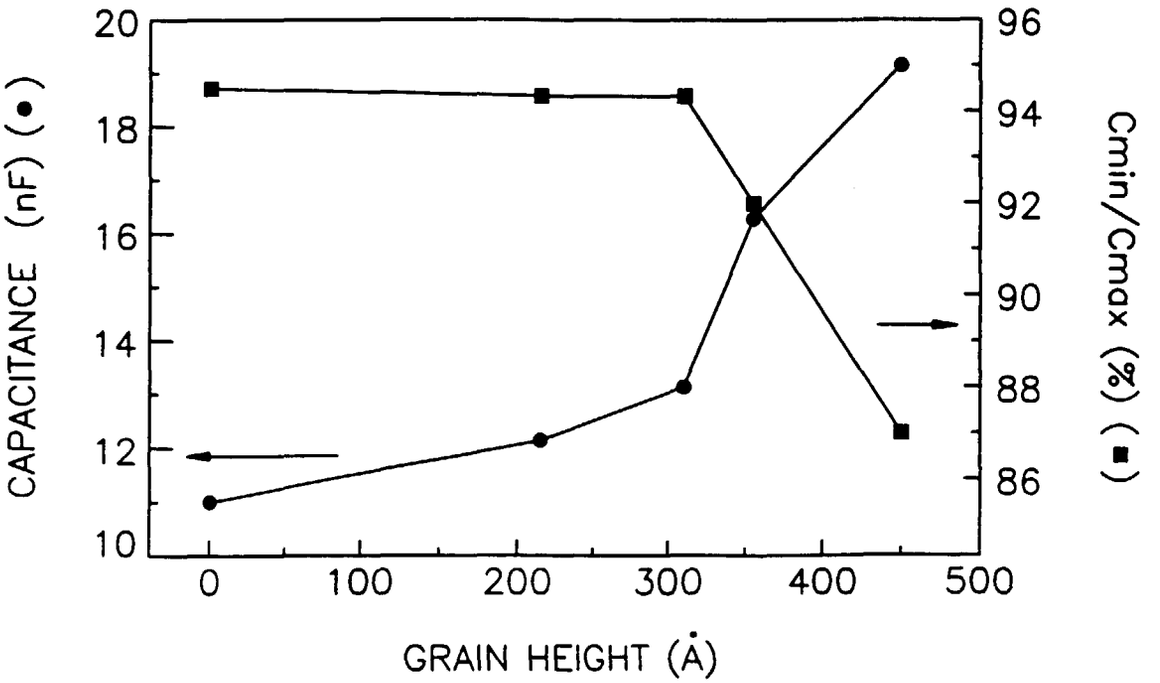

20
18
16
14
12
10
96
94
92
90
88
86
0 100 200 300 400 500
CAPACITANCE (nF) (•)
Cmin/Cmax (%) (■)
GRAIN HEIGHT (Å)

FIG. 11

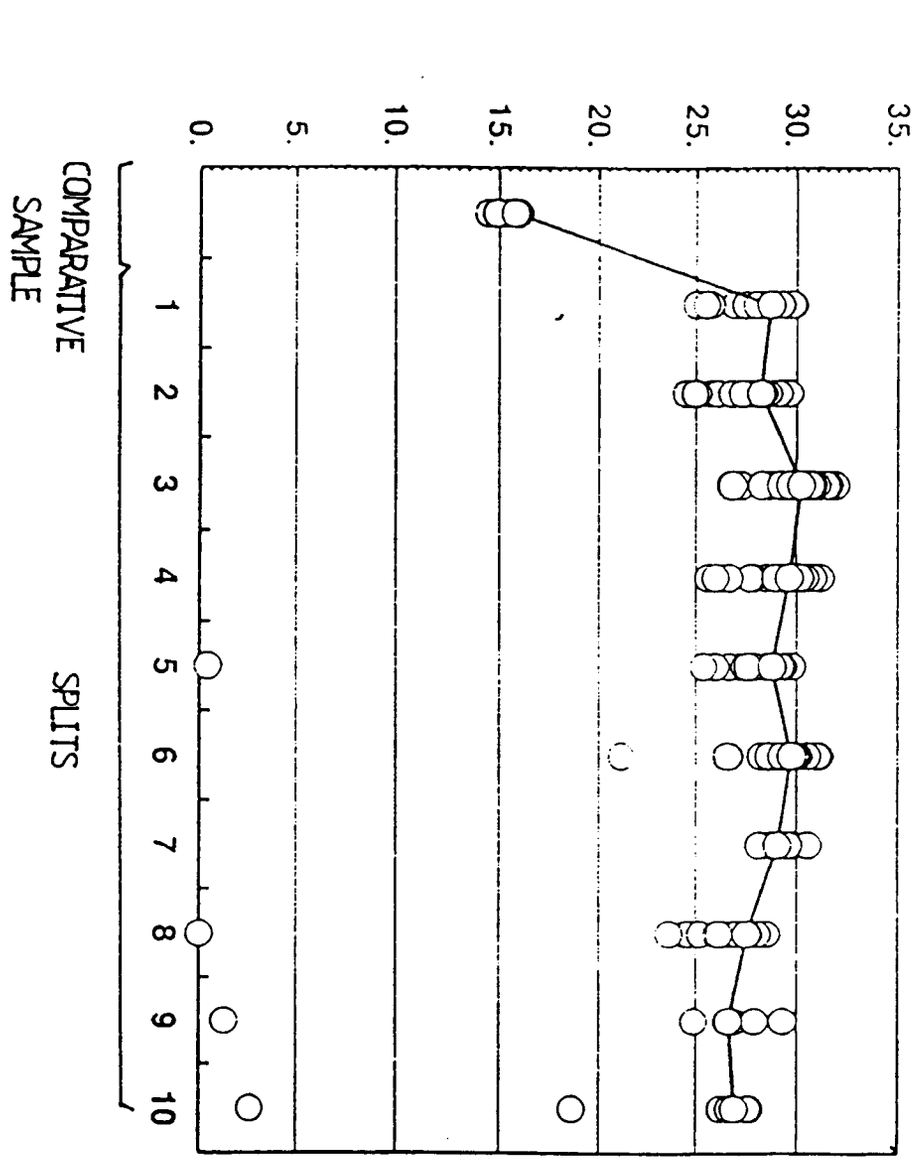
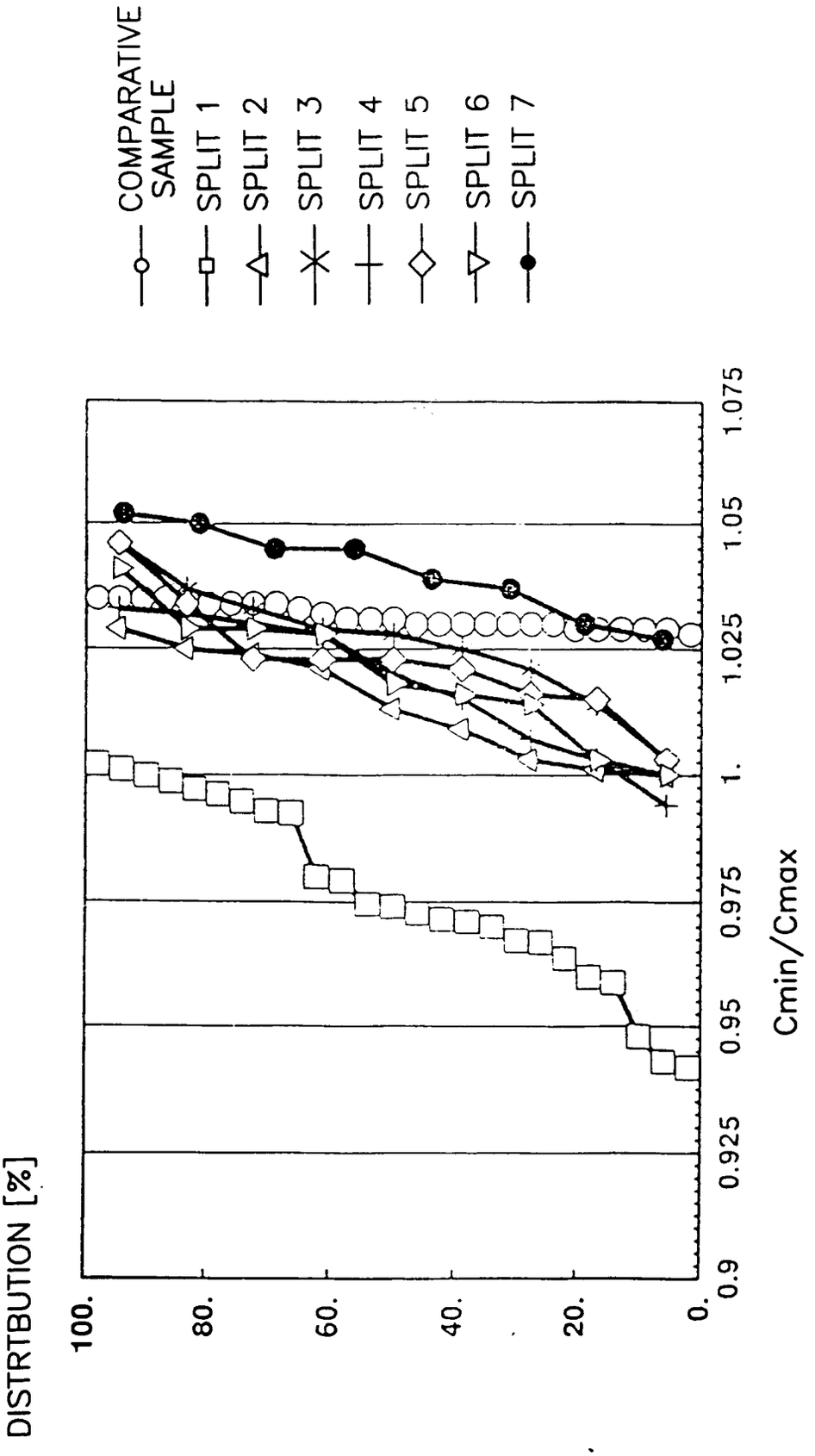

CAPACITNCE [fF/CELL]
35.
30.
25.
20.
15.
10.
5.
0.
1
2
3
4
5
6
7
8
9
10
COMPARATIVE SAMPLE
SPLITS

FIG. 12


COMPARATIVE SAMPLE
SPLIT 1
SPLIT 2
SPLIT 3
SPLIT 4
SPLIT 5
SPLIT 6
SPLIT 7
DISTRTBUTION [%]
100.
80.
60.
40.
20.
0.
0.9
0.925
0.95
0.975
1.
1.025
1.05
1.075
Cmin/Cmax

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 6946

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 731 491 A (NIPPON ELECTRIC CO) * column 3, line 10 - line 22 * * column 4, line 42 - line 51 * * column 23, line 19 - line 54 * * column 25, line 44 - column 26, line 27 * * claims 1,2 *	1-3,5-7, 10	H01L21/3205
A	-----	11	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 March 1998	Schuermans, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
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