(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 909 049 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
14.04.1999 Bulletin 1999/15

(51) Int. Cl.[6]: **H04B 15/04**, H04B 1/16

(21) Application number: **98250355.9**

(22) Date of filing: **07.10.1998**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **08.10.1997 JP 274903/97**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

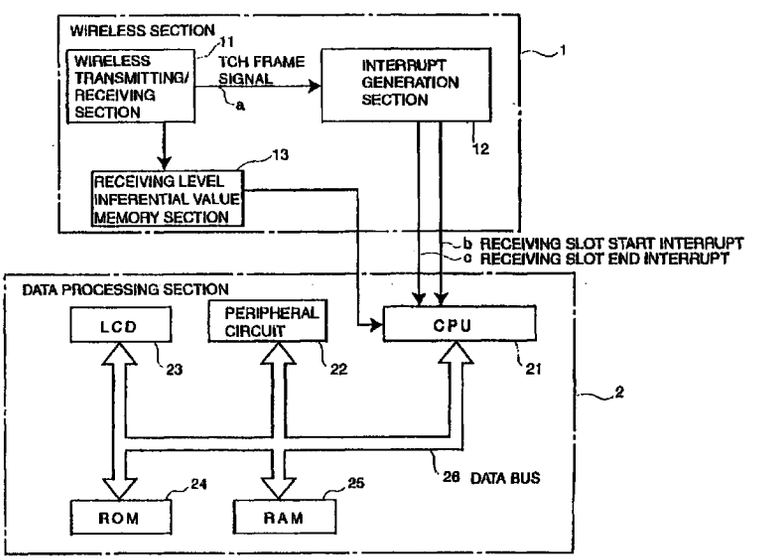
(72) Inventor: **Shimizu, Seiji**
Minato-ku, Tokyo (JP)

(74) Representative:
Patentanwälte Wenzel & Kalkoff
Grubesallee 26
22143 Hamburg (DE)

(54) Method for controlling the clock frequency of a wireless communication terminal

(57) The timing of a receiving slot at the wireless receiving section 11 is detected at the interrupt generation section 12, which generates a receiving slot start interrupt signal (b) and a receiving slot end interrupt signal (c), during a period between a relevant receiving slot start interrupt signal (a) and a receiving slot end interrupt signal (c), an operation clock frequency of the CPU 21 in the data processing section 2 is variably controlled according to a receiving electric field strength, whereby the deterioration of receiving performance due to noises running from the data processing section 2 to the wireless section 1 at the receiving time can be reduced.

FIG.1



EP 0 909 049 A2

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a wireless communication terminal. More particularly, it relates to a digital wireless portable information terminal in accordance with a Time Division Multiplexing Access (TDMA) communication method.

[0002] This type of digital wireless portable information terminal is constituted so as to include a wireless transmitting/receiving section and a data processing section processing data which this wireless transmitting/receiving section transmits and receives. Data processing is performed with a high speed clock (whose frequency is large) so that a CPU in the relevant data processing section operates at high speed.

[0003] In a digital portable information terminal having a built-in CPU which can be operated at such a high speed, it is obviously approved that noises generated with this high speed CPU plunge into the wireless transmitting/receiving section, which has bad influence upon operations of the relevant wireless transmitting/receiving section.

[0004] Particularly, since the required CPU operation speed becomes higher together with the enhancement of processing performance of a portable information terminal, noise generated has a tendency to increase still more. Therefore, it is a big problem to prevent the deterioration of sensitivity of a wireless section, particularly of a wireless receiving section due to noises at a terminal having a wireless communication function.

[0005] In order to achieve this, a method wherein a data processing section and a wireless receiving section are completely separated by a shield not to receive interference of noises for the wireless receiving section is often employed. However, together with a tendency of the miniaturization of terminals, the method for noise removal made by this shield involves a problem in that it needs a space for packaging and can not obtain an adequate effect of noise removal.

SUMMARY OF THE INVENTION

[0006] The objective of the present invention is to solve the problems of the prior art. Moreover, the objective is to provide a wireless communication terminal that can efficiently prevent noises vis-à-vis a wireless receiving section without employing a shield mechanism which requires space for packaging.

[0007] The present invention, which is a wireless communication terminal, is characterized in that it comprises a wireless transmitting/receiving section transmitting and receiving data, detecting means detecting the receiving electric field strength at the foregoing wireless transmitting/receiving section and operation clock control means controlling the frequency of an operation clock for processing data transmitted and received by the foregoing wireless transmitting/receiving section on the basis of a receiving electric field strength detected by the foregoing detecting means.

[0008] Then, the foregoing operation clock means is constituted so as to control the frequency of an operation clock to be come smaller as a receiving electric field strength becomes smaller.

[0009] Moreover, the wireless transmitting/receiving means has memory means memorizing the value of the receiving electric field strength. The operation clock control means is characterized in that it is constituted so as to control the frequency of an operation clock according to the receiving electric field strength memorized by this memory means.

[0010] Furthermore, the wireless transmitting/receiving means performs transmitting/receiving processing in accordance with a Time Division Multiplexing Access (TDMA) communication method. The operation clock control means is characterized in, that it is constituted so as to control the frequency of an operation clock by its being synchronized with the timing of a time division receiving operation.

[0011] Moreover, the wireless transmitting/receiving means is constituted so as to generate an interrupt signal at a starting time of a receiving slot that is a timing of the time division receiving operation and an interrupt end signal at an ending time of said receiving slot. The operation clock control means is characterized in that it performs controlling the frequency of the foregoing operation clock according to the foregoing receiving electric field strength in response to the foregoing interrupt signal and ends off controlling the frequency of the foregoing operation clock in response to the foregoing interrupt end signal.

[0012] Specifically, the present invention will reduce noises generated from the data processing section and secure receiving performance without deteriorating processing performance of the data processing section so much by this means that the operation clock frequency of the CPU in the data processing section is constituted so as to be synchronized with a timing that a receiving slot of the wireless receiving section exists and be variably controlled according to a wireless receiving electric field strength.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and other objectives, features and advantages of the present invention will become more apparent upon reading the following detailed description and drawings, in which:

Fig. 1 is a block diagram of an embodiment of the present invention;

Fig. 2 is a timing chart showing the operation of the embodiment of the present invention;

Fig. 3 is a graphical presentation showing an example of the correlation between a receiving input level

and a receiving level inferential value;

Fig. 4 is a circuit diagram showing an example of an interrupt signal generation section 12;

Fig. 5A and 5B are flow charts showing examples of clock frequency control operations of a CPU 21; and

Fig. 6 is a circuit diagram showing an example of a clock selection function of the CPU 21.

DESCRIPTION OF THE EMBODIMENT

[0014] The embodiment of the present invention will be described below.

[0015] Fig. 1 is a block diagram of the embodiment of the present invention.

[0016] In Fig. 1, reference numeral 1 is a wireless section which transmits and receives data in accordance with the Time Division Multiplexing Access (TDMA) commnunication method. Reference numeral 2 is a data processing section that processes data transmitted and received at the wireless section 1.

[0017] The wireless section 1 has a wireless transmitting/receiving section 11, an interrupt signal generation section 12 for receiving a TCH (Transmission Channel) frame signal (a) sent from the wireless transmitting/receiving section 11 as an input and generating a receiving slot start interrupt signal (b) which is synchronized with a start timing of a receiving time slot and a receiving slot end interrupt signal (c) which is synchronized with an ending timing of the receiving time slot, and a receiving level inferential value memory section 13 for detecting and storing a receiving electric field strength at the wireless transmitting/receiving section 11.

[0018] The data processing section 2 has a CPU 21 in which the operation clock frequency is variably controlled and data is processed with a controlled operation clock, its peripheral circuit 22, a display section of LCD 23 for performing various types of displays, a ROM 24 for read-only, a RAM 25 for freely read/write, and a data bus 26 for connecting respective these sections. The CPU 21 operates synchronizing with an operation clock which determines its operation speed. The frequency of this clock can be controlled according to a receiving level at the receiving level inferential value memory section 13. Moreover, the timing of frequency control of the operation clock is controlled in response to a receiving slot start interrupt signal (b), and a clock frequency return is controlled in response to a receiving slot end interrupt signal (c).

[0019] Fig. 2 is a timing chart showing the relationship between a TCH (Transmission Channel) frame signal (a) which is a standard interface signal utilized when performing data communication in accordance with the PDC (Personal Digital Cellular) method, a mobile unit receiving slot (receiving timing), a receiving slot start interrupt signal (b), and a receiving slot end interrupt signal (c). Hereupon, assume that a slot #0 is a receiving slot of a relevant terminal.

[0020] A TCH frame (a) indicating a period of this slot #0 is active during the period and is led out from the wireless transmitting/receiving section 11 to the interrupt generation section 12. Both a start interrupt signal (b) which is synchronized with a starting timing of this TCH frame signal (a), and an end interrupt signal (c) which is synchronized with an end timing of the TCH frame signal (a) are generated from the interrupt generation section 12.

[0021] The CPU 21 starts controlling an operation clock frequency in response to this start interrupt signal (b) and determines the clock frequency according to a receiving level inferential value stored at the receiving level inferential memory section 13.

[0022] Fig. 3 is a graphical presentation showing the correlation between a receiving input level and a receiving level inferential value stored at the receiving level inferential value memory section 13 and also showing the cases indicated by three (3) stages in which respective receiving level inferential values are large, medium and small.

[0023] The receiving level inferential value memory section 13 selects and memorizes a receiving level inferential value corresponding to a receiving electric field strength (a receiving input level) detected at the wireless transmitting/receiving section 11 according to the graphical presentation of the correlation shown in Fig. 3. According to Fig. 3, clock frequencies are variably controlled in compliance with receiving level inferential values of those three (3) stages.

[0024] Fig. 4 is a circuit diagram showing an example of the interrupt generation section 12. In Fig. 4, a TCH frame signal (a) is shown as data input supplied to a DFF (D-type Flip-Flop circuit) 121, and a clock signal is supplied to the DFF as a clock input. The reversed Q output of this DFF 122 is shown as an input supplied to an AND gate 122 and as an input supplied to an OR gate 123 respectively. As the other input, a TCH frame signal (a) is supplied to the AND gate and to the OR gate respectively. Moreover, a start interrupt signal (b) as an output outputted from the AND gate 122 and an end interrupt signal (c) as an output outputted from the OR gate 123 are led out respectively.

[0025] Fig. 5A and Fig. 5B are flow charts showing processing operations of clock control of the CPU 21. Fig. 5A is a control flow chart in the case of receiving a receiving slot start interrupt signal, in which, responding to a start interrupt signal (Step 100), the CPU 21 reads out and determines a receiving level inferential value from the memory section 13 (Step 101). If the level is at the stage of "large" (Step 102), the clock frequency is not variably controlled (Step 103). Moreover, if the level is at the stage of "medium" (Step 104), the clock frequency is lowered to be 1/4 of the original frequency (Step 105). Furthermore, if the level is at the stage of "small" (Step 106), the clock frequency is lowered to be 1/16 of the original frequency (Step 107).

[0026] Then, as shown in the flow chart of Fig. 5B, responding to a receiving slot end interrupt signal (c) (Step 200), the clock frequency is made to be returned to the original frequency (to the reference frequency before variable controlled) (Step 201).

[0027] Fig. 6 is a circuit block diagram for clock control, which includes a crystal oscillator 211 for oscillating a reference frequency signal, a PLL (Phase Locked Loop) circuit 212 for generating a clock phase-synchronized with an oscillation frequency of the crystal oscillator 211, dividers 213, 214 for making frequencies be 1/4 and 1/16 of the original frequencies by performing frequency division, and a selector 215 for selectively leading out one output out of an output outputted from the PLL circuit 212 and frequency division outputs outputted from the dividers 213, 214.

[0028] Clock frequency is freely controlled by the selector 215 selecting control according to a clock control signal on the basis of a receiving level inferential value read out from the receiving level inferential value memory section 13.

[0029] Specifically, if the receiving level inferential value is at the stage of "large", the selector 215 selects an output outputted from the PLL circuit 212, selects an output outputted from the divider 213 if the receiving level inferential value is at the stage of "medium", and selects an output outputted from the divider 214 if the receiving level inferential value is at the stage of "small".

[0030] As described above, according to the present invention, noise generation at the receiving section can be prevented by reducing the frequency of an operation clock of the CPU in the case where a receiving electric field is weak at a timing that a receiving slot exists, and in the other cases, an effect of noise reduction can be obtained by the clock frequent remaining to be at a high speed without sacrificing data processing speed.

[0031] Moreover, wireless noises will be a problem manly at a receiving signal. Therefore, by making the operation frequency of the CPU to be synchronized with a receiving slot and controlling it, it is not necessary to strictly settle a shield designed for wireless noises. Consequently, an effect of miniaturizing and lightening a portable terminal can be also provided.

[0032] The entire disclosure of Japanese Patent Application No. 9-274903 filed on October 8, 1997 including specification, claims, drawings and summary are incorporated herein by reference in its entirety.

Claims

1. A wireless communication terminal comprising:

   wireless transmitting/receiving means which transmits and receives data;
   detecting means detecting a receiving electric field strength at said wireless transmitting/receiving means; and
   operation clock control means controlling a frequency of an operation clock for processing data transmitted and received by said wireless transmitting/receiving means based on a receiving electric field strength detected by said detected means.

2. The wireless communication terminal according to claim 1, wherein said operation clock control means has means controlling the frequency of an operation clock to be smaller as the receiving electric field strength becomes smaller.

3. The wireless communication terminal according to claim 1, wherein said detecting means has memory means memorizing the measured value of the detected receiving electric field strength, and

   said operation clock control means has means controlling the frequency of said operation clock based on the receiving electric field strength memorized by said memory means.

4. The wireless communication terminal according to said claim 1, wherein a predetermined number of receiving level inferential values is stored in advance and said detecting means has means for selecting said receiving level inferential value from said previously stored receiving level inferential values corresponding to the detected receiving electric field strength and maintaining said receiving level inferential value, and

   said operation clock control means has a predetermined number of operation clock generation means generating operation clocks corresponding to said receiving level inferential values and selecting means selecting said operation clock generation means corresponding to a receiving level inferential value maintained at said detecting means.

5. The wireless communication terminal according to claim 1, wherein said wireless transmitting/receiving means is means performing transmitting/receiving processing in accordance with a Time Division Multiplexing Access (TDMA) communication method, and

   said operation clock control means is means controlling the frequency of an operation clock by its being synchronized with the timing of a time division receiving operation of said wireless transmitting/receiving section.

6. The wireless communication terminal according to claim 5, wherein said wireless transmitting/receiving means has means generating an interrupt signal at a starting time of a receiving slot that is a

timing of the time division receiving operation and an interrupt end signal at an ending time of said receiving slot, and

said operation clock control means has means controlling an operation clock to be a frequency according to said receiving electric field strength in response to said interrupt signal and ending off controlling the frequency of said operation clock in response to said interrupt end signal.

7. A wireless communication terminal comprising:

wireless transmitting/receiving means generating an interrupt signal at a starting time of a receiving slot that is a timing of a time division receiving operation and an interrupt end signal at an ending time of said receiving slot as well as transmitting and receiving data,
detecting means detecting the receiving electric field strength at said wireless transmitting/receiving means and selecting said receiving level inferential value corresponding to said detected receiving electric field strength from a predetermined number of receiving level inferential values stored in advance and maintaining said receiving level inferential value;
a predetermined number of operation clock generation means generating operation clocks corresponding to said receiving level inferential values;
selecting means selecting operation clock generation means corresponding to a receiving level inferential value maintained at said detecting means out of said predetermined number of operation clock generation means in response to said interrupt signal and selecting an initially selected operation clock generation means in response to said interrupt end signal; and
data processing means processing data transmitted and received by said wireless transmitting/receiving means based on the operation clock of operation clock generation means selected by said selecting means.

8. In a wireless communication terminal, a method of controlling an operation clock for processing transmitting/receiving data, said method comprising the steps of:

detecting the receiving electric field strength; and controlling the frequency of an operation clock for processing transmitting/receiving data based on said detected receiving electric field strength.

9. The method of controlling an operation clock for processing transmitting/receiving data according to claim 8, wherein said control step is a step of controlling the frequency of an operation clock to be smaller as a detected receiving electric field strength becomes smaller.

10. The method of controlling an operation clock for processing transmitting/receiving data according to claim 8, wherein said detecting step, in which a plurality of receiving level inferential values are set in advance, is a step of selecting a receiving level inferential value corresponding to a detected receiving electric field strength out of said plurality of receiving level inferential values, and

said control step, in which a plurality of operation clocks corresponding to a plurality of receiving level inferential values are prepared in advance, is a step of selecting an operation clock corresponding to said selected receiving level inferential value out of said plurality of operation clocks.

11. The method of controlling an operation clock for processing transmitting/receiving data according to claim 8, wherein transmitting/receiving data is performed in accordance with a Time Division Multiplexing Access (TDMA) communication method, and

said control step is a step of controlling the frequency of said operation clock by its being synchronized with the timing of time division receiving operation.

12. The method of controlling an operation clock for processing transmitting/receiving data according to claim 11, wherein said control step is a step of starting controlling an operation clock at a starting time of a receiving slot and ending off controlling the frequency of said operation clock at an ending time of said receiving slot.

13. The method of controlling an operation clock for processing transmitting/receiving data according to claim 12, wherein said control step is a step of returning the frequency of an operation clock to a certain original frequency of said operation clock at an ending time of said receiving slot.

FIG.1

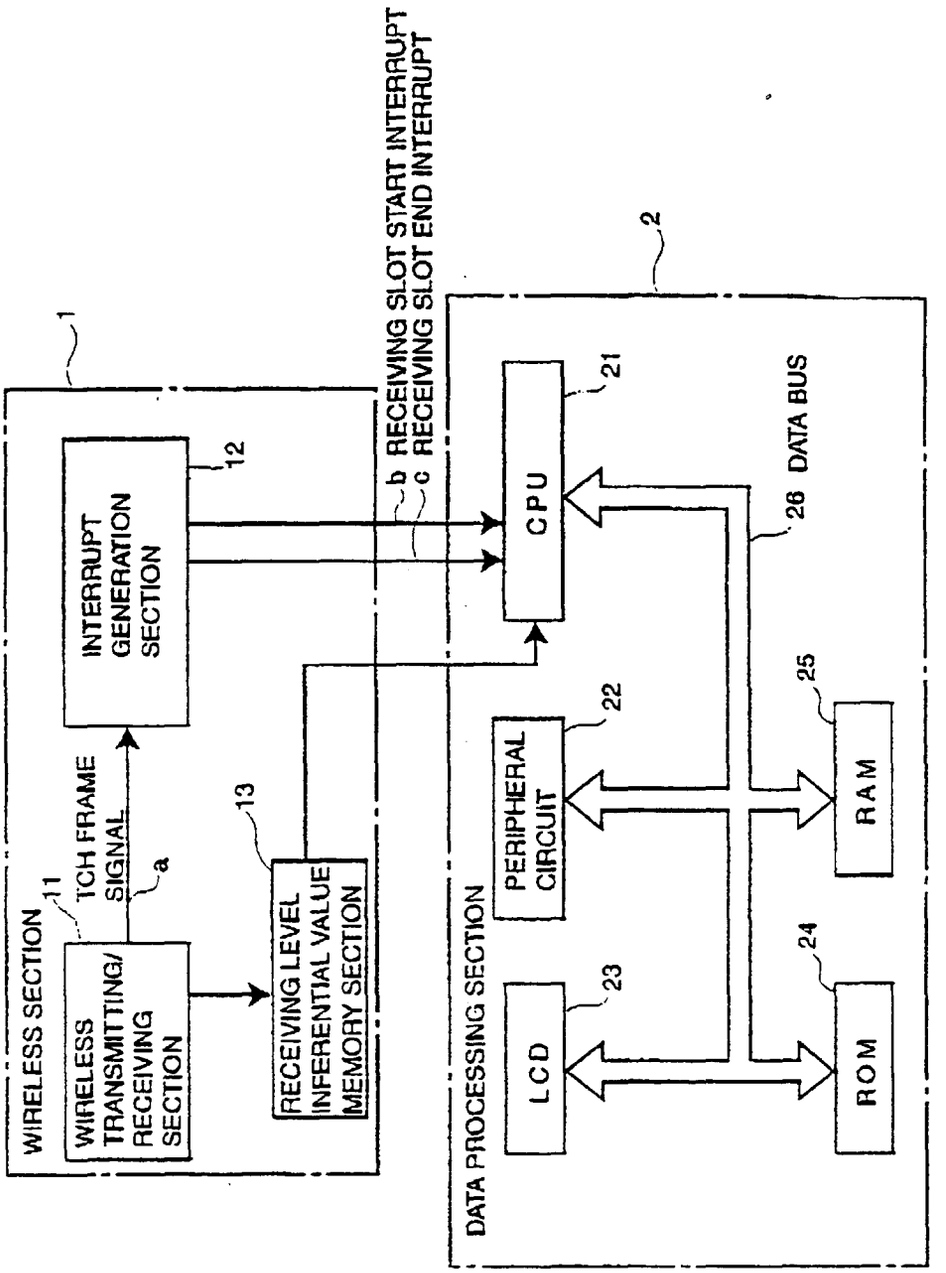

WIRELESS SECTION
1
WIRELESS TRANSMITTING/ RECEIVING SECTION
11
TCH FRAME SIGNAL
a
INTERRUPT GENERATION SECTION
12
RECEIVING LEVEL INFERENTIAL VALUE MEMORY SECTION
13
b RECEIVING SLOT START INTERRUPT
c RECEIVING SLOT END INTERRUPT
DATA PROCESSING SECTION
2
CPU
21
PERIPHERAL CIRCUIT
22
LCD
23
ROM
24
RAM
25
26 DATA BUS

FIG.2

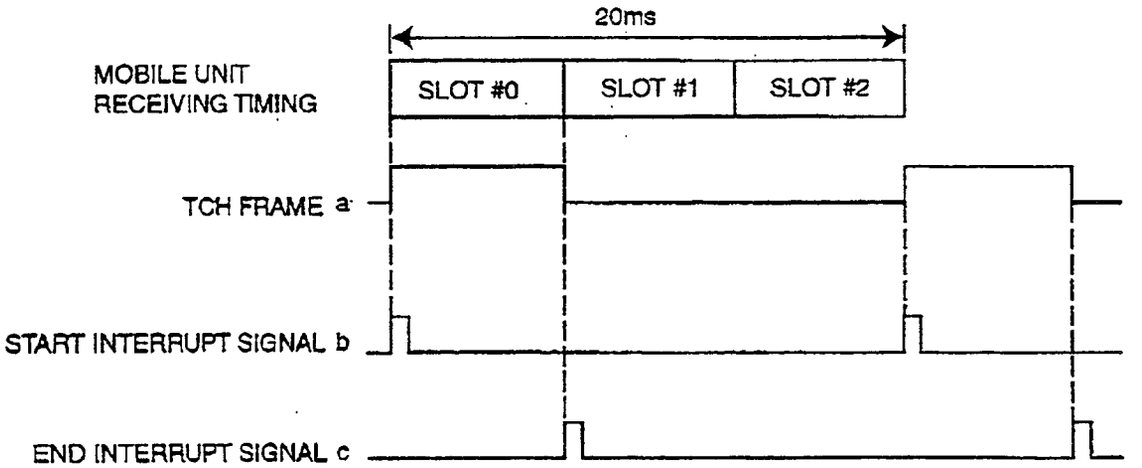

20ms
MOBILE UNIT
RECEIVING TIMING
SLOT #0
SLOT #1
SLOT #2
TCH FRAME a
START INTERRUPT SIGNAL b
END INTERRUPT SIGNAL c

FIG.3

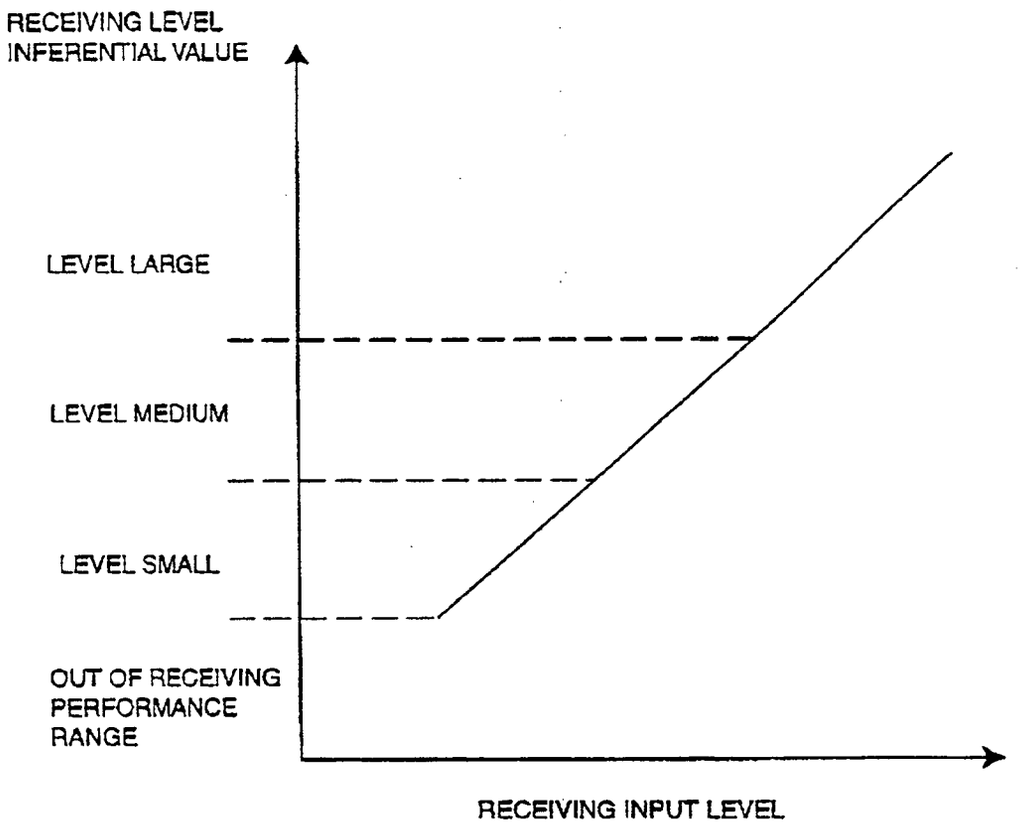

RECEIVING LEVEL
INFERENTIAL VALUE
LEVEL LARGE
LEVEL MEDIUM
LEVEL SMALL
OUT OF RECEIVING
PERFORMANCE
RANGE
RECEIVING INPUT LEVEL

FIG.4

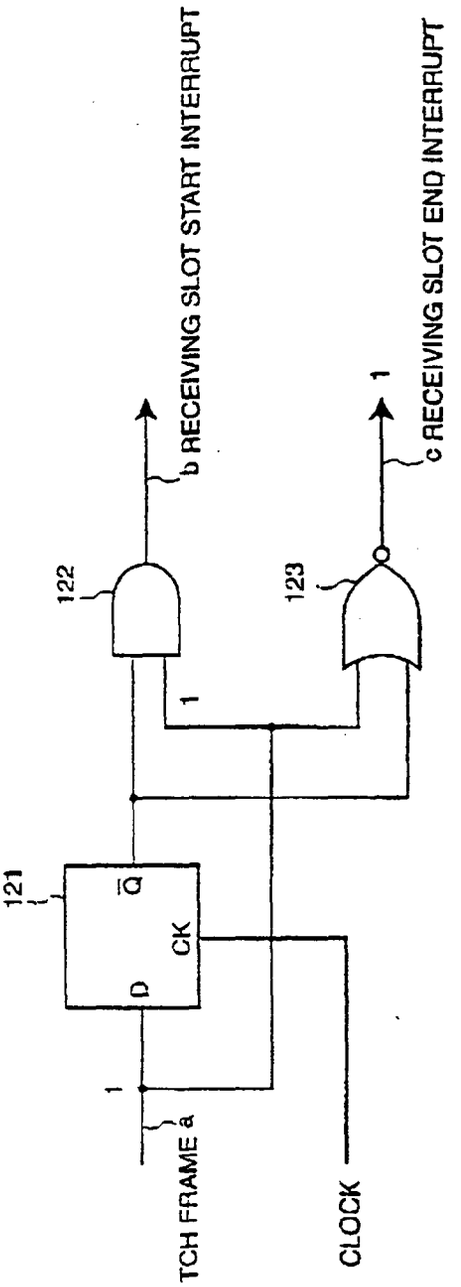

121
D
CK
Q
1
TCH FRAME a
CLOCK
122
1
b RECEIVING SLOT START INTERRUPT
123
1
c RECEIVING SLOT END INTERRUPT

FIG.5A

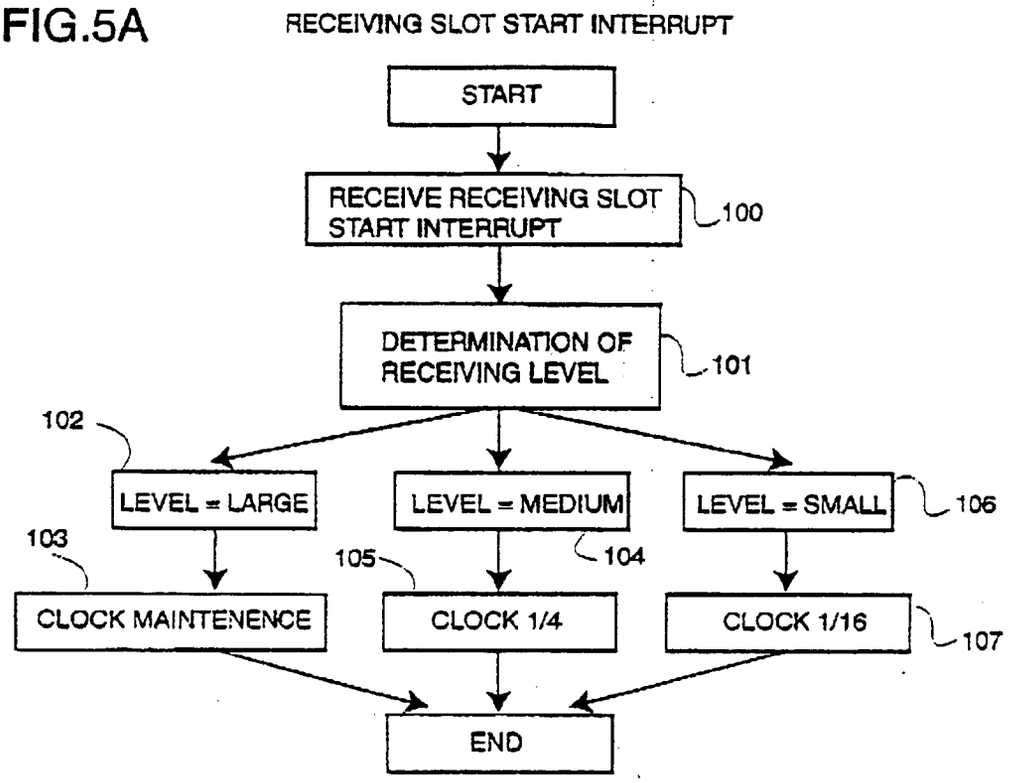

RECEIVING SLOT START INTERRUPT
START
RECEIVE RECEIVING SLOT START INTERRUPT
100
DETERMINATION OF RECEIVING LEVEL
101
102
LEVEL = LARGE
LEVEL = MEDIUM
LEVEL = SMALL
106
103
105
104
CLOCK MAINTENENCE
CLOCK 1/4
CLOCK 1/16
107
END

FIG.5B

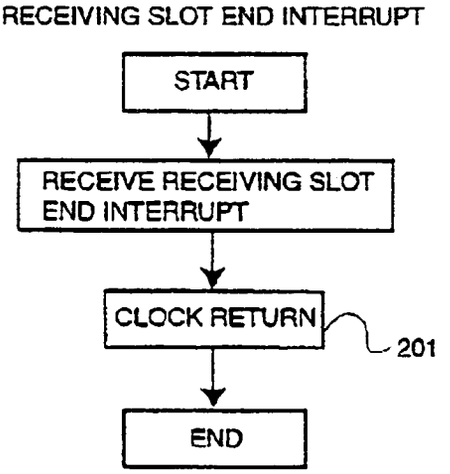
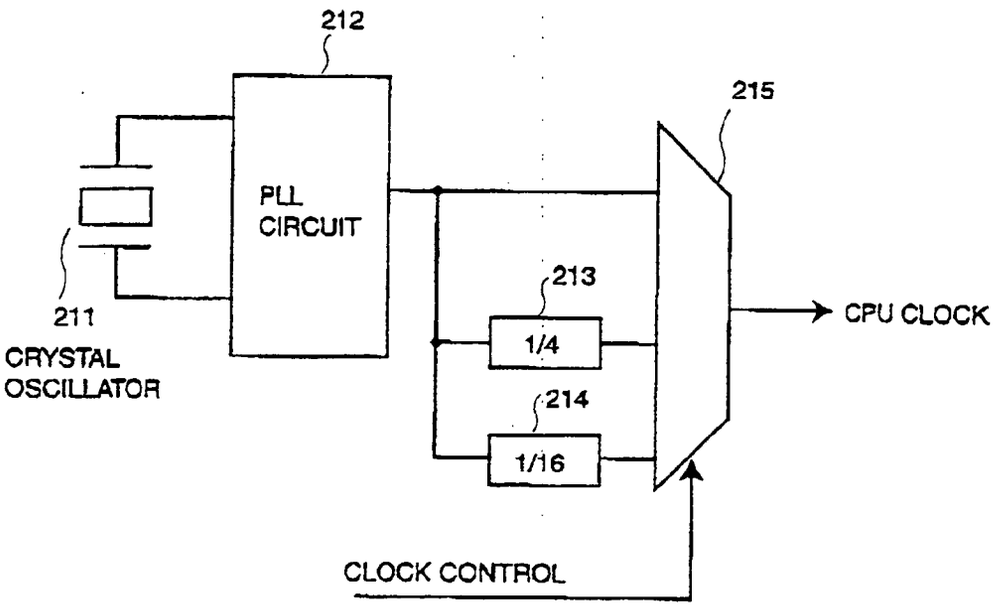

RECEIVING SLOT END INTERRUPT
START
RECEIVE RECEIVING SLOT END INTERRUPT
CLOCK RETURN
201
END

FIG.6


212
215
PLL
CIRCUIT
213
211
CRYSTAL
OSCILLATOR
1/4
CPU CLOCK
214
1/16
CLOCK CONTROL