(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 915 408 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
12.05.1999 Bulletin 1999/19

(51) Int. Cl.[6]: **G05F 1/00**, G05F 1/46

(21) Application number: **97830575.3**

(22) Date of filing: **05.11.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

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Remarks:
Claim 18 is deemed to be abandoned due to non-payment of the claims fee (Rule 31 (2) EPC).

(54) High voltage regulator and corresponding voltage regulation method

(57) This invention relates to a high voltage regulator partly supplied by a boosted voltage (PUMPOUT) and adapted to deliver a regulated output voltage (Vout) on an output terminal (OUT), starting from a sampled voltage (Vsample) obtained by dividing the regulated output voltage (Vout), which regulator comprises at least a comparator element (2) being supplied a supply voltage (Vdd) and feedback connected to a divider (4) of the regulated output voltage (Vout), the divider (4) being a diode type of divider connected between the output terminal (OUT) and a first comparison voltage reference (GND, Vref_v) and having a central connection node (Y, Z) connected to a non-inverting terminal of the comparator element (2).

The invention also relates to a method of regulating a voltage (Vout) derived from a boosted voltage (PUMPOUT), comprising the steps of:

- obtaining a sampled voltage (Vsample) as the voltage value at a central connection node (Y, Z) of a diode type of divider (4) connected to a reference of the voltage to be regulated (Vout) and connected to a first comparison voltage reference (GND, Vref_v);

- regulating this voltage (Vout) according to the comparison of said sampled voltage (Vsample) with a second comparison voltage reference (Vref_v, GND).

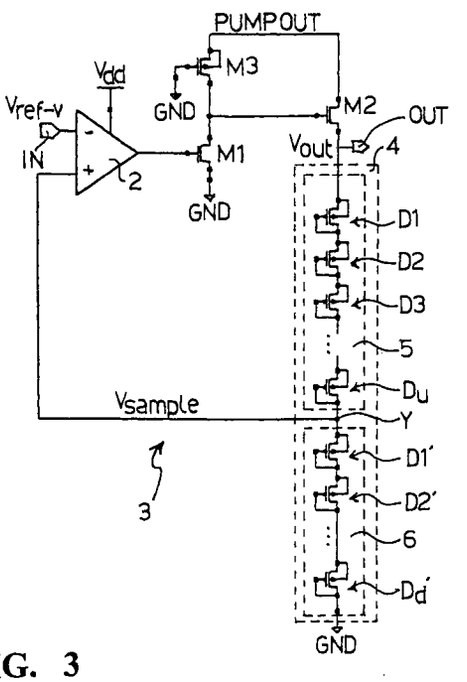

FIG. 3

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Description

Field of the Invention

[0001] This invention relates to a high voltage regulator.

[0002] The invention specifically relates to a high voltage regulator which is partly supplied by a boosted voltage and is adapted to deliver a regulated output voltage on an output terminal, starting from a sampled voltage obtained by dividing the regulated output voltage, which regulator comprises at least a comparator element being supplied by a supply voltage and feedback connected to a divider of said regulated output voltage.

[0003] The invention also concerns a method of regulating a voltage obtained from a boosted voltage.

[0004] The invention particularly, but not exclusively, relates to a high voltage regulator for a memory of the 'flash' type, and the description which follows is given in connection with this field of application for simplicity of illustration only.

Background Art

[0005] As is well known, many applications concerning electronic circuits integrated in a semiconductor require that voltages above the supply voltage Vcc and below the ground voltage reference GND be generated. This requirement is most stringent with devices which are supplied by a low voltage, as in the current trend for many electronic devices among which are electrically programmable and erasable non-volatile memories.

[0006] A boosted voltage is usually generated by means of a voltage multiplier or "booster" circuit, which is purposely formed within the integrated circuit itself.

[0007] The booster circuit output is not at a regulated value but depends to supply voltage, temperature, output current, and process factors.

[0008] In such cases, it becomes necessary to smooth the output voltage Vout by means of a purposely provided regulator circuit. In particular, a regulator for a voltage multiplier circuit of the charge pump type, i.e. a high voltage regulator, must be designed with high accuracy criteria because charge pump circuits can only supply limited value currents.

[0009] Basic requirements for a regulator of high voltages generated by a booster circuit of the charge pump type are:

- low current consumption by the charge pump booster circuits which supply the high voltage to be regulated;
- high precision, especially as regards absence of overshoot and ripples in the regulated voltage, and its independence of the parasitic effects that are typical of high voltages;
- sufficiently fast settling during transient phases, such as the regulator triggering phase;
- low space requirements, i.e. reduced occupation of silicon area.

[0010] A high voltage regulator 1 according to the prior art is shown schematically in Figure 1 appended hereto.

[0011] The high voltage regulator 1 is partly supplied by a boosted voltage PUMPOUT generated by a charge pump circuit which supplies a high voltage at a small current capacity.

[0012] The output voltage Vout is regulated by resistive division of the boosted voltage PUMPOUT.

[0013] In this way, an output voltage Vout can be obtained for the high voltage regulator 1.

[0014] The voltage regulator 1 comprises a resistive divider consisting of two resistive elements R1 and R2, connected between an output terminal OUT and a ground voltage reference GND. The central connection node X of the resistive elements R1 and R2 is connected to a non-inverting input terminal of a comparator element 2 having an inverting input terminal connected to an input terminal IN of the high voltage regulator 1 and a supply terminal connected to a supply voltage reference Vdd.

[0015] The input terminal IN of the high voltage regulator 1 receives a reference voltage Vref of constant value, usually for utilisation by several circuits in the same device.

[0016] The comparator element 2 also has an output terminal connected to the supply terminal of a drive transistor M1.

[0017] The drive transistor M1, specifically one of the NMOS type, has its source terminal connected to the ground voltage reference GND and its drain terminal connected to the control gate terminal of an output transistor M2, itself connected between the boosted voltage reference PUMPOUT and the output terminal OUT of the high voltage regulator 1.

[0018] The high voltage regulator 1 further includes a load transistor M3, specifically one of the PMOS type, which is connected between the boosted voltage reference PUMPOUT and the control gate terminal of the output transistor M2 and has its control gate terminal connected to the ground voltage reference GND. This load transistor M3 has the n-well terminal connected to its source terminal and, hence, to the boosted voltage reference PUMPOUT.

[0019] The regulated output voltage Vout is sampled by the resistive divider of the high voltage regulator 1, which then provides a feedback of the same. Therefore, the value of this regulated output voltage Vout will be dependent on both the value of the reference voltage Vref and the ratio of the resistive divider R1, R2.

[0020] While achieving its objective, this solution is less than fully satisfactory and has certain drawbacks.

[0021] A major problem originates from the resistive

divider R1, R2.

[0022] First, to conform with the above requirement for the charge pump booster circuit supplying the boosted voltage PUMPOUT to have a low current consumption, this resistive divider, and particularly the combined resistances of the resistors R1 and R2, should be rather large (in the MΩ range).

[0023] However, the use of a resistive divider of this size clashes with the other requirements set forth above for the high voltage regulator 1, namely precision, speed, and low space occupation. In fact, to provide an integrated resistor, there are essentially two methods that can be used:

- formation in an n^+ diffusion;

- formation in an n-well.

[0024] Actually, in view of the size (in the MΩ range) involved, only the last-mentioned method can be used for forming the resistive divider of the prior art high voltage regulator 1, since the n-well of an integrated circuit has a higher specific resistivity than n^+ diffusions. An n-well resistor is shown schematically in Figure 2.

[0025] Unfortunately, resistors formed in n-wells give rise to two important problems:

1. They exhibit a high parasitic capacitance Cpar toward the substrate layer of the integrated circuit.

2. They exhibit a varying resistance, dependent in particular on the voltages applied across them, due to the depleted reverse-biases area that exists between the n-well and the substrate.

[0026] Referring to the high voltage regulator 1 shown in Figure 1, the parasitic capacitance associated with a resistive divider so formed causes delayed following of a divided voltage Vsample at the central connection node X of the resistive elements R1 and R2 with respect to variations occurring in the regulated output voltage Vout.

[0027] This delay reflects in a slowed settling of the output voltage Vout, as well as overshooting and rippling thereof, in contrast with the requirements set above for the high voltage regulator 1.

[0028] In addition, the varying character of the resistance of the divider formed in the n-well makes it difficult to obtain a desired value for the regulated output voltage Vout. In fact, this varying resistance is difficult to model and reproduce. Thus, the high voltage regulator 1 incorporating such a divider is unsuitable to meet the aforementioned requirements.

[0029] The underlying technical problem of this invention is to provide a high voltage regulator, in particular for voltages supplied by booster circuits, which exhibits low current consumption and high precision features, as well as sufficient speed during the transient phases, with no overshoot and ripples, and reduced space requirements. In this way, the requirements for such regulators can be met and the drawbacks besetting the prior art regulators overcome.

Summary of the Invention

[0030] The idea of solution behind this invention is one of using a diode type of divider connected to an output voltage reference to be regulated and to a varying reference voltage.

[0031] Based on this idea of solution, the technical problem is solved by a high voltage regulator as previously indicated and defined in the characterising portion of Claim 1.

[0032] The problem is also solved by a method of regulating a voltage obtained from a boosted voltage as previously indicated and defined in the characterising portion of Claim 12.

[0033] The features and advantages of a high voltage regulator according to the invention will be apparent from the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawings.

Brief Description of the Drawings

[0034] In the drawings:

Figure 1 shows in schematic form a high voltage regulator including a resistive divider according to the prior art;

Figure 2 is a detail view of a detail of the regulator in Figure 1;

Figure 3 shows in schematic form a high voltage regulator including a diode divider according to the invention;

Figure 4 shows a modified embodiment of the high voltage regulator according to the invention.

Detailed Description

[0035] Referring in particular to Figure 3, generally and schematically shown at 3 is a high voltage regulator according to the invention. Corresponding circuit elements and signals, described in connection with the prior art high voltage regulator 1, will be denoted by the same alphanumerical references.

[0036] The high voltage regulator 3 is partly supplied by a boosted voltage PUMPOUT, generated by a charge pump circuit (not shown) which supplies a high voltage at a small current capacity. The high voltage regulator 3 has an input terminal IN receiving a varying reference voltage Vref_v, and an output terminal OUT delivering a regulated output voltage Vout.

[0037] The output voltage Vout is regulated by having it divided by a diode divider 4.

[0038] The diode divider 4 comprises a plurality of diodes D1, D2,..., Dn, D1', D2',..., Dn' connected between the output terminal OUT and a ground voltage reference GND. The diode divider 4 is functionally split into first 5 and second 6 legs respectively comprising first and second diode pluralities D1, D2,..., Dn and D1', D2',..., Dn' which are connected together at a central connection node Y.

[0039] The central connection node Y is connected to a non-inverting input terminal of a comparator element 2 which has an inverting input terminal connected to the input terminal IN of the high voltage regulator 1 and a supply terminal connected to a supply voltage reference Vdd, similar as the prior art high voltage regulator 1.

[0040] The comparator element 2 also has an output terminal connected to the control terminal of a drive transistor M1 which has its source terminal connected to the ground voltage reference GND and its drain terminal connected to the control terminal of an output transistor M2, itself connected between the boosted voltage reference PUMPOUT and the output terminal OUT of the high voltage regulator 3.

[0041] The high voltage regulator 3 further comprises a load transistor M3, specifically one of the PMOS type, which is connected between the boosted voltage reference PUMPOUT and the control terminal of the output transistor M2 and has its control terminal connected to the ground voltage reference GND. This load transistor M3 has an n-well terminal connected to the source terminal and, hence, to the boosted voltage reference PUMPOUT.

[0042] The regulated output voltage Vout is sampled by the resistive divider of the high voltage regulator 3 at the central connection node X. The comparator element 2 in combination with the transistors M1, M2 and M3 then provide a negative feedback of the sampled voltage Vsample.

[0043] Advantageously in this invention, the comparator element 2 basically comprises an operational amplifier or a simple differential. In either cases, this operational amplifier or simple differential is supplied by the supply voltage Vdd and, accordingly, can draw large amounts of current from the supply voltage reference Vdd, which makes it specially fast.

[0044] On the other hand, the portion which includes the drive transistor M1, output transistor M2, and load transistor M3 is supplied by the boosted voltage PUMPOUT, i.e. a higher voltage than the supply voltage Vdd.

[0045] It should be noted that the varying reference voltage Vref_v may lie anywhere between the supply voltage reference Vdd and the ground voltage reference GND.

[0046] Advantageously in this invention, the diode divider 4 may comprise a plurality of diode-configured MOS transistors, which would exhibit none of the aforementioned problems affecting the resistive dividers of conventional circuits.

[0047] This diode divider 4 may be formed of PMOS transistors, as shown in Figure 3; likewise, it could be formed of NMOS transistors or semiconductor junctions.

[0048] In all cases:

1. The diode-connected MOS transistors have a high transresistance, and limited silicon area requirements for their formation.

2. The reduced area requirement eliminates the presence of undesired parasitic capacitances, thereby enabling the divided voltage Vsample at the central connection node Y of the diode divider 4 to most promptly follow the value of the voltage to be regulated (Vout) at the output terminal OUT, thus enhancing both accuracy and speed during transient phases and attenuating overshoot and ripples of the high voltage regulator 3 as a whole.

3. The equivalent resistance of the diode divider 4 is in no way concerned with the voltages applied across it, which means that the diode divider 4 will be unaffected by parasitic effects typical of high voltages.

[0049] The value of the regulated output voltage Vout of the high voltage regulator 3 according to the invention is given as:

$$Vout = \frac{n_u + n_d}{n_d} Vref\_v \qquad (1)$$

where:

n_u, n_d are the (obviously natural) numbers of diodes included in the first 5 and second 6 legs of the diode divider 4.

[0050] If, from a given value of the varying reference voltage Vref_v, numbers (which obviously must be natural numbers) of diodes n_u, n_d included in the first 5 and second 6 legs of the diode divider 4 can be found which yield the desired value for the regulated output voltage Vout, then the varying reference voltage Vref_v can be used.

[0051] It should be noted that for the diode divider 4 to perform as expected, its diodes should be in the on state. For this to occur, a voltage drop at least equal to the diode threshold voltage VT is required across each diode.

[0052] On the contrary, if no number pair n_u, n_d of diodes exist in the first and second legs 5 and 6 of the diode divider 4 which can yield the desired value for the regulated output voltage Vout, the reference voltage

Vref_v should be changed. This does not represent a problem, since for a value of the reference voltage Vref_v lying, as already stated, between the value of the supply voltage Vdd and the ground GND, a different starting reference voltage Vref' can be derived therefrom, in a known manner by the skilled persons in the art, which lies anywhere between the supply voltage Vdd and the ground GND. A circuit adapted to provide the new starting reference voltage Vref' is simple to design and allows the same supply voltage Vdd to be used from which a large amount of current can be extracted.

[0053] Such a circuit, therefore, exhibits low current consumption of the booster circuits, is highly accurate, and shows no overshoot and ripples of the regulated voltage, which will be free of parasitic effects typical of high voltages and settle at a fast rate during the transient phases.

[0054] The single drawback of such a circuit is a waste of occupied area, especially where a new starting reference voltage Vref' with a high value is to be generated.

[0055] Figure 4 shows a modified embodiment 3' of the high voltage regulator according to the invention. In particular, this regulator 3' has the input terminal IN connected to the ground voltage reference GND and to the inverting input of the comparator element 2, itself having a non-inverting input connected to a central connection node Z of the diode divider 4.

[0056] The comparator element 2, comprising in particular an operational amplifier being supplied by the supply voltage Vdd, also has an output terminal OUT'.

[0057] In the modified embodiment of Figure 4, the diode divider 4 is connected between the varying reference voltage reference Vref_v and the output terminal OUT of the high voltage regulator. This diode divider 4 comprises first 5 and second 6 diode legs connected together at the central connection node Z.

[0058] Thus, the high voltage regulator 3' is a regulator of negative voltages. Its operation is similar to that of the high voltage regulator 3 shown in Figure 3.

[0059] In particular, the output voltage Vout to be regulated is sampled through the diode divider 4, in this case with respect to the varying reference voltage Vref_v rather than to the ground GND. The voltage value so sampled is then compared, by means of the operational amplifier 2, with the ground GND through a suitable feedback network (not shown) connected to the output terminal OUT'.

[0060] In summary, the high voltage regulator of this invention provides a regulated output voltage from a boosted voltage obtained, in particular, by means of a charge pump booster circuit, through a diode divider. In particular, the output voltage is regulated by comparison of the sampled voltage from the divider with a varying reference voltage or the ground.

Claims

1. A high voltage regulator partly supplied by a boosted voltage (PUMPOUT) and adapted to deliver a regulated output voltage (Vout) on an output terminal (OUT), starting from a sampled voltage (Vsample) obtained by dividing the regulated output voltage (Vout), which regulator comprises at least a comparator element (2) being supplied by a supply voltage (Vdd) and feedback connected to a divider (4) of said regulated output voltage (Vout), characterised in that said divider (4) is a diode divider connected between the output terminal (OUT) and a first comparison voltage reference (GND, Vref_v) and has a central connection node (Y, Z) connected to a non-inverting terminal of the comparator element (2).

2. A high voltage regulator according to Claim 1, characterised in that it further comprises an input terminal (IN), connected to a second comparison voltage reference (Vref_v, GND) and to an inverting terminal of the comparator element (2) incorporated to the high voltage regulator (3).

3. A high voltage regulator according to Claim 2, characterised in that said diode divider (4) comprises first and second legs (5, 6) of diodes (D1,D2,...,Du, D1',D2',...,Dd') connected in series with one another at said central connection node (Y, Z), said first leg (5) of diodes being connected between the output terminal (OUT) and the central connection node (Y, Z) of said divider, and said second leg (6) being connected between the central connection node (Y, Z) and the first comparison voltage reference (GND, Vref_v).

4. A high voltage regulator according to Claim 3, characterised in that the second leg (6) of diodes is connected between the central connection node (Y) and a ground voltage reference (GND), and that the input terminal (IN) of the high voltage regulator (3) is connected to a varying voltage reference (Vref_v).

5. A high voltage regulator according to Claim 1, characterised in that the comparator element (2) comprises essentially an operational amplifier or a simple differential.

6. A high voltage regulator according to Claim 5, characterised in that only said operational amplifier or simple differential included in the comparator element (2) is supplied by the supply voltage (Vdd).

7. A high voltage regulator according to Claim 1, characterised in that said comparator element (2) has an output terminal connected to the output terminal

(OUT) of the high voltage regulator (3) through a series of the drive transistor (M1), an output transistor (M2), and a load transistor (M3), said drive transistor (M1) having its control gate terminal connected to the output terminal of the operational amplifier (2), its source terminal connected to the ground voltage reference (GND), and its drain terminal connected to the control gate terminal of the output transistor (M2), said output transistor (M2) being connected between the boosted voltage reference (PUMPOUT) and the output terminal (OUT) of the high voltage regulator (3), and said load transistor (M3) being connected between the boosted voltage reference (PUMPOUT) and the control gate terminal of the output transistor (M2) and having its control gate terminal connected to the ground voltage reference (GND).

8. A high voltage regulator according to any one of the preceding claims, characterised in that the value of the varying reference voltage (Vref_v) ranges from the value of the supply voltage (Vdd) to the ground value (GND).

9. A high voltage regulator according to Claim 3, characterised in that the second leg (6) of diodes is connected between the central connection node (Z) and a varying voltage reference (Vref_v), and that the input terminal (IN) of the high voltage regulator (3) is connected to a ground voltage reference (GND).

10. A high voltage regulator according to Claim 1, characterised in that the diode divider (4) comprises a plurality of MOS transistors in diode configuration.

11. A high voltage regulator according to Claim 1, characterised in that the diode divider (4) comprises a plurality of semiconductor junctions.

12. A high voltage regulator according to any one of the preceding claims, characterised in that said boosted voltage (PUMPOUT) is generated by a booster circuit adapted to supply a high voltage at a small current capacity.

13. A method of regulating a voltage (Vout) derived from a boosted voltage (PUMPOUT), characterised in that it comprises the following steps:

- obtaining a sampled voltage (Vsample) as the voltage value at a central connection node (Y, Z) of a diode type of divider (4) connected to a reference of the voltage to be regulated (Vout) and to a first comparison voltage reference (GND, Vref_v);
- regulating said voltage (Vout) according to the comparison of said sampled voltage (Vsample) with a second comparison voltage reference (Vref_v, GND).

14. A regulating method according to Claim 13, characterised in that the comparison of said sampled voltage (Vsample) with said second comparison voltage reference (Vref_v, GND) is performed by an operational amplifier (2) being supplied a supply voltage (Vdd) and feedback connected to said divider (4), the central connection node (Y, Z) of the diode divider (4) being connected to a non-inverting terminal of the operational amplifier (2).

15. A regulating method according to Claim 14, characterised by the step of comparing the sampled voltage (Vsample) with a varying reference voltage (Vref_v) supplied to an inverting input of the operational amplifier (2), said diode divider (4) being connected to said voltage to be regulated (Vout) and to a ground voltage reference (GND).

16. A regulating method according to Claim 15, characterised in that, with said diode divider (4) comprising first and second legs (5, 6) of diodes (D1,D2,...,Du,D1',D2',...,Dd') connected in series with one another at said central connection node (Y, Z), the value of the voltage to be regulated (Vout) is obtained from the varying reference voltage (Vref_v) by the following relation:

$$Vout = \frac{n_u + n_d}{n_d} Vref\_v \qquad (1)$$

where:

n_u, n_d are the numbers of diodes included in the first and second legs (5, 6) of the diode divider (4).

17. A regulating method according to Claim 16, characterised in that, if the numbers (n_u, n_d) of diodes included in the first and second legs (5, 6) of the diode divider (4), said numbers being of necessity natural numbers, can be found from a value whichever of the varying reference voltage (Vref_v), then a desired value of the regulated voltage is obtained.

18. A regulating method according to Claim 16, characterised in that, starting from a given number (n_u, n_d) of diodes included in the first and second legs (5, 6) of the diode divider (4), the varying reference voltage (Vref_v) can be varied to obtain a desired value of the regulated voltage.

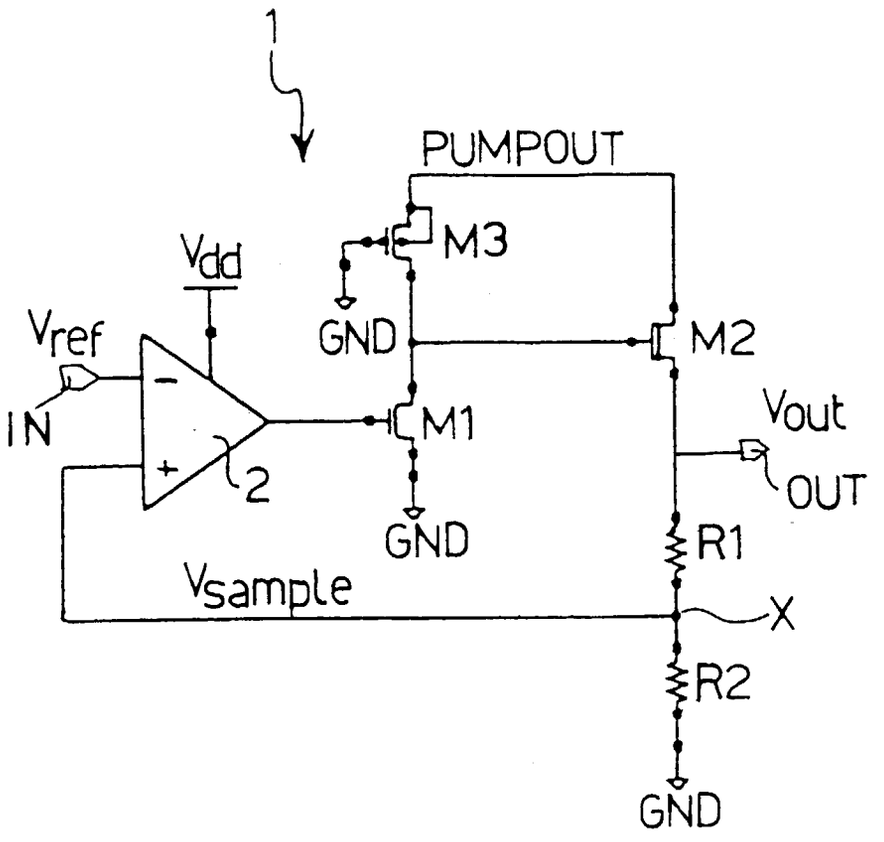

FIG. 1
PRIOR ART

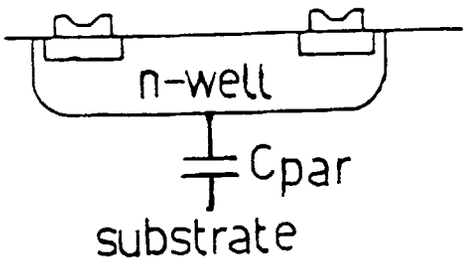

FIG. 2
PRIOR ART

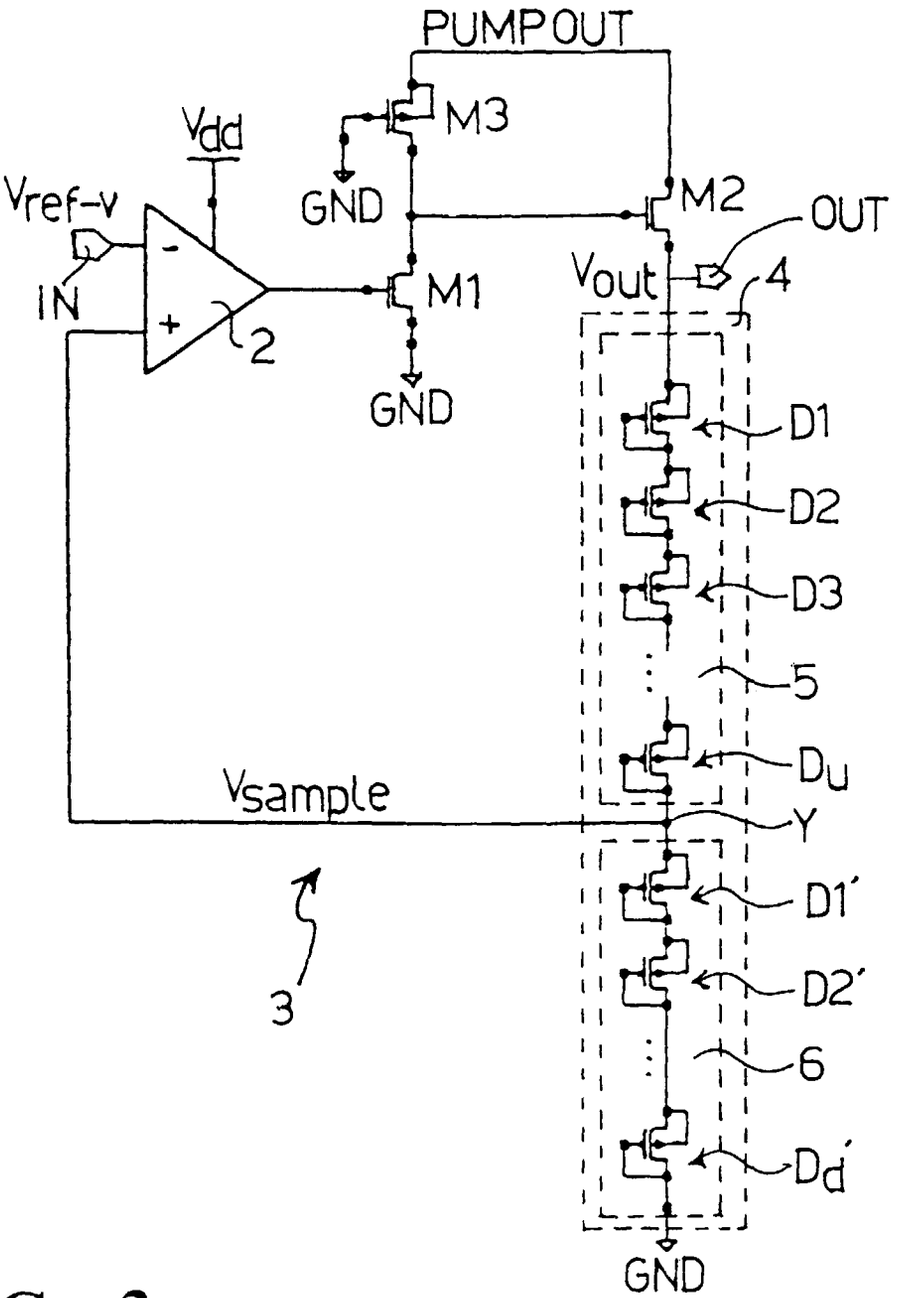
PUMPOUT
M3
Vdd
GND
M2
OUT
Vref-v
IN
M1
Vout
4
2
GND
D1
D2
D3
5
Du
Vsample
Y
D1'
D2'
3
6
Dd'
GND

FIG. 3

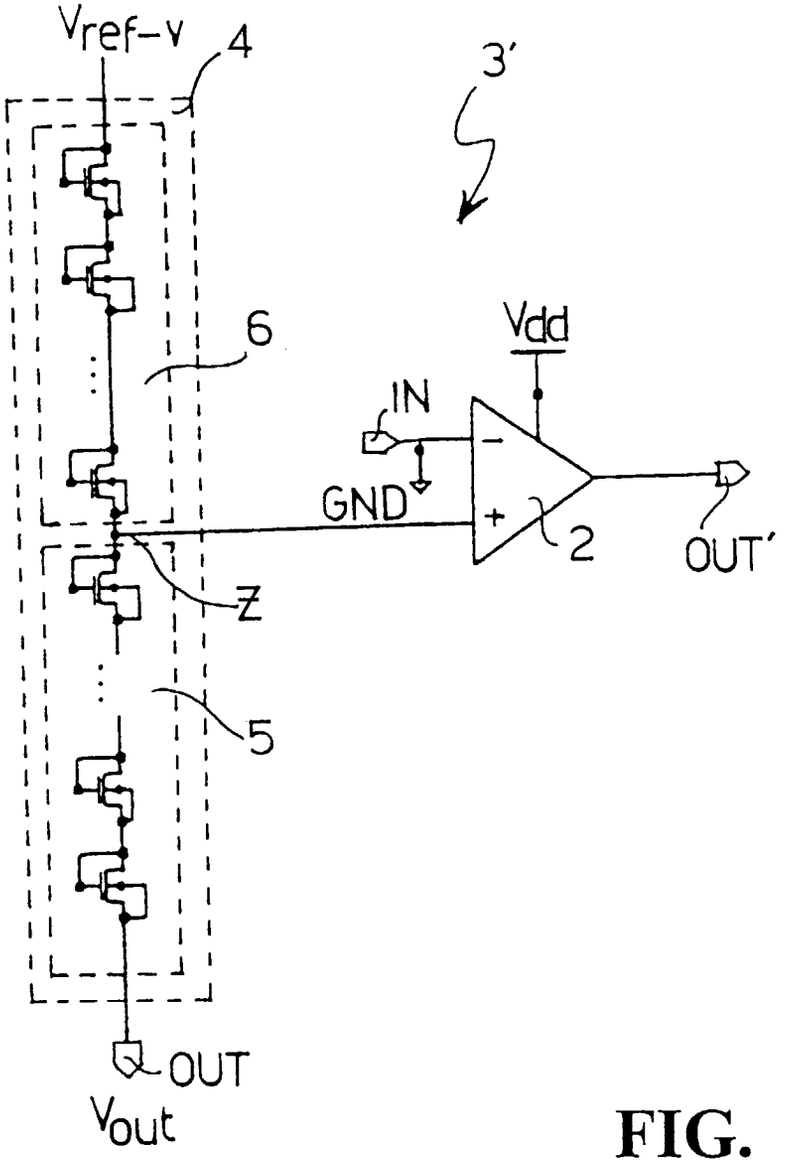

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0575

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	FR 2 681 180 A (GEMPLUS CARD INT) 12 March 1993 * page 3, line 14 - page 5, line 13 *	1,13	G05F1/00 G05F1/46
A	US 5 077 518 A (HAN GYO-JIN) 31 December 1991 * column 1, line 5 - line 47 *	1,13	
A	US 5 530 640 A (HARA MOTOKO ET AL) 25 June 1996 * the whole document * & JP 06 217 528 A (MITSUBISHI DENKI KK) 5 August 1994	1,13	
A	US 5 132 565 A (KUZUMOTO TAKATOSHI) 21 July 1992 * abstract *	1,13	
A	US 5 162 668 A (CHEN CHIH-LIANG ET AL) 10 November 1992 * abstract *	1,13	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
G05F G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 July 1998	Schobert, D

CATEGORY OF CITED DOCUMENTS

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