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(71) Applicant: **MOTOROLA, INC.**
Schaumburg, IL 60196 (US)

(72) Inventor: **Chu, On Ki Andrew**
Yuen Long, Hong Kong (HK)

(74) Representative:
Gibson, Sarah Jane et al
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
Basingstoke, Hampshire RG21 7PL (GB)

(54) Liquid crystal display controller with subframe control

(57) A DMA controller 33 retrieves pixel intensity data 60 from memory 16 and provides the pixel intensity data 60 to the frame rate controller 37. The frame rate controller 37 also receives a frame synchronising signal 32 and provides switching data 42 which is stored in a display data buffer 41, 41A, 41B and 41C in accordance with the frame synchronising signal 32 to switch pixels 45 in corresponding display frames 50, 50A, 50B and 50C to have the intensity indicated by the pixel intensity data 60.

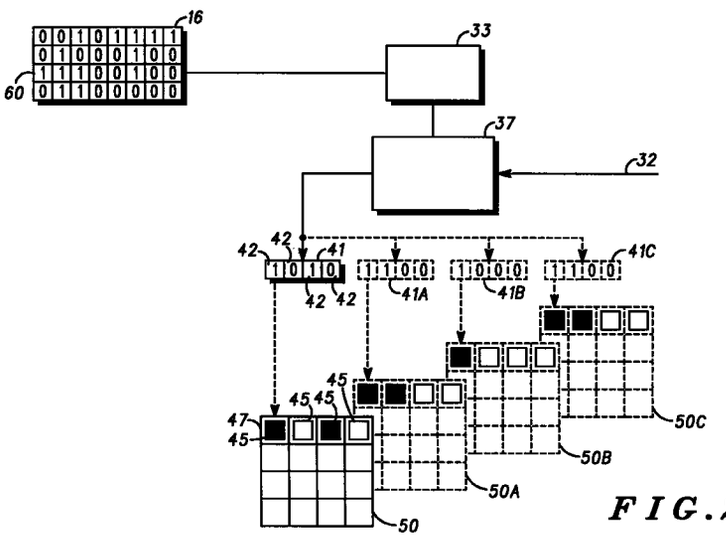

FIG. 2

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Description

Field of the Invention

[0001] This invention relates to a controller for a liquid crystal display (LCD), and in particular to a LCD controller that requires a reduced amount of memory.

Background of the Invention

[0002] A LCD has a matrix of picture elements or pixels. Each pixel can be switched to an opaque state or a clear state by application of corresponding voltage levels, and by selectively applying the voltage levels to each of the pixels, information is presented on the display.

[0003] It has been found that by varying the frequency at which a pixel is switched between the opaque and clear states, a pixel can appear to have selectable shades of "grey" between the opaque and clear states.

[0004] In a N-level grey scale display N denotes the number of different shades or levels from the opaque to the clear states. Conventionally, information indicating the grey level for each pixel is stored in a memory known as a pixel buffer which is located in the LCD controller. In a binary based system, the pixel buffer must store $\log_2 N$ bits per pixel for a display to have N grey levels. For example, when 4 grey levels are required, the pixel buffer needs to store 2 binary digits or bits per pixel, and when 16 grey levels are required, the pixel buffer stores 4 bits per pixel. Consequently, the larger the number of grey levels the larger the amount of memory required for a pixel buffer.

Brief Summary of the Invention

[0005] The present invention therefore seeks to provide a LCD controller whose memory requirement does not increase substantially in proportion to the number of grey levels to be displayed.

[0006] Accordingly, in one aspect the invention provides a display controller comprising a frame controller and a display data buffer, wherein the frame controller has: a pixel intensity data input; a synchronising input; and a switching data output, and the display data buffer has: a data input coupled to the switching data output of the frame controller; and an output.

Brief Description of the Drawings

[0007] An embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a block diagram of a LCD controller; and

FIG. 2 shows a simplified block diagram of the LCD controller in FIG. 1.

Detailed Description of the Drawings

[0008] In FIG. 1, a liquid crystal display (LCD) controller 10 receives information from a central processing unit (CPU) 12 which includes information for display on a display 25, and information on how the information for display is to be displayed. The information for display indicates which picture elements (pixels) on the display 25 of the display module 23 are to be turned ON and which are to be turned OFF, and when this information is provided to a display, the information is displayed in "black" and "white" only. When the information on how the information for display is to be displayed includes pixel intensity data that indicate the selected frequency at which each pixel is to be switched ON and OFF, the particular pixels can be displayed having selected "grey" levels or tones.

[0009] The LCD controller 10 is coupled to the CPU 12 and a memory 16 via an address bus 18 and a data bus 21. A memory controller 14 is coupled between the memory 16 and the CPU 12 to control access by the CPU 12 to the memory 16. The LCD controller 10 is also coupled to a display module 23 having the display 25 with a matrix of pixels thereon.

[0010] The LCD controller 10 includes control registers 31 that are coupled to the address bus 18 and the data bus 21, and to provide an output to a direct memory access (DMA) controller 33. The control registers 31 receive, store, and provide control information to and from the CPU 12, and the control information determines the operation of the LCD controller 10.

[0011] The DMA controller 33 is also coupled to the address bus 18 and the data bus 21, and is coupled to provide an output to a screen panning circuit 35. The DMA controller 33 controls the transfer of data from the memory 16 to the LCD controller 10. The DMA controller 33 also has an input that is coupled to receive control information from the control registers 31 that determines the operation of the DMA controller 33. The DMA controller 33 also has an input for receiving a low data signal and an input for receiving a buffer full signal. Upon receipt of the low data signal the DMA controller 33 will transfer more data from the memory 16 to the LCD controller 10, and upon receiving the buffer full signal the DMA controller 33 stops transferring data from the memory to the LCD controller 10.

[0012] The screen panning circuit 35 shifts the information displayed on the display 25 horizontally by a number of pixels, where the number of pixels is programmed in the control registers 31. The screen panning circuit 35 has an output which is coupled to a frame rate controller 37.

[0013] The frame rate controller 37 receives a frame synchronising signal (32 in FIG. 2) and information including pixel intensity data from the memory 16, and controls the switching or ON/OFF frequency of the pixels on the display 25 so that the pixels will be displayed in accordance with the pixel intensity data.

[0014] The frame rate controller 37 provides an output to a cursor logic circuit 39 which provides an output to a pixels buffer 41. The cursor logic circuit 39 adds the cursor to the information displayed on the display 25 and is implemented by overlay or logic operation of the pixels with a predefined cursor bitmap.

[0015] The pixels buffer 41 is a first-in-first-out (FIFO) structure that holds information being displayed on the display 25. The information provided from the output of the pixels buffer 41 is only the ON/OFF switching information for each of the pixels on the display 25. The number of storage locations for storing bits in the pixel buffer 41 can equal the number of pixels on the display 25. Typically, the number of storage locations in the pixel buffer 41 is less than the number of pixels on the display 25, and several transfers of pixel intensity data are made from the memory 16 to the frame rate controller 37 under the control of the DMA controller 31 to provide switching data for all the pixels on the display 25. A trade off is made based upon the amount of data traffic caused by the frequency of data transfer and the size of the pixel buffer 41.

[0016] The pixels buffer 41 has an output which that provides the low data signal and an output that provides the buffer full signal, to the DMA controller 33. The pixels buffer provides the low data signal when the switching data in the pixels buffer 41 is less than a predetermined level. For example, when the predetermined level is 2 data words for a pixels buffer having a 4 data word capacity, the pixels buffer will generate the low data signal when 2 or less data words remain in the pixels buffer. When there are 4 data words in the pixels buffer, the pixels buffer will stop transferring data from the memory 16 to the frame rate controller 37.

[0017] The output of the pixels buffer 41 is provided to a LCD interface 42 that packs the display data so that it matches control signals, data bus width and polarity of the display module 23. The LCD interface 42 converts the output of the pixels buffer 41 into a form suitable for switching pixels on the display 25, and provides the converted information to the display module 23.

[0018] In FIG. 2 the simplified block diagram will be used to describe the operation of the LCD controller 10 for a 4 level grey scale display. In a 4 level grey scale display pixels 45 on the display (25 in FIG. 1) can have one of four intensity levels. 4 complete screens of pixels, each referred to as a frame 50, 50A, 50B and 50C, are displayed sequentially in accordance with a frame synchronising signal.

[0019] The number of frames of the four frames 50, 50A, 50B and 50C in which the pixels 45 are switched ON determines the intensity of those pixels on the display (25 in FIG. 1). A pixel has the highest intensity when it is switched ON in all the four frames 50, 50A, 50B and 50C. When a pixel is switched ON in every second frame of the four frames 50, 50A, 50B and 50C, it has a lower intensity. A pixel has an even lower intensity when it is switched ON in every third frame of the four frames 50, 50A, 50B and 50C. A pixel has the lowest intensity when it is switched OFF in all of the four frames 50, 50A, 50B and 50C.

[0020] Two binary digits or bits are required to select each of the 4 intensity levels for each of the pixels 45. Hence, for a row 47 of four pixels 45, 8 bits are required, and these are stored as display intensity data 60 in the memory 16.

The eight bits constitute 4 pairs of 2 bits, where each pair is for each of the 4 pixels 45 in the top row 47 of the display (25 in FIG. 1).

[0021] The pixels buffer 41 stores one bit 42 for each pixel 45, hence, the pixel buffer 41 stores 4 bits for the 4 pixels 45 in the top row 47 of the display (25 in FIG. 1). Each bit 42 in the pixels buffer 41 represents the switching status of corresponding pixels 45 in the top row 47 of the display (25 in FIG. 1). When a bit 42 in the pixels buffer 41 is 1(binary) the corresponding pixel on the display (25 in FIG. 1) is switched ON, and when the bit 42 is 0(binary) that pixel is switched OFF.

[0022] Hence, the pixel buffer in accordance with the present invention advantageously stores only one bit for each pixel. Consequently, the total number of bits stored in the pixel buffer is equal to the number of pixels on a display, and is independent of the number of grey levels displayed.

[0023] The DMA controller 33 transfers the display intensity data 60 from the memory 16 to the frame rate controller 37 in accordance with the low data and buffer full signals received from the pixels buffer 41. At a frame synchronising frequency, provided by a frame synchronising signal 32, the frame rate controller 37 sequentially loads the pixels buffer 41 four times with display data bits 42. This is indicated by the contents of the pixels buffer 41, and the subsequent contents of the pixels buffer 41 as shown in broken lines and labelled 41A, 41B, and 41C.

[0024] The frame 50 shows the pixels 45 in the top row 47 switched in accordance with the contents of the pixel buffer 41. Corresponding frames 50A, 50B and 50C show the pixels 45 in the top row 47 switched in accordance with the subsequent contents of the pixels buffer 41 as shown in broken lines and labelled 41A, 41B, and 41C.

[0025] In operation, when the frame rate controller 37 determines that the first 2 bits of the display intensity data 60 are 11(binary) indicating the highest intensity level, it stores 1(binary) in the first bit location in the pixel buffer 41 for each of the 4 frames 50, 50A, 50B and 50C. Similarly, when the next 2 bits of the display intensity data 60 are 10 (binary) indicating the lower intensity level, the frame rate controller 37 stores 1(binary) in the second bit location in the pixel buffer 41 for each alternate frame 50A and 50C of the four frames 50, 50A, 50B and 50C.

[0026] Further, when the third set of 2 bits of the display intensity data 60 are 01(binary) indicating the even lower intensity level, the frame rate controller 37 stores

a 1(binary) in the third bit location in the pixel buffer 41 in one frame 50 of the four frames 50, 50A, 50B and 50C. In addition, when the last set of 2 bits of the display intensity data 60 are 00(binary) indicating the lowest intensity level, the frame rate controller 37 does not set the fourth bit in the pixel buffer 41 in any of the four frames 50, 50A, 50B and 50C.

[0027] Hence, the described LCD controller advantageously utilises a fixed and limited amount of memory to provide "grey" levels on a display. This is accomplished by storing only one switching data bit for each of the pixels on the display.

[0028] The present invention, as described, therefore provides a LCD controller whose memory requirements are relatively constant and substantially independent of the number of grey levels to be displayed.

Claims

1. A display controller comprising:

   a frame controller having:

   a pixel intensity data input;
   a synchronising input;
   a switching data output;

   a display data buffer having:

   a data input coupled to the switching data output of the frame controller; and
   an output.

2. A display controller in accordance with claim 1 wherein the frame controller comprises a frame controller means for receiving the pixel intensity data of at least one pixel on a display, for receiving a frame synchronising signal, and for providing switching data to switch the at least one pixel on the display.

3. A display controller in accordance with claim 2 wherein the display data buffer comprises a display data buffer means for receiving the switching data for the at least one pixel on the display and for storing the switching data therein in accordance with the frame synchronising signal.

4. A display controller in accordance with claim 2 wherein the pixel intensity data selects one of a predetermined number of pixel display intensities for the at least one pixel on the display.

5. A display controller in accordance with claim 4 wherein the predetermined number of pixel display intensities is given by 2^N when the pixel intensity data comprises N bits.

6. A display controller in accordance with claim 4 wherein the frame synchronising signal has a frequency that is proportional to the predetermined number of pixel display intensities.

7. A display controller in accordance with claim 1 further comprising a direct memory access (DMA) controller coupled to the frame controller for receiving the pixel intensity data and for providing the pixel intensity data to the frame controller.

8. A display controller in accordance with claim 6 further comprising control registers coupled to the DMA controller for receiving control information that control operation of the display controller and for providing at least some of the control information to the DMA controller to control the transfer of pixel intensity data to the frame controller.

9. A method in a liquid crystal display (LCD) controller comprising the steps of:

   a) receiving pixel intensity data for at least one pixel on a display and a frame synchronising signal;
   b) generating a sequence of switching data bits in accordance with the pixel intensity data; and
   c) storing the sequence of switching data bits in accordance with the frame synchronising signal.

10. A display controller comprising:

    a frame controller means for receiving the pixel intensity data of at least one pixel on a display and a frame synchronising signal, and for providing switching data to switch the at least one pixel on the display; and

    a display data buffer means coupled to the frame controller means for receiving the switching data for the at least one pixel on the display and for storing the switching data therein in accordance with the frame synchronising signal.

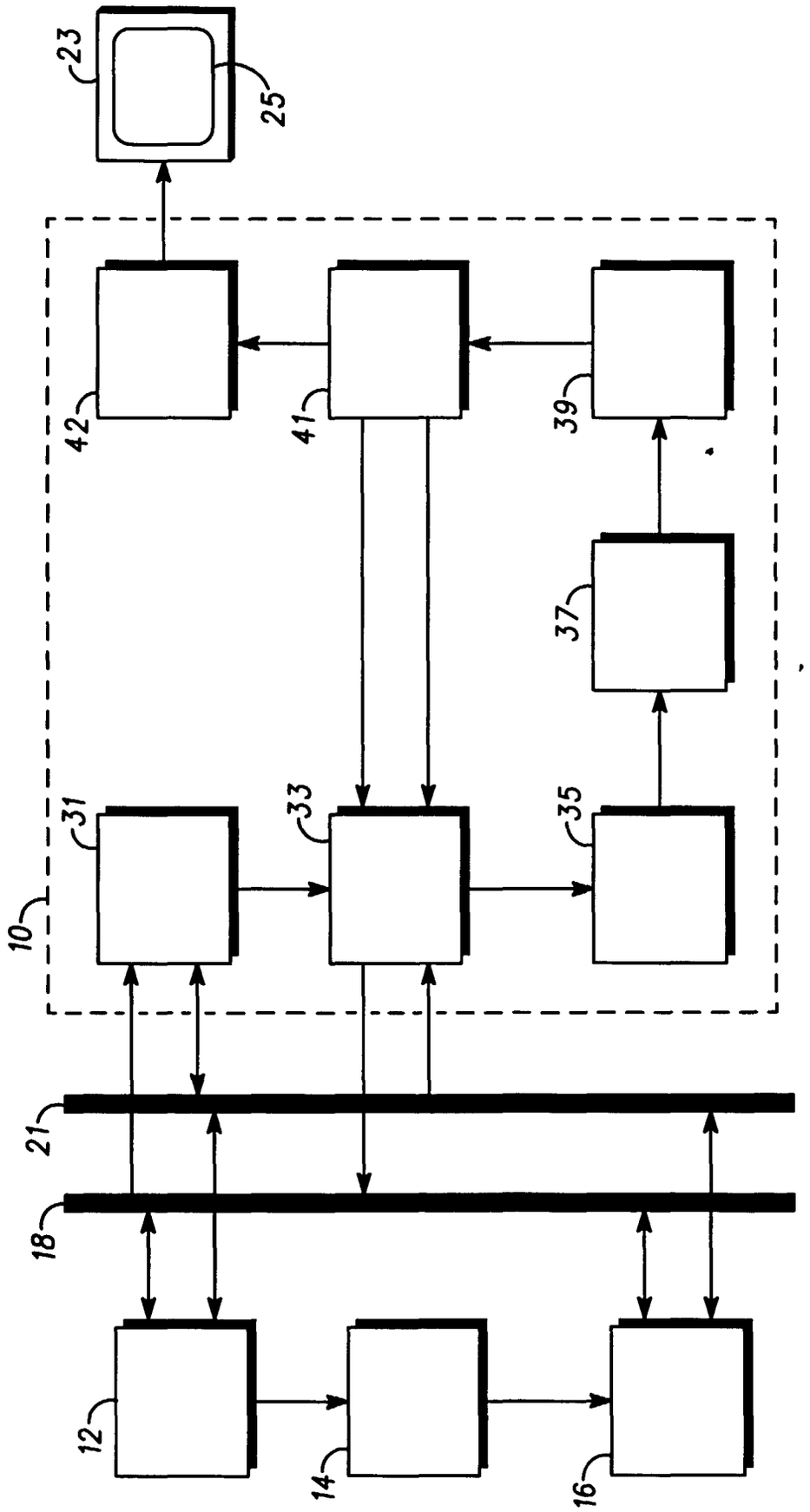

FIG.1

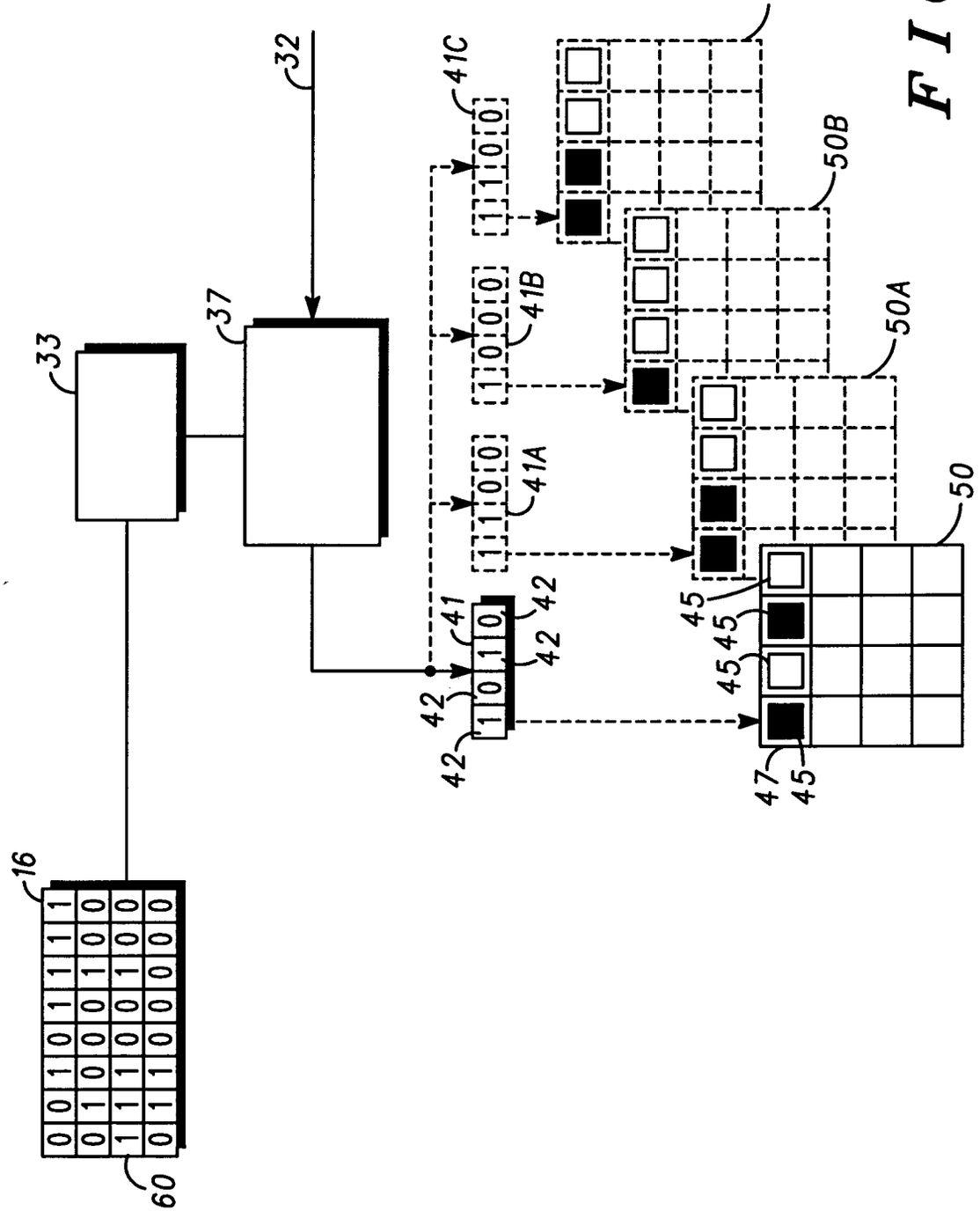

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 98 12 1762

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 April 1999	Farricella, L

CATEGORY OF CITED DOCUMENTS

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