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(54) **FABRICATION OF GATED ELECTRON-EMITTING DEVICE UTILIZING DISTRIBUTED PARTICLES TO DEFINE GATE OPENINGS**

HERSTELLUNG VON GITTERGESTEUERTER ELEKTRONEN EMITTIERENDE QUELLE MITTELS VERTEILTE TEILCHEN ZUR BESTIMMUNG DER GITTERÖFFNUNGEN

FABRICATION D'UN DISPOSITIF EMETTEUR D'ELECTRONS POURVU D'UNE GRILLE UTILISANT LA DISTRIBUTION DE PARTICULES POUR DEFINIR DES OUVERTURES DE GRILLE

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Description

FIELD OF USE

[0001] This invention relates to the fabrication of electron-emitting devices, commonly referred to as cathodes, suitable for products such as cathode-ray tube ("CRT") displays of the flat-panel type.

BACKGROUND ART

[0002] A field-emission cathode (or field emitter) emits electrons upon being subjected to an electric field of sufficient strength. The electric field is produced by applying a suitable voltage between the cathode and an electrode, typically referred to as the anode or gate electrode, situated a short distance away from the cathode.

[0003] When a field-emission cathode is utilized in a flat-panel CRT display, electron emission from the cathode occurs across a sizable area. The electron-emitting area is commonly divided into a two-dimensional array of electron-emitting portions, each situated across from a corresponding light-emitting portion to form part or all of a picture element (pixel). The electrons emitted by each electron-emitting portion strike the corresponding light-emitting portion and cause it to emit visible light.

[0004] It is generally desirable that the illumination be uniform (constant) across the area.of each light-emitting portion. One method for achieving uniform illumination is to arrange for electrons to be emitted uniformly across the area of the corresponding electron-emitting portion. This typically involves fabricating the electron-emitting portion as a large number of small, closely spaced electron-emissive elements.

[0005] Various techniques have been investigated for manufacturing electron-emitting devices that contain small, closely spaced electron-emissive elements. Spindt et al, "Research in Micron-Sized Field-Emission Tubes," IEEE Conf. Rec. 1966 Eighth Conf. Tube Techniques, 20 September 1966, pp. 143 - 147, describes how small randomly distributed spherical particles are employed to define the locations for conical electron-emissive elements in a flat field-emission cathode. The size of the spherical particles strongly controls the base diameter of the conical electron-emissive elements.

[0006] Figs. 1a - 1g (collectively "Fig. 1") illustrate the sphere-based process utilized in Spindt et al to fabricate an electron-emitting diode having a thick anode. In Fig. 1a, the starting point is sapphire substrate 20. A sandwich consisting of lower molybdenum layer 22, insulating layer 24, and upper molybdenum layer 26 is situated on substrate 20.

[0007] Polystyrene spheres 28, one of which is shown in Fig. 1b, are scattered across the top of molybdenum layer 26. "Resist" is deposited to form resist layer 30A on the uncovered part of layer 26. See Fig. 1c. Portions 30B of the resist, typically alumina (aluminum oxide), accumulate on spherical particles 28 during the resist deposition. Spheres 28 are subsequently removed, thereby removing resist portions 30B. Referring to Fig. 1d, openings 32 extend through resist layer 30A at the locations of removed spheres 28.

[0008] The exposed portions of molybdenum layer 26 are etched through resist openings 32 to form openings 34 through molybdenum 26, the remainder of which is indicated as item 26A in Fig. 1e. Similarly, the exposed parts of insulating layer 24 are etched through openings 34 to form cavities 36 through remaining insulating layer 24A. See Fig. 1f. Resist layer 30A is removed, typically during the cavity etch.

[0009] Finally, molybdenum is evaporatively deposited on top of the structure and into cavities 36. The evaporation is performed in such a way that the openings through which the molybdenum accumulates in cavities 36 progressively close. As indicated in Fig. 1g, conical molybdenum electron-emissive elements 38A are formed in cavities 36, while continuous molybdenum layer 38B is formed on top of molybdenum layer 26A. Layers 38B and 26A together form the anode for the diode.

[0010] Utilization of spherical particles to establish the locations, and base dimensions, of electron-emissive elements in Spindt et al is a creative approach to creating an electron-emitting device. However, the electrons emitted by elements 38A are collected by anode 26A/38B and thus are not utilized to directly activate light-emitting areas. It would be desirable to employ spherical particles to define the locations for small, closely spaced electron-emissive elements that emit electrons which can be'utilized to directly activate light-emissive elements in a flat-panel device in a highly uniform manner.

GENERAL DISCLOSURE OF THE INVENTION

[0011] The present invention furnishes a group of fabrication processes in which particles, typically spherical, are so employed in manufacturing gated electron-emitting devices. The particles define the locations of electron-emitting elements in the gated electron emitters. Importantly, the fabrication processes of the invention are arranged so that electrons emitted by the electron-emissive elements are available for directly activating elements such as light-emissive regions in a flat-panel device.

[0012] The surface density of the particles defines (equals) the surface density of the electron-emissive elements. The particle surface density can readily be set at a high value. Consequently, a high surface density of electron-emissive elements can easily be attained. Although the particles, and therefore the electron-emissive elements, are normally situated at locations largely random relative to one another, the number of electron-emissive elements per unit area is relatively uniform across the overall electron-emitting area.

[0013] Also, the particles can readily be chosen to have a tight size distribution--i.e., the standard deviation

in the average particle diameter is quite small. By appropriately adjusting the values for certain dimensional parameters, such as certain thicknesses, the electron-emissive elements can be made to be quite similar to one another. The net result is that utilization of particles according to the manufacturing processes of the invention enables highly uniform electron-emission to be achieved, thereby enabling light-emissive regions to be directly activated in a highly uniform manner.

[0014] In fabricating a gated electron emitter according to the invention, a multiplicity of particles are distributed over a suitable starting structure. Importantly, the magnitude of the lateral area of the starting structure typically has little effect on the ability to distribute the particles in a relatively uniform (though largely random) manner over the starting structure. Consequently, the fabrication processes of the invention can readily be used to make electron emitters of large area.

[0015] The particles are typically spherical in shape. After having been distributed over the starting structure, the particles are employed to define the locations for corresponding gate openings extending through an electrically non-insulating gate layer provided over an electrically insulating layer in the structure. As discussed below, "electrically non-insulating" means electrically conductive or electrically resistive.

[0016] The particles can be distributed over the insulating layer or over the gate layer, thereby leading to different sequences for utilizing the particles to define the gate openings. When the particles are distributed over the insulating layer, electrically non-insulating gate material is provided over the insulating layer, at least in space between the particles. The particles are then removed. During the particle removal operation, any of the gate material overlying the particles is simultaneously removed. The remaining gate material forms the gate layer through which the gate openings extend at the locations of the removed particles.

[0017] When the particles are distributed over the gate layer, further material is provided over the gate layer, at least in space between the particles. The particles are removed, thereby simultaneously removing any of the further material overlying the particles. Apertures then extend through the remaining further material at the locations of the removed particles. The gate layer is subsequentially etched through the openings in the remaining further material to form the gate openings.

[0018] A primary layer can be formed over the gate layer. The primary layer typically consists of inorganic dielectric material. If the further material is also present, the primary layer is located between the gate layer and the further material. A multiplicity of primary openings extend through the primary layer. Each gate opening is vertically aligned to a corresponding one of the primary openings. When the primary layer is employed in fabricating a gated electron emitter according to the invention, the particles can be distributed over the insulating layer, the gate layer, or the primary layer. Depending on which of these three layers receives the particles, the particles are employed to define the gate openings according to process sequences of types similar to those described in the previous two paragraphs.

[0019] A pattern-transfer layer can be provided over the insulating layer. The particles are then distributed over the pattern-transfer layer after which pedestals are created from the pattern-transfer layer by removing the portion of the pattern-transfer layer not shadowed by the particles. The gate material is deposited over the insulating layer, at least in space between the pedestals. The pedestals and any overlying material, including the particles are removed. The remaining gate material forms the gate layer through which the gate openings extend at the locations of the so-removed pedestals.

[0020] Regardless of how the particles are utilized to define the gate openings, additional processing can be performed so as to readily produce electron-emissive elements generally in the shape of filaments. For example, spacer material can be provided in the gate openings to cover the side edges of the gate openings but leave corresponding apertures extending through the spacer material down to the insulating layer. The insulating layer is subsequently etched through the apertures in the spacer material to form corresponding dielectric openings substantially through the insulating layer down to a lower non-insulating region provided below the insulating layer. Alternatively, the insulating layer can be etched through the gate openings to form dielectric openings through the insulating layer. Spacer material is then provided in the dielectric openings to substantially cover their side edges but leave corresponding apertures extending through the spacer material down to the lower non-insulating region.

[0021] Electron-emissive elements are formed over the lower non-insulating region by introducing electrically non-insulating emitter material either into the dielectric openings or into the apertures through the spacer material depending on whether the insulating layer is etched through the gate openings or through the apertures in the spacer material. As a result, the electron-emissive elements are typically shaped as filaments. The spacer material controls the lateral spacing between the gate layer and each electron-emissive element.

[0022] In a process flow that employs the primary layer mentioned above, additional processing can be performed on a structure having the primary, gate, and insulating layers so as to readily produce electron-emissive elements generally in the shape of cones. Specifically, the insulating layer can be etched through the primary and gate openings to form corresponding dielectric openings through the insulating layer down to a lower electrically non-insulating region provided below the insulating layer. Each primary opening is normally no larger than the corresponding gate opening. Consequently, the primary openings define the lateral dimensions of the (later-formed) electron-emissive elements.

By choosing the particles to have a tight size distribution as is typically the case, the size distribution of the primary openings is, to a first approximation, equally tight.

[0023] Electrically non-insulating emitter material is deposited over the primary layer, through the primary and gate openings, and into the dielectric openings to form corresponding electron-emissive elements over the lower non-insulating region. The electron-emissive elements are typically shaped as cones. Since the primary openings typically have a tight size distribution, the lateral areas occupied by the electron-emissive elements are typically largely equal. The primary layer is subsequently removed so as to lift off excess emitter material accumulated over the primary layer.

[0024] Contrary to what occurs in Spindt et al, the movement of electrons emitted by the electron-emissive elements in an electron emitter fabricated according to the invention is normally not impeded by electrically conductive material deposited over the insulating layer. The electrons can move beyond the electron emitter to activate elements, such as light-emitting phosphor regions, situated at a suitable distance above the electron emitter. In short, the invention furnishes a group of economical processes for manufacturing high-performance electron emitters that can readily be incorporated into flat-panel CRT devices, especially large-area flat-panel CRT displays.

[0025] An important feature of the invention is that the candidates for the gate material in certain of the present fabrication processes include metals through which it is difficult to accurately etch small, typically sub-micrometer openings. In particular, when the gate material is deposited over the particles, gate openings are formed at the locations of the so-deposited particles during the gate material deposition. There is no need to perform an etch to form the gate openings. Consequently, the gate material can be a difficult-to-etch metal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026]

Figs. 1a - 1g are cross-sectional structural views representing steps in a prior art process for manufacturing a diode field emitter.

Figs. 2a - 2g are cross-sectional structural views representing a set of steps in a process that follows the invention's teachings for manufacturing a gated field emitter having conical electron-emissive elements.

Figs. 3a - 3i are cross-sectional structural views representing a set of steps in another process that follows the invention's teachings for manufacturing a field emitter having conical electron-emissive elements.

Figs. 4a - 4f, 4g1, and 4g2 are cross-sectional structural views representing a set of front-end steps in a process for manufacturing a gated field emitter according to the invention. The front-end process sequence of Figs. 4a - 4f can be completed with the step of Fig. 4g1 or the step of Fig. 4g2. The field emitter can be provided with conical electron-emissive elements in accordance with the invention by applying the back-end steps of Figs. 2d - 2g, or the back-end steps of Figs. 3f - 3h, to the front-end steps of Figs. 4a - 4f and 4g1 or 4g2.

Figs. 5a - 5g are cross-sectional structural views representing a set of back-end steps by which the front-end structure of Fig. 4e, 4f, or 4gl is further processed according to the invention to produce a gated field emitter having filamentary electron-emissive elements. Alternatively, the front-end structure of Fig. 2d or 3e can be further processed in accordance with the invention by utilizing the back-end steps of Figs. 5b - 5g to produce a gated field emitter having filamentary electron-emissive elements.

Figs. 6a - 6h are cross-sectional structural views representing another set of back-end steps by which the front-end structure of Fig. 4e, 4f, or 4gl is further processed according to the invention to produce a gated field emitter having filamentary electron-emissive elements. Alternatively, the front-end structure of Fig. 2d or 3e can be further processed in accordance with the invention by utilizing the back-end steps of Figs. 6a - 6h to produce a gated field emitter having filamentary electron-emissive elements.

Figs. 7a - 7j are cross-sectional structural views representing a set of steps in a process according to the invention for manufacturing a gated field emitter having filamentary electron-emissive elements.

Figs. 8a and 8b are expanded cross-sectional structural views of portions of Figs. 7f and 7h centering around the fabrication of one of the electron-emissive elements.

Figs. 9a - 9c are expanded cross-sectional structural views representing a set of steps that can be substituted for the steps of Figs. 7h - 7j in fabricating a gated field emitter having filamentary electron-emissive elements in accordance with the invention.

Figs. 10a - 10g are cross-sectional structural views representing a set of back-end steps by which the front-end structure are Fig. 3f (or 3e) is further processed according to the invention to produce a gated field emitter having filamentary electron-emissive elements. Alternatively, the front-end structure of Fig. 2d (or 2c), 4g1 or 4g2 can be further processed in accordance with the invention by utilizing the back-end steps of Figs. 10a - 10g to produce a gated field emitter having filamentary electron-emissive elements.

Figs. 11a - 11h are cross-sectional structural views representing a set of steps in another process according to the invention for manufacturing a gated

field emitter having filamentary electron-emissive elements.

Figs. 12a - 12i are cross-sectional structural views representing a set of steps in a further process according to the invention for manufacturing a gated field emitter having filamentary electron-emissive elements.

Figs. 13a - 13g are cross-sectional structural views representing a set of front-end steps in a process for manufacturing a gated field emitter according to the invention. The front-end process sequence of Figs. 13a - 13g can, for example, be completed according to the back-end process sequence of Figs. 7e - 7j.

Fig. 14 is a cross-sectional structural view illustrating how the initial structure of Fig. 2a, 3a, 4a, 7a, or 12a appears when the lower non-insulating region consists of an electrically resistive portion and an electrically conductive portion.

Figs. 15.1 and 15.2 are cross-sectional structural views illustrating how the final field-emission structures of Figs. 2g and 5g appear when the lower non-insulating region consists of an electrically resistive portion and an electrically conductive portion.

Fig. 16 is a cross-sectional structural view of a flat-panel CRT display that incorporates a gated field emitter, such as that of Fig. 5g, fabricated according to the invention.

[0027] Like reference symbols are employed in the drawings and in the description of the preferred embodiments to represent the same, or very similar, item or items.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

General Considerations

[0028] The present invention utilizes particles distributed across a surface of a structure to define openings in a gate electrode for a gated field-emission cathode. Each field emitter fabricated according to the invention is suitable for exciting phosphor regions on a faceplate in a cathode-ray tube of a flat-panel device such as a flat-panel television or a flat-panel video monitor for a personal computer, a lap-top computer, or a workstation.

[0029] The invention furnishes a variety of different ways to utilize the particles, typically spherical, in defining the gate openings. The invention also furnishes a variety of ways for using the so-defined gate openings to produce electron-emissive elements of various shapes such as cones and filaments. Each electron-emissive element emits electrons through a corresponding one of the gate openings. Inasmuch as the particles define the locations of the gate openings, the particles also define the locations of the electron-emissive elements.

[0030] In some examples, the particles can be employed according to any one of several front-end process sequences to define gate openings in a partially finished structure that can be completed according to any one of several back-end process sequences to produce a gated field-emission cathode. The partially finished structure can often be used in creating either conical electron-emissive elements or filamentary electron-emissive elements. The invention thereby furnishes a mix-and-match capability in which any one of several front-end fabrication sequences can be combined with any one of several back-end fabrication sequences to create an efficient overall field-emitter manufacturing process that yields field emitters tailored to specific needs and particular choices of materials.

[0031] In the following description, the term "electrically insulating" (or "dielectric") generally applies to materials having a resistivity greater than 10^{10} ohm-cm. The term "electrically non-insulating" thus refers to materials having a resistivity below 10^{10} ohm-cm. Electrically non-insulating materials are divided into (a) electrically conductive materials for which the resistivity is less than 1 ohm-cm and (b) electrically resistive materials for which the resistivity is in the range of 1 ohm-cm to 10^{10} ohm-cm. These categories are determined at an electric field of no more than 1 volt/μm.

[0032] Examples of electrically conductive materials (or electrical conductors) are metals, metal-semiconductor compounds (such as metal silicides), and metal-semiconductor eutectics. Electrically conductive materials also include semiconductors doped (n-type or p-type) to a moderate or high level. Electrically resistive materials include intrinsic and lightly doped (n-type or p-type) semiconductors. Further examples of electrically resistive materials are (a) metal-insulator composites, such as cermet (ceramic with embedded metal particles), (b) forms of carbon such as graphite, amorphous carbon, and modified (e.g., doped or laser-modified) diamond, (c) and certain silicon-carbon compounds such as silicon-carbon-nitrogen.

[0033] Except as otherwise indicated, the following applies to anisotropic etches performed in the fabrication processes of the invention. All anisotropic etches are largely unidirectional and occur at the result of movement of ions in a direction substantially perpendicular to the upper surface of the emitter/gate interelectrode dielectric layer. Consequently, substantially no undercutting occurs during an anisotropic etch. All anisotropic etches are dry etches performed, for example, with a plasma or according to reactive-ion etching.

Fabrication of Field Emitters with Electron-Emissive Cones

[0034] Referring to the drawings, Figs. 2a - 2g (collectively "Fig. 2") illustrate a process for manufacturing a gated field-emission cathode utilizing spherical parti-

cles to define gate openings for conical electron-emissive elements according to the teachings of the invention. In the fabrication process of Fig. 2, the starting point is an electrically insulating substrate 40 typically formed with ceramic or glass. See Fig. 2a. Substrate 40, which provides support for the field emitter, is configured as a plate. In a flat-panel CRT display, substrate 40 constitutes at least part of the backplate.

[0035] A lower electrically non-insulating emitter region 42 lies along the top of substrate 40. Lower non-insulating region 42 may be configured in various ways. At least part of non-insulating region 42 is typically patterned into a group of generally parallel emitter-electrode lines referred to as row electrodes. When non-insulating region 42 is configured in this way, the final field-emission cathode is particularly suitable for exciting light-emitting phosphor elements in a flat-panel CRT display. Nonetheless, non-insulating region 42 can be arranged in other patterns, or can even be unpatterned.

[0036] A largely homogenous electrically insulating layer 44 is provided on top of the structure. Insulating layer 44 typically consists of silicon oxide. Alternatively, layer 44 could be formed with silicon nitride. Although not shown in Fig. 2a, portions of the lower surface of insulating layer 44 may contact substrate 40 depending on the configuration of lower non-insulating region 42. Part of insulating layer 44 later becomes the emitter/gate interelectrode dielectric.

[0037] The thickness of insulating layer 44 should be sufficiently great that the later-created electron-emissive elements are shaped as cones whose tips extend slightly above the top of layer 44. The height of each electron-emissive cone depends on its base diameter which, as described below, is determined by the diameter of a spherical particle used in defining a gate opening for that electron-emissive cone. The thickness of insulating layer 44 is normally 1 - 2 times the diameter of the spherical particles. A typical range for the insulating layer thickness is 0.1 - 3 μm.

[0038] Solid spherical particles 46 are distributed in a random, or largely random, manner across the top of insulating layer 44 as shown in Fig. 2b. Spherical particles 46 typically consist of polystyrene. Alternative materials for particles 46 include glass (e.g., silicon oxide), polymers (e.g., latex) other than polystyrene, and polymers coated with functional groups such as alcohol, acid, amide, and sulfonate groups.

[0039] When particles 46 consist of polystyrene, they have an average diameter in the range of 0.1 - 3 μm, typically 0.3 μm. The standard deviation in the average particle diameter is normally very small, less than 10%, typically 2%. The average surface density of particles 46 across insulating layer 44 is in the range of 10^6 - 10^{10} particles/cm^2, preferably 10^7 - 10^9 particles/cm^2. A typical value is 10^8 particles/cm^2. The average spacing between particles 46 is typically 2 - 3 times the average particle diameter. For 0.3-μm particles at 10^8 particles/cm^2, the average spacing is on the order of 0.6 - 0.9 μm.

[0040] Spherical particles 46 adhere quite strongly to insulating layer 44. Van der Waals forces are believed to at least partially provide the adherence mechanism. Part or all of spheres 46 may be charged--e.g., negatively when spheres 46 consist of polystyrene. In the polystyrene case, each sphere 46 typically bears at least one double negative charge, each double negative charge arising from the attachment of a carboxyl group to that sphere 46. A charge of opposite polarity on initial structure 40/42/44 may assist the adherence mechanism. In any case, once attached to insulating layer 44, particles 46 do not move readily across the top of layer 44.

[0041] Various techniques may be used to distribute spherical particles 46 across insulating layer 44. In one technique, de-ionized water containing suitably small polystyrene spheres is first combined with a reagent-grade alcohol in a beaker. The alcohol is typically isopropanol. Ethanol is an alternative candidate for the alcohol.

[0042] In the isopropanol case, the liquid in the resultant isopropanol/water solution is primarily isopropanol, typically over 99% isopropanol by volume. The polystyrene spheres are suspended in the isopropanol/water solution. Nitrogen is bubbled through the solution to make the distribution of spheres more uniform throughout the solution. Alternatively, the solution can be subjected to ultrasonic agitation to improve the uniformity of the spheres throughout the solution.

[0043] With initial structure 40/42/44 being manufactured in the form of a generally circular wafer, the wafer is placed in a spin chamber. While the wafer is in the chamber, a controlled amount of the isopropanol/water solution, including the suspended polystyrene spheres, is deposited on top of the wafer so as to cover a selected portion of the upper wafer surface but not run off the top of the wafer. The wafer is then spun for a short time to remove most of the solution. The spinning speed is 200 - 2000 rpm, typically 750 rpm. The spinning time is 5 - 120 sec., typically 20 sec.

[0044] During the spin, substantially all of the remaining isopropanol/water solution evaporates, leaving polystyrene spheres 46 behind. If any of the isopropanol/water solution remains, the wafer is dried to remove the remaining isopropanol/water. The drying operation can, for example, be done with a nitrogen jet. Regardless of whether a drying operation is, or is not, performed, the wafer is subsequently removed from the spin chamber. In this way, the structure of Fig. 2b is produced.

[0045] Electrically non-insulating gate material is deposited on insulating layer 44 and spherical particles 46. The gate material deposition is normally performed in a direction substantially perpendicular to the upper surface of layer 44 using a technique such as evaporation or collimated sputtering. The gate material accumulates on layer 44 in space between particles 46 to form an electrically non-insulating gate layer 48A of relatively uniform thickness. See Fig. 2c. Portions 48B of the gate

material accumulate simultaneously on the upper halves (hemispheres) of particles 46. The gate material is usually a metal such as chromium, nickel, molybdenum, titanium, tungsten, or gold.

[0046] A suitably etchable material, referred to here as the primary material, is deposited on gate layer 48A and gate material portions 48B. As with the gate material deposition, the primary material deposition is normally conducted in a direction substantially perpendicular to the upper surface of interelectrode dielectric layer 44, again using a technique such as evaporation or collimated sputtering. The primary material accumulates on gate layer 48A in space between spherical particles 46 to form a primary layer 50A of relatively uniform thickness as shown in Fig. 2c. Portions 50B of the primary material accumulate simultaneously on gate material portions 48B situated on spheres 46. To avoid having primary material portions 50B bridge to primary layer 50A, the total thickness of gate layer 48A and primary layer 50A is normally less than the average radius of spheres 46.

[0047] The primary material typically consists of inorganic dielectric material such as silicon nitride, aluminum oxide, or/and silicon oxide. Primary layer 50A is later employed as a lift-off layer in the process of Fig. 2 and in certain process variations described below. In certain other process variations described below, layer 50A does not perform a lift-off function. When layer 50A serves as a lift-off layer, the primary material could alternatively be a metal such as aluminum, tungsten, or gold. The primary material could also be a metal dielectric composite or a salt such as magnesium fluoride, magnesium chloride, or sodium chloride when layer 50A functions as a lift-off layer.

[0048] Spherical particles 46 are now removed. During the removal of particles 46, gate material portions 48B and primary material portions 50B are simultaneously removed to produce the structure shown in Fig. 2d. Primary openings 52 extend through primary layer 50A at the locations of removed particles 46. Gate openings 54 similarly extend through gate layer 48A at the locations of removed particles 46. In this way, particles 46 directly define the locations of both primary openings 52 and gate openings 54. Because the formation of gate openings 54 occurs during the deposition of the gate material over particles 46 and is not accomplished by etching the gate material, the candidates for the gate material include gold through which it is difficult to accurately etch small openings--i.e., openings whose diameters are typically less than 1 μm--that later expose the electron-emissive cones. The same applies to the primary material in the process of Fig. 2.

[0049] Each gate opening 54 is vertically centered on, and therefore vertically aligned to, corresponding primary opening 52. Since removed particles 46 are spherical, primary openings 52 are largely circular. For the case in which the depositions to form layers 48A and 50A were performed substantially perpendicular to the upper surface of insulating layer 44, the diameters of each pair of corresponding openings 50 and 52 are approximately the same and thus are approximately equal to the diameter of corresponding removed sphere 46.

[0050] A mechanical process is typically used to remove spherical particles 46. For example, particles 46 can be removed by an ultrasonic/megasonic operation. Most of spheres 46 are removed during the ultrasonic part of the removal operation. The ultrasonic operation is typically performed by placing the wafer in a bath of de-ionized water with a small volume percentage (e.g., 1%) of Valtron SP2200 alkoline detergent (2-butylxyethanol and non-ionic surfactant) and subjecting the bath to an ultrasonic frequency. The megasonic operation, which is normally performed after the ultrasonic operation and which removes the remainder of spheres 46, typically entails placing the wafer in another bath of de-ionized water with a small weight percentage (e.g., 0.5%) of Valtron 2200 alkaline detergent and subjecting the bath to a megasonic frequency.

[0051] A detergent which largely neutralizes the charges on particles 46 can be used in place of Valtron 2200 detergent during both the megasonic and ultrasonic operations. The charge-neutralizing detergent typically includes ionic surfactant. A high-pressure water jet could alternatively be used to remove spheres 46.

[0052] Using primary layer 50A as an etch mask, insulating layer 44 is etched through primary openings 52 and gate openings 54 to form corresponding dielectric openings (or dielectric open spaces) 56 through layer 44 down to lower non-insulating emitter region 42. See Fig. 2e in which item 44A is the remainder of insulating layer 44. While, primary layer 50A may be slightly attacked by the etchant used to form dielectric openings 56, the amount of attack is normally not enough to significantly affect the sizes or shapes of primary openings 52. Consequently, each primary opening 52 remains substantially circular even if it is of slightly different diameter than corresponding gate opening 54.

[0053] The interelectrode dielectric etch to create dielectric open spaces 56 is normally performed in such a manner that dielectric openings 56 undercut gate layer 48A somewhat. The amount of undercutting is chosen to be sufficient to avoid having the later-deposited emitter cone material accumulate on the sidewalls (or side edges) of dielectric openings 56 and provide electrical leakage paths between the electron-emissive elements and gate layer 48A.

[0054] The interelectrode dielectric etch can be performed in various ways such as: (a) an isotropic wet etch using one or more chemical etchants, (b) an undercutting (and thus not fully anisotropic) dry etch, and (c) a non-undercutting (fully anisotropic) dry etch followed by an undercutting etch, wet or dry. When insulating layer 44 and primary layer 50A respectively consist of silicon oxide and silicon nitride, the etch is preferably done in two stages. An anisotropic plasma etch is performed with carbon tetrafluoride to create vertical openings sub-

stantially through insulating layer 44 after which an isotropic wet etch is performed with buffered hydrofluoric acid to widen the initial openings and form dielectric openings 56.

[0055] Electrically non-insulating emitter cone material is evaporatively deposited on top of the structure in a direction generally perpendicular to the upper surface of insulating layer 44A. The emitter cone material accumulates on primary layer 50A and passes through gate openings 54 to accumulate on lower non-insulating region 42 in dielectric open spaces 56. Due to the accumulation of the cone material on primary layer 50A, the openings through which the cone material enters open spaces 56 progressively close. The deposition is performed until these openings fully close. As a result, the cone material accumulates in dielectric open spaces 56 to form corresponding conical electron-emissive elements 58A as shown in Fig. 2f. A continuous layer 58B of the cone material is simultaneously formed on primary layer 50A. The cone material is normally a metal such as molybdenum, nickel, chromium, or niobium, or a refractory metal carbide such as titanium carbide.

[0056] Primary layer 50A is now removed with a suitable etchant. During the removal of layer 50A, excess cone material layer 58B is simultaneously lifted off. Fig. 2g shows the resultant electron emitter. Since the cone material deposition was performed generally perpendicular to insulating layer 44A, each electron-emissive cone 58A is vertically centered on corresponding primary opening 52 and also on corresponding gate opening 54.

[0057] Gate layer 48A may be patterned into a group of gate lines running perpendicular to the emitter row electrodes of lower non-insulating region 42. The gate lines then serve as column electrodes. With suitable patterning being applied to gate layer 48A, the field emitter of Fig. 2g may alternatively be provided with separate column electrodes that contact portions of gate layer 48A and run perpendicular to the row electrodes. This gate patterning and, when included, separate column-electrode formation are typically done before etching insulating layer 44 to form dielectric openings 56 but can be done at a later stage in the process.

[0058] Instead of defining the gate openings with spherical particles 46 distributed across the top of insulating layer 44, the gate openings can be defined by spherical particles distributed across the gate layer. Doing so helps to alleviate the above-mentioned constraint imposed by the particle diameter on the gate layer thickness.

[0059] Figs. 3a-3i (collectively "Fig. 3") present an example of a process in which spherical particles are so utilized in accordance with the invention to produce a gated field-emission cathode having conical electron-emissive elements. In the process of Fig. 3, an initial structure consisting of substrate 40, lower non-insulating region 42, and insulating layer 44 is formed in substantially the same way as in the process of Fig. 2. Fig. 3a, which repeats Fig. 2a, illustrates initial structure 40/42/44 for the process of Fig. 3.

[0060] Electrically non-insulating gate material is deposited on insulating layer 44 to form an electrically non-insulating gate layer 60 of relatively uniform thickness. See Fig. 3b. The gate material in the process of Fig. 3 is usually a metal such as chromium, nickel, molybdenum, titanium, or tungsten. The gate metal deposition can be performed according to any of a number of deposition techniques such as evaporation, sputtering, and chemical vapor deposition ("CVD"). In contrast to the process of Fig. 2, the gate material deposition in the process of Fig. 3 need not be performed substantially perpendicular to the upper surface of interelectrode dielectric layer 44. For the reasons discussed below, at a given sphere diameter, gate layer 60 in the process of Fig. 3 can be thicker than the maximum tolerable thickness of gate layer 48A in the process of Fig. 2.

[0061] Solid spherical particles 46 are distributed across the top of gate layer 60 as shown in Fig. 3c. Spherical particles 46 again typically consist of polystyrene. The particle distribution step is typically performed in the same way as in the process of Fig. 2. The distribution of particles 46 is random, or largely random, across the top of gate layer 60. Spheres 46 in the process of Fig. 3 normally have the same characteristics, including average diameter and standard deviation in average diameter, as in the process of Fig. 2.

[0062] A suitably etchable material, again referred to as the primary material, is deposited on gate layer 60 and spherical particles 46. The primary material deposition in the process of Fig. 3 is performed in a direction substantially perpendicular to the upper surface of interelectrode dielectric 44 using a technique such as evaporation or collimated sputtering. Similar to the method of Fig. 2, the primary material in the method of Fig. 3 accumulates on gate layer 60 in space between particles 46 to form a primary layer 62A of relatively uniform thickness. See Fig. 3d. Primary layer 62A later serves as a lift-off layer in the process of Fig. 3. Portions 62B of the primary material accumulate simultaneously on the upper halves of spheres 46.

[0063] As in the process of Fig. 2, the primary material here typically consists of inorganic dielectric material such as silicon nitride, aluminum oxide, or/and silicon oxide. Likewise, when primary layer 62A performs a lift-off function, the primary material can be (a) a metal such as aluminum, (b) a metal/dielectric composite, or (c) a salt such as magnesium fluoride, magnesium chloride, or sodium chloride.

[0064] To avoid having primary material portions 62B bridge to primary layer 62A, the thickness of primary layer 62A is normally less than the average radius of spheres 46. Compared to the process of Fig. 2 where the total combined thickness of gate layer 48A and primary layer 50A normally must be less than the average radius of spheres 46 in order to avoid undesired bridging, the avoidance of undesired bridging places less

constraint on the gate layer thickness in the process of Fig. 3 than in the process of Fig. 2. This is especially true when the etch selectively of gate layer 60 to primary layer 62A is high (i.e., layer 60 is etched much more than layer 62A) during the below-described etch to form gate openings through layer 60 using layer 62A as an etch mask. For a given sphere diameter, gate layer 60 can therefore be thicker than gate layer 48A.

[0065] In fact, gate layer 60 in the process of Fig. 3 can be considerably thicker than gate layer 48A in the process of Fig. 2. For example, the thickness of gate layer 60A can exceed the average radius, and even the average diameter, of spheres 46. As a comparative examination of the full manufacturing processes of Figs. 2 and 3 indicates, the method of Fig. 3 requires slightly more processing than the method of Fig. 2. In short, compared to the method of Fig. 2, the method of Fig. 3 significantly alleviates a constraint on the gate layer thickness in exchange for a slight amount of additional fabrication processing.

[0066] Returning to the process of Fig. 3, spherical particles 46 are now removed, typically in the same way as in the process of Fig. 2. During the sphere removal, primary material portions 62B are simultaneously removed to produce the structure of Fig. 3e. Primary openings 64 extend through primary layer 62A at the locations of removed particles 46. Since particles 46 are spherical, primary openings 64 are largely circular. Also, the diameter of each primary opening 64 is approximately the same as the diameter of corresponding removed sphere 46.

[0067] Using primary layer 62A as an etch mask, gate layer 60 is etched through primary opening 64 to form corresponding gate openings 66 through gate layer 60 down to insulating layer 44. See Fig. 3f. Item 60A is the remainder of gate layer 60.

[0068] The etch to create gate openings 66 may be performed anisotropically. The diameter of each gate opening 66 is then approximately the same as the diameter of the corresponding primary opening 64. Alternatively, the gate opening etch may be performed in such a manner that gate openings 66 undercut primary layer 62A sufficiently to avoid having the later-deposited emitter cone material accumulate on the side edges of gate layer 60A along openings 66. Fig. 3f illustrates the undercutting example in which the diameter of each gate opening 66 is greater than the diameter of corresponding primary opening 64.

[0069] Regardless of how the gate opening etch is performed, each gate opening 66 is vertically centered on, and therefore vertically aligned to, corresponding primary opening 64. Since primary openings 64 are situated at the locations of removed spheres 46, particles 46 define the locations of gate openings 66 as well as primary openings 64. Because primary openings 64 are circular, gate openings 66 are also largely circular.

[0070] The process of Fig. 3 is now completed in largely the same way as the process of Fig. 2. Using primary layer 62A as an etch mask, insulating layer 44 is etched through openings 64 and 66 to form corresponding dielectric openings (or dielectric open spaces) 68 through layer 44 down to lower non-insulating region 42. See Fig. 3g in which item 44B is the remainder of insulating layer 44. Dielectric open spaces 68 undercut layers 60A and 62A sufficiently to avoid having the later-deposited emitter cone material accumulate on the sidewalls of dielectric openings 68 and short the electron-emissive elements to gate layer 60A. The etch to create dielectric openings 68 may be performed in any of the ways described above for the interelectrode dielectric etch in the process of Fig. 2.

[0071] Electrically non-insulating emitter cone material is evaporatively deposited on top of the structure in a direction generally perpendicular to the upper surface of insulating layer 44B. The emitter cone material again normally is a metal such as molybdenum, nickel, chromium, or niobium, or a refractory metal carbide such as titanium carbide.

[0072] The cone material accumulates on primary layer 62A and passes through openings 64 and 66 to accumulate on lower non-insulating region 42 in dielectric open spaces 68. Similar to the process of Fig. 2, the openings through which the cone material enters open spaces 68 progressively close during the course of the cone material deposition. The deposition is likewise performed until these openings fully close. As a result, the cone material accumulates in open spaces 68 to form corresponding conical electron-emissive elements 70A as shown in Fig. 3h. A continuous layer 70B of the cone material is formed on primary layer 60A at the same time.

[0073] Primary layer 62A is removed. During its removal, excess cone material layer 70B is lifted off. The resultant electron emitter is depicted in Fig. 3i. In light of the fact that the cone material deposition was performed generally perpendicular to insulating layer 44B, each conical electron-emissive element 70A is vertically centered on corresponding primary opening 64 and also on corresponding gate opening 66.

[0074] Patterning of gate layer 60A into column electrodes running perpendicular to the emitter row electrodes of lower non-insulating region 42 may be done in the same way that gate layer 48A is patterned in the method of Fig. 2. Likewise, with suitable patterning being applied to gate layer 60A, the field emitter of Fig. 3i may alternatively be provided with separate column electrodes that contact portions of gate layer 60A and run perpendicular to the row electrodes.

[0075] As an alternative to the processes of Figs. 2 and 3, the gate openings can be defined by spherical particles distributed across a layer, again referred to as the primary layer, formed over the gate layer. In this case, the constraint imposed by the sphere diameter on the thickness of the primary layer is substantially lessened, along with the thickness constraint imposed by the sphere diameter on the thickness of the gate layer.

[0076] Figs. 4a - 4f and either Fig. 4g1 or Fig. 4g2 (collectively "Fig. 4") illustrate the front-end portion of a process for manufacturing a gated field-emission cathode in which spherical particles deposited on such a primary layer are utilized in defining gate openings according to the invention. To furnish the field emitter with conical electron-emissive elements, the process of Fig. 4 can be completed in accordance with the invention by following either the back-end steps of Figs. 2d - 2g or the back-end steps of Figs. 3f - 3i.

[0077] In the process of Fig. 4, an initial structure consisting of substrate 40, lower non-insulating region 42, and insulating layer 44 is formed substantially in the manner described above. See Fig. 4a which repeats Fig. 2a.

[0078] Referring to Fig. 4b, electrically non-insulating gate layer 60 is formed on insulating layer 44 according to any of the deposition techniques described above for the method of Fig. 3. For a given sphere diameter, gate layer 60 here can again be thicker than gate layer 48A in the method of Fig. 2. Likewise, gate layer 60 here is usually a metal such as chromium, nickel, molybdenum, titanium, or tungsten.

[0079] A suitably etchable material referred to as the primary material is deposited on gate layer 60 to form a primary layer 72 of relatively uniform thickness. When the front-end process sequence of Fig. 4 is combined with the back-end steps of Figs. 2d - 2g or 3f - 3i, primary layer 72 is later utilized as a lift-off layer. Candidates for the primary material here consist of the primary material candidates given above for the process of Fig. 3.

[0080] The primary material deposition in the front-end sequence of Fig..4 can be performed in various ways such as sputtering, evaporation, CVD, electrochemical deposition (provided that primary layer 72 is electrochemically depositable), spinning, and screen printing. In contrast to the processes of Figs. 2 and 3, the primary material deposition in the process of Fig. 4 need not be performed in a direction substantially perpendicular to the upper surface of insulating layer 44. For the reasons discussed below, at a given sphere diameter, primary layer 72 can be thicker than either of primary layers 50A and 62A in the methods of Figs. 2 and 3. This is especially beneficial when, for example, increased primary layer thickness is needed to cover bumps in gate layer 60 caused by factors such as bumps in insulating layer 44.

[0081] Solid spherical particles 46 are distributed across the top of primary layer 72 as shown in Fig. 4c. The particle distribution step is typically performed in the manner described above. The distribution of spheres 46 is thus random, or largely random, across the top of primary layer 72. Particles 46 typically consist of polystyrene and have the other characteristics described above.

[0082] Suitably etchable further material is deposited on primary layer 72 and spherical particles 46. The deposition of the further material is performed in a direction substantially perpendicular to the upper surface of insulating layer 44 using a technique such as evaporation or collimated sputtering. The further material accumulates in space between particles 46 to form a further layer 74A. See Fig. 4d. Portions 74B of the further material accumulate simultaneously on the upper halves of spheres 46.

[0083] To prevent further material portions 74B from bridging to further layer 74A, the thickness of further layer 74A is normally less than the average sphere radius. However, the avoidance of undesired bridging along the surfaces of spheres 46 places less constraint on the primary layer thickness in the process sequence of Fig. 4 than in the processes of Figs. 2 and 3. This is particularly true when the etch selectivity of primary layer 72 to further layer 74A is high (i.e., layer 72 is etched much more than layer 74A) during the etch described below to form primary openings through layer 72 using further layer 74A as an etch mask. For a given sphere diameter, primary layer 72 thus can be thicker than primary layer 50A in the process of Fig. 2 or primary layer 62A in the process of Fig. 3. Similarly, the necessity to avoid such undesired bridging constrains the gate layer thickness less in the process sequence of Fig. 4 than in the process of Fig. 2 or 3.

[0084] When the front-end process sequence of Fig. 4 is completed by the back-end steps of Figs. 2d - 2g or the back-end steps of Figs. 3f - 3i, the complete process requires slightly more process operations than the . complete process of each of Figs. 2 and 3. This is the tradeoff for lessening the constraint on the primary layer thickness and, relative to the process of Fig. 2, also lessening the constraint on the gate layer thickness.

[0085] The material used to form further layer 74A is a material that can be used as an etch mask for etching primary layer 72A and can also be selectively etched with respect to layer 72A. The further material typically consists of a metal. The further material is typically nickel when the gate material is chromium, and vice versa. However, depending on the selection of other materials used in fabricating the field emitter, the further material could be electrically resistive or electrically insulating.

[0086] Spherical particles 46 are now removed, typically in the manner described above. During the sphere removal, further material portions 74B are simultaneously removed to produce the structure of Fig. 4e. Further openings 76 extend through further layer 74A at the locations of removed particles 46. Because particles 46 were spherical, further openings 76 are largely circular. The diameter of each further opening 76 is approximately the same as the diameter of corresponding removed sphere 46.

[0087] Using further layer 74A as an etch mask, primary layer 72 is anisotropically etched through further openings 76 to form corresponding primary openings 78 through layer 72 down to gate layer 60. See Fig. 4f in which item 72A is the remainder of primary layer 72. Each primary opening 78 is vertically centered on, and

is of approximately the same diameter as, corresponding further opening 76. Since further openings 76 are situated at the locations of removed spheres 46, the locations of primary openings 78 are defined by particles 46. Also, primary openings 78 are of largely the same shape as further openings 76 and therefore are largely circular.

[0088] With further layer 74A still serving as an etch mask, gate layer 60 can be anisotropically etched through further openings 76 and primary openings 78 to form corresponding gate openings 80 through layer 60 down to insulating layer 44. Fig. 4g1 illustrates the resultant structure. Item 60B is the remainder of gate layer 60. Since the etch is anisotropic, the diameter of each gate opening 80 is approximately the same as the diameter of corresponding (overlying) opening pair 78 and 76. The gate opening etch can be performed as a continuation of the primary opening etch or as a separate step with a different anisotropic etchant.

[0089] Each gate opening 80 is vertically centered on, and thus vertically aligned to, both corresponding primary opening 78 and corresponding further opening 76. Inasmuch as further openings 76 are situated at the locations of removed spheres 46, the locations of gate openings 80 are defined by the locations of particles 46. Also, gate openings 80 are largely circular.

[0090] Further layer 74A in Fig. 4gl can now be removed to produce a structure which, except for a partial difference in labeling and potential differences in the gate-layer and primary-layer thicknesses, is substantially identical to the structure of Fig. 2d. Items 60B, 72A, 78, and 80 in Fig. 4gl respectively correspond to items 48A, 50A, 52, and 54 in Fig. 2d. Subject to this labeling difference, the front-end processing sequence of Fig. 4 is completed according to the above-mentioned back-end steps that lead from the structure of Fig. 2d to the final structure of Fig. 2g. Conical electron-emissive elements 58A thereby extend through gate openings 52 (80) in gate layer 48A (60B) of the so-completed field emitter

[0091] Alternatively, when applying the back-end portion of the method of Fig. 2 to the front-end processing sequence of Fig. 4, dielectric openings 56 can be formed in insulating layer 44 when further layer 74A is still in place and serves as an etch mask. In this case, further layer 74A is removed immediately prior to the cone material deposition of Fig. 2f.

[0092] As another alternative, further layer 74A can be removed directly after forming primary openings 78 at the stage shown in Fig. 4f and therefore before creating gate openings 80 at the stage shown in Fig. 4gl. Using primary layer 72A as an etch mask, gate openings 80 are formed by anisotropically etching gate layer 60 through primary openings 78 to produce the structure of Fig. 2d, again subject to partially different labeling (gate openings 80 in Fig. 4 become gate openings 54 in Fig. 2) and potential differences in the gate-layer and primary-layer thicknesses. The processing steps leading from the structure of Fig. 2d to the structure of Fig. 2g are then undertaken in the manner described above to form the field emitter.

[0093] Instead of performing an anisotropic, and therefore non-undercutting, etch through openings 76 and 78, an undercutting etch can be performed on gate layer 60 of Fig. 4f through openings 76 and 78 to form corresponding gate openings 82 through layer 60 down to insulating layer 44. See Fig. 4g2 in which item 60C is now the remainder of gate layer 60. With gate openings 82 undercutting primary layer 72A, the diameter of each gate opening 82 is greater than the diameter of corresponding (overlying) opening pair 78 and 76. Each gate opening 82 is largely circular and is vertically centered on corresponding opening pair 78 and 76. Since further openings 76 are situated at the locations of removed spheres 46, spherical particles 46 define the locations of gate openings 82.

[0094] Further layer 74A in Fig. 4g2 can be removed to produce a structure which, except for a partial labeling difference and potentially a difference in the primary-layer thickness, is substantially identical to the structure of Fig. 3f. Items 60C, 72A, 78, and 82 in Fig. 4g2 respectively correspond to items 60A, 62A, 64, and 66 in Fig. 3f. Subject to this labeling difference, the front-end processing sequence of Fig. 4 is now completed according to the above-mentioned back-end steps that lead from the structure of Fig. 3f to the structure of Fig. 3i. Conical electron-emissive elements 70A are thereby exposed through gate openings 66 (82) in gate layer 60A (60C) of the so-completed field emitter.

[0095] As a further alternative in applying the back-end portion of the process of Fig. 3 to the front-end processing sequence of Fig. 4, further layer 74A can be removed directly after forming primary openings 78 at the stage shown in Fig. 4f. Using primary layer 72A as an etch mask, gate openings 82 are created by performing an undercutting etch on gate layer 60 through primary openings 78 to produce the structure of Fig. 3f, again subject to partially different labeling (gate openings 82 in Fig. 4 become gate openings 66 in Fig. 3) and potentially a difference in the primary-layer thickness. The processing steps leading from the structure of Fig. 3f to the structure of Fig. 3i are then undertaken to finish the field emitter in the manner described above.

[0096] Looking now at the various electron emitters manufactured according to the fabrication steps of Figs. 2 - 4 including the above-mentioned variations, the locations of the conical electron-emissive elements, such as cones 58A or 70A, are determined by the locations of the primary openings, such as openings 52, 64, or 78. Since the locations of the primary openings are determined (directly or indirectly) by the locations of spherical particles 46, the locations of the electron-emissive cones are defined by particles 46.

[0097] The electron-emissive cones are situated at random, or largely random locations, relative to one another since the surface distribution of particles 46 is ran-

dom, or largely random. Nonetheless, the number of electron-emissive cones per unit area does not vary greatly from place to place across the entire electron-emitting area.

[0098] The base diameter of each electron-emissive cone in each of the electron emitters manufactured according to the fabrication steps of Figs. 2 - 4 (again including the above-mentioned process variations) is approximately the same as the base diameter of the corresponding primary opening and thus is approximately the same as is the diameter of corresponding removed sphere 46. Consequently, the average base diameter of the electron-emissive cones is controlled by adjusting the average diameter of particles 46. Decreasing the average particle diameter causes the average cone diameter to be decreased by an approximately equal amount, and vice versa. In this way, particles 46 determine the lateral area occupied by the electron-emissive cones. Inasmuch as spheres 46 define the locations of the electron-emissive cones, the average spacing between the cones is controlled by adjusting the average surface density and average diameter of spheres 46.

[0099] The standard deviation in the average diameter of particles 46 is, as noted above, quite small compared to the average particle diameter. The standard deviation in the average base diameter of the electron-emissive cones is thus, to a first approximation, equally small compared to the average cone base diameter. Since particles 46 are spherical, the base of each electron-emissive cone is largely circular. The lateral areas occupied by the cones are largely equal. By appropriately adjusting parameters such as the thickness of interelectrode dielectric layer 44, electron-emissive elements of highly uniform size and shape can be achieved.

[0100] The electron-emissive elements are preferably fabricated so as to be small and closely spaced together. This is accomplished by utilizing spheres of suitably small average sphere diameter and by distributing an appropriately high density of spheres 46 across the sphere-receiving surface. With there being little variation in the sizes and shapes of the individual electron-emissive cones for a particular area electron emitter, the electron emission is relatively uniform across the electron-emitting area. Importantly, this highly desirable feature is achieved largely by controlling the size and surface density of particles 46, thereby enabling the electron current to be well controlled.

Fabrication of Field Emitters with Electron-Emissive Filaments

[0101] A gated field-emission cathode having electron-emissive elements shaped like filaments, rather than cones, can be produced in accordance with the invention's teaching by utilizing a suitable back-end filamentary process sequence to complete the front-end process sequence of Fig. 4, as ended with Fig. 4gl, or to complete the front-end portion of the process of either of Figs. 2 and 3.

[0102] Figs. 5a - 5g (collectively "Fig. 5") illustrate a back-end processing sequence which is so applied to the front-end sequence of Figs. 4a - 4f and 4gl and which utilizes spacers in accordance with the invention to produce a gated field emitter having filamentary electron-emissive elements. Referring to Fig. 4g1, an anisotropic etch is performed on insulating layer 44 through further openings 76, primary openings 78, and gate openings 80 using further layer 74 as an etch mask to form corresponding dielectric openings 100 through layer 44 down to lower non-insulating region 42. This leads to the structure of Fig. 5a in which item 44C is the remainder of insulating layer 44. Each dielectric opening 100 is vertically centered on, and is of approximately the same diameter as, corresponding opening triad 76, 78, and 80. Also, dielectric openings 100 are largely circular.

[0103] Further layer 74A is removed with etchant that does not significantly attack primary layer 72A or any other part of the structure. Fig. 5b depicts the resultant structure.

[0104] Suitably etchable spacer (or coating) material is conformally deposited on primary layer 72A and into composite openings 78/80/100 down to lower non-insulating region 42 to form a blanket spacer (or coating) layer 102 as shown in Fig. 5c. Spacer layer 102 covers the top of the structure but does not completely fill openings 78/80/100. Depressions 104 are present at the unfilled portions of openings 78/80/100. Each depression 104 is vertically centered on corresponding composite opening 78/80/100.

[0105] CVD is typically used to deposit the spacer material. Consequently, the thickness of spacer layer 102 along the side edges of layers 72A, 60B, and 44C along each composite opening 78/80/100 is relatively uniform (constant) at any given height.

[0106] The spacer material is typically chosen to be commonly etchable with the primary material of layer 72A. The spacer material also preferably has a high etch selectivity relative to the interelectrode dielectric (layer 44C here). In particular, the spacer material is typically the same as the primary material and different from the interelectrode dielectric. For example, the spacer material is normally silicon nitride when (a) the primary material consists of silicon nitride and (b) the interelectrode dielectric consists of silicon oxide.

[0107] An anisotropic etch is performed to remove substantially all of spacer layer 102 except for portions 102A that cover (a) the side edges of primary layer 72A along primary openings 78, (b) the side edges of gate layer 60B along gate openings 80, and (c) the side edges of insulating layer 44C along dielectric openings 100. See Fig. 5d. Inasmuch as central portions of spacer layer 102 at the bottoms of dielectric openings 100 are removed during the etch, depressions 104 are extended down to lower non-insulating region 42 and slightly widened (not shown in Fig. 5d) to become corresponding

apertures 104A. Since depressions 104 were vertically centered on composite openings 78/80/100, each aperture 104A is vertically centered on corresponding composite opening 78/80/100.

[0108] Electrically non-insulating emitter filament material is electrochemically deposited (electroplated) into apertures 104A to form corresponding precursor electron-emissive elements 106 that contact lower non-insulating region 42. Fig. 5e depicts the resulting structure. During the electrochemical deposition, the combination of primary layer 72A, spacer portions 102A, and insulating layer 44C encapsulates gate layer 60B (except possibly along the lateral perimeter of the structure) to prevent precursor electron-emissive elements 106 from contacting layer 60B. The lateral spacing between gate layer 60B and precursor elements 106 is determined by the thickness of spacers 102A.

[0109] The emitter filament material is normally a metal such as nickel or platinum. When precursor filaments 106 are later sharpened by an electropolishing technique, the filament material is normally different from the gate material.

[0110] The electrochemical deposition is typically done in the manner described in Spindt et al, U.S. Patent 5,564,959.

[0111] During the electrochemical deposition, lower non-insulating region 42 serves as the deposition cathode. A deposition anode is situated in the deposition electrolyte a short distance above primary layer 72A.

[0112] The electrochemical deposition is conducted for a time sufficiently long to overfill apertures 104A but not cause precursor electron-emissive elements 106 to meet one another along the top of primary layer 72A. Consequently, each precursor element 106 has a cap portion 106A that extends out of corresponding aperture 104A. The overfill of apertures 104A helps to assure that the final electron-emissive filaments will not be of significantly different height due to differences in the nucleation and growth of the filament material.

[0113] Primary layer 72A and spacers 102A are removed, preferably with etchant that does not significantly attack insulating layer 44C. See Fig. 5f. As a result of the etch, precursor electron-emissive elements 106 are separated from gate layer 60B and insulating layer 44C by cylindrical apertures 108.

[0114] When primary layer 72A and spacers 102A consist of the same material (e.g., silicon nitride), the etch is typically performed in a single step with a wet chemical. Alternatively, a plasma having an isotropic component can be used to perform the etch. The etch can be done in two stages when layer 72A and spacers 102A are formed with different materials..

[0115] Precursor elements 106 are processed to remove caps 106A and provide the remaining filamentary portions with sharp tips that extend at least partially through gate openings 80. Fig. 5g shows the final gated field emitter in which sharpened filamentary electron-emissive elements 106B are the remainders of precursor elements 106. Since apertures 104A were vertically centered on composite openings 78/80/100, each electron-emissive filament 106B is vertically centered on corresponding gate opening 80.

[0116] The conversion of precursor electron-emissive elements 106 into electron-emissive filaments 106B is preferably done electrochemically according to an electropolishing/sharpening technique of the type described in U.S. Patent 5,564,959 cited above. Lower non-insulating emitter region 42 in conjunction with precursor elements 106 serves as the anode during the electropolishing/sharpening operation. Gate layer 60B functions as the cathode. During the electropolishing/sharpening operation, the material of precursor elements 106 is removed generally along the plane of gate layer 60B, causing elements 106 to be pinched off and form sharpened tips. Cap portions 106A are washed away in the electropolishing/sharpening electrolyte, leaving electron-emissive filaments 106B as depicted in Fig. 5g.

[0117] Because gate openings 80 were vertically concentric with further openings 76, each gate opening 80 is vertically centered on the location of corresponding removed sphere 46. Consequently, the locations of electron-emissive filaments 106B are defined by (the locations of) spherical particles 46.

[0118] Also, the diameter of each aperture 104A equals the diameter of corresponding composite opening 70/80/100 minus twice the thickness of corresponding spacer 102A. Since the diameter of each composite opening is approximately the same as the diameter of corresponding removed sphere 46, the lateral areas occupied by filaments 106B are controlled by the size of spheres 46 and the thickness of spacers 102A.

[0119] The spacer thickness varies little from spacer 102A to spacer 102A. As mentioned above, the size of spherical particles 46 varies little from one sphere 46 to another. Inasmuch as the surface density of spheres 46 did not vary greatly across primary layer 72, the sphere size and surface density in combination with the spacer thickness can be suitably adjusted so that filaments 106B provide highly uniform electron emission across the electron-emitting area at a controllable magnitude of the electron current.

[0120] Instead of starting the back-end process sequence of Fig. 5 from the structure of Fig. 4g1, further layer 74A could be removed directly after the step shown in Fig. 4f. With primary layer 72A now serving as an etch mask, gate layer 60 and insulating layer 44 are anisotropically etched through primary openings 78 (and through gate openings 80 for layer 44) to produce the structure of Fig. 5b. A two-stage etch process is typically used, one stage for layer 60 and the second for layer 44. From this point on, the structure of Fig. 5b is further processed in the way described above for Figs. 5c - 5g.

[0121] The front-end portions of the methods of Figs. 2 and 3 can be combined with the back-end process sequence of Fig. 5 in ways similar to that described above.

Starting from the structure of Fig. 2d, dielectric openings 100 can be created through insulating layer 44 by performing an anisotropic etch on layer 44 through openings 52 and 54 using primary layer 50A as an etch mask. Except for partially different labeling and potential differences in the primary-layer and gate-layer thicknesses, the structure of Fig. 5b is produced.

[0122] Similarly, starting from the structure of Fig. 3e, gate openings 80 and dielectric openings 100 can be created by anisotropically etching gate layer 60 and insulating layer 44 through primary openings 64 using primary layer 62A as an etch mask. The anisotropic etch is typically performed in two stages, one for layer 60 and the second for layer 44. Subject to partial differences in labeling and a potentially different primary-layer thickness, the structure of Fig. 5b is again produced.

[0123] In the alternatives described in the preceding three paragraphs, each gate opening 80, 66, or 54 is vertically centered on the location of corresponding removed sphere 46 because the gate openings were vertically concentric with primary openings 78, 64,-or 52. Spheres 46 therefore define the locations of electron-emissive filaments 106B. Also, the combination of spheres 46 and spacers 102A controls the lateral areas occupied by filaments 106B. Accordingly, filaments 106B can provide highly uniform electron emission at a controlled magnitude by suitably adjusting the sphere size and surface density in combination with the spacer thickness.

[0124] Figs. 6a-6h (collectively "Fig.6") depict another back-end process sequence which is applied to the front-end process sequence of Figs. 4a - 4f and 4g1 and which utilizes spacers in accordance with the invention to produce a gated field-emission cathode having filamentary electron-emissive elements. After forming the structure of Fig. 4g1, further layer 74A is removed. This leads to the structure of Fig. 6a.

[0125] Suitably etchable spacer (or coating) material is conformally deposited on primary layer 72A and into composite openings 78/80 to form a blanket spacer (or coating) layer 110 as shown in Fig. 6b. Spacer layer 110 covers the top of the structure but does not completely fill openings 78/80. Depressions 112 are present at the unfilled portions of openings 78/80. Each depression 112 is vertically centered on corresponding composite opening 78/80.

[0126] CVD is normally used to deposit the spacer material. The thickness of spacer layer 110 along the side edges of layers 72A and 60B along each composite opening 78/80 is relatively uniform at any given height. The spacer material in the process sequence of Fig. 6 has the same characteristics relative to the primary material and the interelectrode dielectric as in the process sequence of Fig. 5.

[0127] An anisotropic etch is performed to remove substantially all of spacer layer 110 except for annular portions 110A that cover (a) the side edges of primary layer 72A along primary openings 78 and (b) the side edges of gate layer 60B along gate openings 80. See Fig. 6c. Depressions 112 are thereby extended down to insulating layer 44 and slightly widened (not shown in Fig. 6c) to become corresponding apertures 112A. Since depressions 112 were vertically centered on openings 78/80, each aperture 112A is vertically centered on corresponding opening 78/80.

[0128] Using primary layer 72A and annular spacer portions 110A as an etch mask, insulating layer 44 is anisotropically etched through apertures 112A to form dielectric openings 114 through layer 44 down to lower non-insulating region 42. See Fig. 6d. Item 44D is the remainder of insulating layer 44.

[0129] Electrically non-insulating emitter filament material is electrochemically deposited into composite openings (or apertures) 112A/114 to form precursor electron-emissive filaments 116 that contact non-insulating 42. The resulting structure is shown in Fig. 6e. During the electrochemical deposition, the combination of primary layer 72, spacers 110A, and insulating layer 44D encapsulates gate layer 60B (except possibly along the lateral periphery of the structure) to prevent precursor electron-emissive elements 116 from contacting gate layer 60B. Spacers 116A determine the lateral spacing between gate layer 60B and precursor elements 116. The emitter filament material is again normally a metal such as nickel or platinum.

[0130] The electrochemical deposition is performed in the manner described above for the process sequence of Fig. 5. The deposition time is sufficiently long to overfill openings 112A/114 but typically not long enough to cause precursor elements 116 to meet one another along the top of primary layer 72A. Each precursor electron-emissive element 116 thus has a cap portion 116A that extends out of corresponding aperture 112A/114. As in the process sequence of Fig. 5, the overfilling reduces the likelihood of creating electron-emissive filaments of significantly different height due to differences in the nucleation and growth of the filament material.

[0131] Primary layer 72A and spacers 110A are removed, preferably with etchant that does not significantly attack insulating layer 44D or gate layer 60B. See Fig. 6f. Outer portions of gate openings 80 are thereby reopened. These portions of gate openings 80 now separate precursor elements 116 from gate layer 60B. When primary layer 72A and spacers 110A are formed with the same material, the etch is typically done in a single step with a wet chemical or a plasma having an isotropic component. A two-stage etch process is normally used when layer 72A and spacers 110A consist of different materials.

[0132] Precursor electron-emissive elements 116 are processed to remove cap portions 116A and to provide the remaining filamentary portions with sharpened tips that extend at least partially through gate openings 80. See Fig. 6g in which sharpened filamentary electron-emissive elements 116B are the remainders of precursor elements 116. Electron-emissive filaments 116B are

created from precursor elements 116 by an electropolishing/sharpening technique in substantially the same way as that utilized to produce electron-emissive filaments 106B in the process sequence of Fig. 5. Consequently, each electron-emissive filament 116B is vertically centered on corresponding gate opening 80.

[0133] Using gate layer 60B as an etch mask, insulating layer 44D is etched through gate openings 80 in an undercutting, typically isotropic, manner to form corresponding dielectric open spaces 118 around electron-emissive filaments 116B. Fig. 6h shows the resultant structure. Item 44E is the remainder of insulating layer 44D. Dielectric open spaces 118 may extend partially or fully through insulating layer 44E. Fig. 6h illustrates the fully through case.

[0134] The electropolishing/sharpening step can be performed before creating dielectric open spaces 118. The final structure appears substantially the same as shown in Fig. 6b. Alternatively, dielectric open spaces 118 can be formed by an anisotropic etch so that open spaces 118 do not significantly undercut gate layer 60B.

[0135] With each gate opening 80 being vertically centered on the location of corresponding removed sphere 46, the locations of spherical particles 46 define the locations of electron-emissive filaments 116B. Similar to the process of Fig. 5, the lateral areas occupied by filaments 116B are controlled by spheres 46 and spacers 110.

[0136] Instead of beginning the back-end process sequence of Fig. 6 at the structure of Fig. 4gl, the back-end process sequence can be started at the structure of Fig. 4f. Further layer 74A is removed. Using primary layer 72A as an etch mask, gate layer 60 is anisotropically etched through primary openings 78 to produce the structure of Fig. 6a.

[0137] The front-end portion of the process of each of Figs. 2 and 3 can also be completed with the back-end process sequence of Fig. 6 in accordance with the invention to produce a gated field emitter having filamentary electron-emissive elements. Subject to partial differences in labeling and potential differences in the primary-layer and gate-layer thicknesses, the structure of Fig. 6a repeats the structure of Fig. 2d to serve as a joining point for the front-end portion of the process of Fig. 2 and the back-end process sequence of Fig. 6.

[0138] The structure of Fig. 3e serves as a joining point for the front-end portion of the process of Fig. 2 and the back-end process sequence of Fig. 6. Referring to Fig. 3e, gate openings 80 are created by anisotropically etching gate layer 60 through primary openings 64 using primary layer 62A as an etch mask. Subject to partial differences in labeling and a potentially different primary layer thickness, the structure of Fig. 6a is again produced.

[0139] In the alternatives described in the two preceding paragraphs, the locations of filaments 116B are again defined by particles 46. Likewise, spheres 46 and spacers 110 control the lateral areas occupied by filaments 116B. The sphere size and surface density, along with the spacer thickness, can then be appropriately varied so that filaments 116B provide highly uniform electron emission at a controlled magnitude.

[0140] Figs. 7a - 7j (collectively "Fig. 7") present an example of a full process for manufacturing a gated field-emission cathode which employs spherical particles to define gate openings and which utilizes spacers in creating filamentary electron-emissive elements in accordance with the invention. In the process of Fig. 7, an initial structure consisting of substrate 40, lower non-insulating region 42, and insulating layer 44 is formed in substantially the same way as in the process of Fig. 2. Fig. 7a, which repeats Fig. 2a, illustrates structure 40/42/44 for the process of Fig. 7. Likewise, as shown in Fig. 7b, solid spherical particles 46 are distributed across the top of insulating layer 44. The sphere deposition is performed according to the random, or largely random, technique described above for the process of Fig. 2.

[0141] Electrically non-insulating gate material is deposited on insulating layer 44 and spherical particles 46, preferably in a direction substantially perpendicular to the upper surface of layer 44 using a technique such as evaporation or collimated sputtering. The gate material accumulates on insulating layer 44 in space between particles 46 to form an electrically non-insulating gate layer 120A of relatively uniform thickness. See Fig. 7c. Portions 120B of the gate material simultaneously accumulate on the upper halves of spheres 46. To avoid having gate material portions 120B bridge to gate layer 120A, the thickness of gate layer 120A is normally less than the average sphere radius. The gate material typically consists of a metal such as chromium, nickel, molybdenum, titanium, tungsten, or gold.

[0142] Spheres 46 are removed, typically according to the technique utilized in the process of Fig. 2. During the sphere removal, gate material portions 120B are removed to produce the structure of Fig. 7d. Gate openings 122 extend through gate layer 120A at the respective locations of removed particles 46. Gate openings 122 are largely circular since particles 46 are spherical. The diameter of each gate opening 122 is approximately the same as the diameter of corresponding removed sphere 46. Since gate openings 122 are created during the deposition of gate layer 120A without the necessity for a gate layer etch, the gate material here can be gold.

[0143] Suitably etchable spacer (or coating) material is deposited, typically in a conformal manner, on gate layer 120A and into gate openings 122 down to insulating layer 44 to form a blanket spacer (or coating) layer 124 as shown in Fig. 7e. Spacer layer 124 covers the top of the structure but does not completely fill gate openings 122. Depressions 126 are present at the unfilled portions of gate openings 122. Each depression 126 is vertically centered on corresponding gate opening 122.

[0144] With CVD being used to deposit the spacer

material, the thickness of spacer layer 124 at the side edges of gate layer 120 along each gate opening 122 is relatively uniform at any given height. The spacer material is chosen so as to be selectively etchable with respect to the gate material and the interelectrode dielectric. The spacer material is typically an electrical insulator (the case shown in Fig. 7e) such as silicon nitride but could be an electrical non-insulator, for example, a metal such as aluminum. When the spacer material consists of metal, the spacer material deposition can be performed electrochemically. In this case, the deposition is typically not conformal across the upper surface of the structure.

[0145] An anisotropic etch is performed to remove substantially all of spacer layer 124 except for portions 124A that cover the side edges of gate layer 120A along gate openings 122. See Fig. 7f. Inasmuch as central portions of spacer layer 124 at the bottoms of gate openings 122 are removed during the etch, depressions 126 are extended through spacer layer 124 down to insulating layer 44 and'are slightly widened (not shown in Fig. 7f) to become apertures 126A.

[0146] Each spacer portion 124A is pictorially quite small in Fig. 7f. To illustrate spacers 124A more clearly, Fig. 8a presents an enlarged view of a portion of the structure of Fig. 7f centered around the intended location for the left-hand electron-emissive element.

[0147] Using gate layer 120A and spacers 124A as an etch mask, insulating layer 44 is anisotropically etched through apertures 126A to form corresponding dielectric openings 128 through layer 44 down to lower non-insulating region 42. See Fig. 7g. Item 44F is the remainder of insulating layer 44. Since depressions 126 were vertically centered on gate openings 122, each composite opening 126A/128 is vertically centered on corresponding gate opening 122.

[0148] Electrically non-insulating filament material is electrochemically deposited into composite openings (or apertures) 126A/128 to form precursor electron-emissive elements 130 that contact lower non-insulating region 42. Fig. 7h depicts the resulting structure. The electrochemical deposition is again typically performed in the manner described in above-cited U.S. Patent 5,564,959. Likewise, the emitter filament material again normally is a metal such as nickel or platinum.

[0149] The deposition time is sufficiently long to completely fill dielectric openings 128 and to partially fill apertures 126A but not so long that each precursor electron-emissive element 130 extends laterally beyond its spacer 124A. Consequently, precursor elements 130 are laterally separated from gate layer 120A by (the thickness of) spacer portions 124A. Because spacers 124A are pictorially small in Fig. 7h, Fig. 8b presents an enlarged view of a portion of the structure of Fig. 7h centered on left-hand precursor element 130.

[0150] Spacer portions 124A are removed with etchant that does not significantly attack gate layer 120A. Using gate layer 120A as an etch mask, insulating layer 44F is etched through gate openings 122 in an undercutting, typically isotropic, manner to form corresponding dielectric open spaces 132 around precursor electron-emissive elements 130. See Fig. 7i in which item 44G is the remainder of insulating layer 44F. Dielectric open spaces 132 may extend partially or fully through insulating layer 44G. Fig. 7i depicts the partially through case.

[0151] An electropolishing/sharpening operation is conducted to provide precursor electron-emissive elements 130 with sharpened tips. Fig. 7j shows the resulting structure. Filamentary electron-emissive elements 130A are the sharpened remainders of precursor elements 130. The electropolishing/sharpening operation is again performed according to a technique of the type described in U.S. Patent 5,564,959.

[0152] The operations shown in Figs. 7i and 7j can be reversed. That is, precursor elements 130 can be electropolished/sharpened to form electron-emissive filaments 130A after which dielectric open spaces 132 are formed around elements 130A. Also, open spaces 132 can be formed by an anisotropic etch so that they do not significantly undercut gate layer 120A.

[0153] In any case, with composite openings 126A/128 being vertically centered on gate openings 122, each filamentary electron-emissive element 130A is vertically centered on corresponding gate opening 122. Since each gate opening 122 is vertically centered on corresponding removed sphere 46, spherical particles 46 define the locations of filaments 130A. The lateral areas occupied by filaments 130A are controlled by the diameter of spheres 46 and the thickness of spacer layer 124. Filaments 130B can therefore be arranged to provide highly uniform electron emission at a controlled magnitude by appropriately adjusting the sphere size and surface density along with the spacer thickness.

[0154] Figs. 9a - 9c (collectively "Fig. 9") illustrate an enlarged view of a process sequence that can be applied to the structure of Fig. 7g in fabricating a gated field-emission cathode having filamentary electron-emissive elements in accordance with the invention. In the process of Figs. 7a - 7g and Fig. 9, spacer portions 124A consist of electrically non-insulating material, normally a metal, that is selectively etchable with respect to both the emitter filament material and the gate material. For example, when (a) the gate material is chromium and (b) the filament material is nickel, the spacer material of portions 124A is typically aluminum. Also, as described more fully below in connection with Fig. 14, lower non-insulating emitter region 42 in the process sequence of Fig. 9 consists of a lower electrically conductive layer and an upper electrically resistive layer.

[0155] Starting from the structure of Fig. 7g, the emitter filament material is electrochemically deposited into composite apertures 126A/128 to form precursor filamentary electron-emissive elements 134. During the electrochemical deposition, gate layer 120A acts as a control electrode. Non-insulating spacers 124A contact

gate layer 120A and therefore serve as part of the control electrode. A deposition anode is situated in the deposition electrolyte. Lower non-insulating emitter region 42 is the deposition cathode. Since the filament material being deposited into dielectric openings 126A contacts lower non-insulating region 42, the filament material that accumulates in apertures 126A/128 serves as part of the deposition cathode.

[0156] The lower conductive layer of lower non-insulating region 42 is maintained at a voltage sufficient to cause the emitter filament material to electrochemically accumulate in dielectric openings 126A on the upper resistive layer of non-insulating region 42. Gate layer 120A is, on the other hand, maintained at a voltage insufficient to cause the filament material to electrochemically deposit on the control electrode formed with gate layer 120A and non-insulating spacers 124A.

[0157] The accumulation of filament material in dielectric openings 126A continues until precursor electron-emissive filaments 134 touch non-insulating spacers 124A, as indicated at point 136 in Fig. 9a. When each precursor filament 134 touches its non-insulating spacer 124A, that filament 134 is electrically shorted to the control electrode formed with gate layer 120A and non-insulating spacers 124A. The voltage of each so-shorted filament 134 then changes from the deposition-cathode value sufficient for electrochemical deposition of the filament material to the control-electrode value insufficient for filament material deposition. Accordingly, the electrochemical deposition of that filament 134 is terminated.

[0158] When each precursor filament 134 is electrically shorted to the control electrode, control-electrode current flows through that filament 134 and the underlying portion of the upper resistive layer in lower non-insulating region 42. The combined resistance R_D of each so-shorted filament 134 and the underlying portion of the upper resistive layer causes a voltage drop V_D to occur across that filament 134 and the underlying portion of the lower resistive layer.

[0159] For each electrically shorted filament 134, the value of combined resistance R_D is sufficiently high to cause voltage drop V_D to reach a value adequate to prevent the deposition-cathode voltage of the lower conductive layer of non-insulating region 42 from being changed to a value sufficient for electrochemical deposition of the filament material. Consequently, termination of the deposition of one precursor filament 134 has little effect on the deposition of another precursor filament 134. Deposition of all of precursor filaments 134 substantially terminates as each of them independently touches its non-insulating spacer 124A. The filament material thus cannot bulge out of apertures 126A sufficiently far to cause precursor filaments 134 to bridge to gate layer 120A.

[0160] Using a suitable etchant that does not significantly attack gate layer 120A or precursor electron-emissive filaments 134, spacer portions 124 are removed to produce the structure of Fig. 9b. An electropolishing/sharpening operation is performed to convert precursor elements into sharpened filamentary electron-emissive elements 134A as shown in Fig. 9c.

[0161] With gate layer 120A serving as an etch mask, insulating layer 44 is etched through gate openings 122 in an undercutting, typically isotropic, manner to form corresponding dielectric open spaces 138 around electron-emissive filaments 134A. Item 44H in Fig. 9c is the remainder of insulating layer 44F. The electropolishing/sharpening operation can be performed before or after the etch to create dielectric open spaces 138. In either case, the structure of Fig. 9c is further processed in the manner described above.

[0162] Regardless of whether dielectric open spaces 138 are created before or after the electropolishing/sharpening operation, each filamentary electron-emissive element 134A is vertically centered on corresponding gate opening 122. Consequently, spheres 46 define the locations of electron-emissive filaments 134A. Also, spheres 46 and spacers 124A control the lateral areas occupied by filaments 134A. The uniformity and magnitude of the electron emission from filaments 134A is then controlled by appropriately varying the sphere size and surface.density in combination with the spacer thickness.

[0163] The technique utilized to automatically terminate electrochemical deposition of the filament material in the process sequence of Fig. 9 can be applied to a process that includes the process sequence of Figs. 6a - 6d. In this case, annular spacer portions 110A consist of electrically non-insulating material, normally a metal, which is selectably etchable with respect to the filament and gate materials. Spacer portions 110A are also typically selectively etchable with respect to the primary material. Primary layer 72A may consist of electrically non-insulating material, again normally a metal such as aluminum, which is selectively etchable with respect to the filament and gate materials. Lower non-insulating region 42 again consists of a lower conductive layer and an upper resistive layer as described further below in connection with Fig. 14.

[0164] Beginning at the structure of Fig. 6d, electrochemical deposition of the emitter filament material is performed with an electrochemical cell in which gate layer 60B acts as the control electrode. Since spacer portions 110A contact gate layer 60B, spacers 110A act as part of the control electrode. With the deposition anode being situated in the deposition electrolyte, lower non-insulating emitter region 42 is the deposition cathode. The filament material being deposited into dielectric openings 114 contacts region 42 and thus serves as part of the deposition cathode.

[0165] When the filament material accumulating in each dielectric opening 114 touches corresponding spacer portion 110A, the deposition cathode for electron-emissive filament 116 being formed in that opening 114 is electrically shorted to the control electrode. This

terminates the electrochemical deposition of the filament material into that opening 114. Precursor electron-emissive filaments having shapes similar to precursor filaments 134 in Fig. 9a are formed in dielectric openings 114.

[0166] Primary layer 72A and spacer portions 110A are subsequently removed. An electropolishing step is performed to sharpen each electron-emissive filament, and an etch is performed through gate openings 80 to create dielectric open spaces around the filaments. As in the process sequences of Figs. 6, 7, and 9, either of these steps can be performed first. The resulting structure appears generally as shown in Fig. 6h or 7j depending on whether the dielectric open spaces extend fully or partly through insulating layer 44.

[0167] In the processes/process sequences of Figs. 5 - 7, spacers are created by depositing a blanket layer of the spacer material and then removing undesired portions of the blanket layer. Spacers can, however, be formed by a selective deposition technique in certain circumstances. The requisite circumstances typically arise when the gate layer is exposed along its side edges but not along its upper or lower surface.

[0168] Figs. 10a - 10g (collectively "Fig. 10") depict a back-end process sequence which is applied to the front-end process sequence of Figs. 3a - 3f and which utilizes selective spacer deposition in accordance with the invention to produce a gated field-emission cathode having filamentary electron-emissive elements. As illustrated in Fig. 10a which repeats Fig. 3f, each gate opening 66 is slightly larger than corresponding primary opening 64 in the back-end process sequence of Fig. 10 so that gate opening 66 slightly undercut primary layer 62A. Nonetheless, each gate opening 66 can be a substantially the same diameter as corresponding primary opening 64. Regardless of whether gate openings 66 do, or do not, undercut primary layer 62A, only the side edges of gate layer 60A are exposed.

[0169] Using an electrochemical technique, suitably etchable electrically non-insulating spacer (or coating) material is selectively deposited on the exposed edges of gate layer 60 along gate openings 66 to form annular electrically non-insulating spacers 140. See Fig. 10b. Apertures 142 extend respectively through annular spacers 140. Each aperture 142 is vertically aligned to corresponding annular spacer 140. The electrochemical deposition is performed for a time sufficiently long that the diameter of each aperture 142 is considerable less than the diameter of corresponding gate opening 64.

[0170] During the electrochemical spacer deposition, gate layer 60A is the deposition cathode. Since spacers 140 contact gate layer 60A, spacers 140 form part of the cathode as they are grown along the gate edges. The deposition anode is situated in the deposition electrolyte.

[0171] Spacers 140 are selectively etchable with respect to gate layer 62A, insulating layer 44, and the material later used informing the electron-emissive filaments. The spacer material is normally a material such as copper or nickel subject to being different from the gate material and also being different from the filament material.

[0172] Using gate layer 62A and spacers 140 as an etch mask, insulating layer 44 is anistropically etched through gate openings 64 and apertures 142 to form corresponding dielectric openings 144 through insulating layer 44 down to lower non-insulating region 42. Fig. 10c shows the resultant structure. Items 44I are the remainder of insulating layer 44. The side walls of dielectric openings 144 are largely vertical. Since each aperture 142 is of smaller diameter than corresponding gate opening 64, the diameter of each dielectric opening 144 approximately equals the diameter of corresponding aperture 142.

[0173] Electrically non-insulating emitter filament material is electrochemically deposited into dielectric openings 144 to form precursor electron-emissive filaments 146 that contact lower non-insulating region 44. See Fig. 10d. The filament deposition is performed until precursor filaments 146 touch, or nearly touch, spacers 140. The electrochemical filament deposition is typically performed according to the techniques generally described in U.S. Patent 5,564,959. The filament deposition is terminated either after a selected deposition time or according to the automatic technique utilized in the process sequence of Fig. 9.

[0174] During the electrochemical filament deposition, the combination of primary layer 62A, spacers 140, and insulating layer 44I encapsulates gate layer 60A (again except possibly along the lateral periphery of the structure) to prevent precursor electron-emissive filaments 146 from touching gate layer 60A. Spacers 140 determine the lateral spacing between precursor filaments 146 and gate layer 60A. Each filament 146 is vertically centered on corresponding primary opening 64 and thus on the location of corresponding removed sphere 46.

[0175] Primary layer 62A and spacers 140 are removed to produce the structure shown in Fig. 10e. Primary layer 62A can be removed before removing spacers 140, or vice-versa. Alternatively, when an etchant that etches both the spacer and primary materials is available, primary layer 62A and spacers 140 can be removed at the same time. In any case, the removal operation is performed with etchant that does not significantly attack gate layer 60A or precursor electron-emissive filaments 146. Gate openings 66 are thereby reopened. Since each reopened gate opening 66 and corresponding dielectric opening 146 were centered on corresponding primary opening 64, each filament 146 is vertically centered on corresponding gate opening 66.

[0176] Using gate layer 60A as an etch mask, insulating layer 44I is etched through gate openings 66 to form corresponding dielectric open spaces 148 around precursor electron-emissive filaments 146 as shown in Fig. 10f. Item 44J is the remainder of insulating layer 44I.

The etch can be performed in an isotropic manner, the situation illustrated in Fig. 10f. Alternatively, the etch can be performed in a partially or fully isotropic manner so that dielectric open spaces 148 undercut gate layer 60A. Open spaces 148 may extend partially or fully through insulating layer 44J. Fig. 10f illustrates the fully through situation.

[0177] An electropolishing/sharpening operation is performed on precursor electron-emissive filaments 146 to provide them with sharpened tips. See Fig. 10g. Items 146A are the sharpened remainders of precursor filaments 146. Once again, the electropolishing/sharpening operation is performed according to a technique of the type described in U.S. Patent 5,564,959.

[0178] The process of Figs. 3a - 3f and 10 can be modified in various ways. The front-end process sequence of Figs. 2a - 2d can be substituted for the front-end process sequence of Figs. 3a - 3f. Likewise, the front-end process sequence of Fig. 4 (either the version of Fig. 4g1 or the version of Fig. 4g2), accompanied by the removal of further layer 74A, can be substituted for the process sequence of Figs. 3a - 3f. The electropolishing/sharpening operation on precursor electron-emissive filaments 146 can be performed before creating dielectric open spaces 148.

[0179] In the final structure, each electron-emissive filament 146A is vertically centered on corresponding gate opening 66. Inasmuch as removed spheres 46 define the locations of gate openings 66, removes spheres 46 also define the locations of filaments 146A. The lateral area of each electron-emissive filament 146A is controlled by the diameter of corresponding removed sphere 46 and the lateral thickness of corresponding spacer 140. By suitable adjusting the sphere size and particle surface density along with the spacer thickness, filaments 146A can provide highly uniform electron-emission.

[0180] In the processes of Figs. 2 and 7, gate openings 54 and 122 have been described as being present in the gate material that remains after removal of spherical particles 46. However, gate openings 54 and 122 are actually created in gate layers 48A and 120A at the same time as the gate material is deposited. Similar comments apply to primary openings 64 in the process of Fig. 3 and to further openings 76 in the process sequence of Fig. 4.

[0181] Figs. 11a - 11h (collectively "Fig. 11") illustrate a process sequence in which spherical particles 46 are utilized to define gate openings in manufacturing a gated field-emission cathode according to the invention and in which spacer material is deposited into the gate openings before removing spheres 46. The starting point for the process sequence of Fig. 11 is structure 40/42/44 of Fig. 7a. Spheres 46 are deposited on top of insulating layer 44 as shown in Fig. 7b after which the gate material deposition is performed in a direction generally perpendicular to the upper surface of layer 44 to form gate layer 120A and excess gate material portions 120B. This results in the structure of Fig. 7c, repeated here as Fig. 11a. Gate openings 122 in gate layer 120 are expressly marked in Fig. 11a. The gate layer thickness in Fig. 11a is typically less than the gate layer thickness in the fabrication process of Fig. 7.

[0182] Suitably etchable spacer material, typically an electrical insulator, is deposited on top of the structure to form a spacer (or cover) layer 150A on gate layer 120A as indicated in Fig. 11b. Spacer layer 150A is situated in the space between spheres 46. The spacer material deposition is performed in such a way that annular portions 150B of spacer layer 150A are formed in gate openings 122 on insulating layer 44 below particles 46. Portions 150C of the spacer material accumulate simultaneously on gate material portions 120B situated on spheres 46. To avoid having excess spacer material portions 150C bridge to spacer layer 150A, the total thickness of layers 150A and 120A is normally less than the average radius of spheres 46.

[0183] The spacer material deposition is typically performed by a uniform non-collimated technique such as non-collimated sputtering (i.e., sputtering in which there is a substantial spread in the natural incident angle of the impinging atoms of the material being sputtered) or plasma-enhanced CVD. During non-collimated sputtering, the pressure is normally 10 - 100 millitorr. The non-collimated spacer material deposition can also be performed by an angled rotational technique such as angled rotational sputtering or angled rotational evaporation. In angled rotational deposition, the spacer material is deposited on insulating layer 44 at an angle considerably less than 90° relative to the upper surface of insulating layer 44 while rotating structure 40/42/44, relative to the source of the spacer material, about an axis generally perpendicular to the upper surface of layer 44. Although atoms of the impinging spacer material may instantaneously form a collimated beam during the angled rotational deposition, the angled rotation of structure 40/42/44 relative to the spacer material source causes the overall deposition to be non-collimated.

[0184] When the spacer material deposition is performed in a uniform non-collimated manner into the space below particles 46, the lateral thickness of annular spacer portions 150B--i.e., the radial distance that spacer layer 150A extends into the area vertically shadowed by spheres 46--can readily equal 20 - 80% of the average sphere radius and is typically slightly more than 50% of the average sphere radius.

[0185] Particles 46 are removed, again typically according to the technique utilized in the process of Fig. 2. During the removal of spheres 46, excess gate material portions 120B and excess spacer material portions 150C are simultaneously removed to produce the structure of Fig. 11c. Apertures 152 now extend through spacer layer 150A at the locations of removed spheres 46. Specifically, apertures 152 extend through annular spacer portions 150B situated in gate openings 122. Since particles 46 are largely spherical, apertures 152

are largely circular. Each aperture 152 is vertically centered on corresponding gate opening 122.

[0186] Using spacer layer 150A as an etch mask, insulating layer 44 is anisotropically etched through apertures 152 to form corresponding dielectric openings 154 through layer 44 down to lower non-insulating region 42. See Fig. 11d in which item 44K is the remainder of insulating layer 44. Because apertures 152 are centered on gate openings 122, each dielectric opening 154 is vertically centered on corresponding gate opening 122.

[0187] Electrically non-insulating emitter filament material is electrochemically deposited into composite openings (or apertures) 152/154 to form precursor filamentary electron-emissive elements 156 that contact lower non-insulating emitter region 42. Fig. 11e shows the resultant structure. Once again, the electrochemical filament deposition is typically performed in the manner generally described in U.S. Patent 5,564,959. Likewise, the emitter filament material is normally a metal such as nickel or platinum.

[0188] During the electrochemical filament deposition, the combination of insulating layer 44 and spacer layer 150A, including spacer portions 150B, encapsulates gate layer 120A (again except possibly along the lateral periphery of the structure) to prevent precursor electron-emissive filaments 156 from contacting gate layer 120A. Spacers 150B determine the lateral spacing between gate layer 120A and precursor filaments 156.

[0189] The electrochemical deposition is typically conducted for a time sufficiently long to overfill composite openings 152/154 but not long enough for electron-emissive filaments 156 to meet one another along the top of spacer layer 158. Consequently, each electron-emissive filament 156 has a cap portion 156A that protrudes out of composite opening 152/154. The overfilling again reduces the likelihood of creating electron-emissive filaments of significantly different type due to differences in the nucleation and growth of the filament material.

[0190] Spacer layer 150A, including spacer portions 150B, is removed. See Fig. 11f. The spacer material removal is preferably done with etchant that does not significantly attack either insulating layer 44K or gate layer 120A. As a result, the outer portions of gate openings 122 are re-opened. A wet chemical, or a plasma having an isotropic component, is typically used to perform the spacer material etch.

[0191] Using gate layer 120A as an etch mask, insulating layer 44K is etched through gate openings 122 in an undercutting, typically isotropic, manner to form corresponding dielectric open spaces 158 around electron-emissive filaments 156. See Fig. 11g. Item 44L is the remainder of insulating layer 44K. Dielectric open spaces 158 may extend partially or fully through insulating layer 44L. Fig. 11g illustrates the fully through case.

[0192] Precursor electron-emissive filaments 156 are processed to remove caps 156A and provide the remaining filamentary portions with sharpened tips that extend at least partially through gate openings 122. Fig. 11h shows the resultant structure in which sharpened electron-emissive filaments 156B are the remainders of filaments 156. Sharpened filaments 156B are typically created from precursor filaments 156 by the electropolishing/sharpening technique described above for creating sharpened filaments 116B in the process sequence of Fig. 5. Each electron-emissive filament 156B is thus vertically centered on corresponding gate opening 122.

[0193] The electropolishing/sharpening operation can be done after creating dielectric open spaces 158. The structure of Fig. 11h is again produced. Also, an anisotropic etch can be used to form open spaces 158 so that they do not significantly undercut gate layer 120A. Alternatively, the formation of open spaces 158 can be deleted. The technique employed in the process sequence of Fig. 9 to automatically terminate the electrochemical deposition of the filament material can be applied to the process of Fig. 11 in the same way that the filament deposition is automatically terminated in the process sequence of Fig. 9.

[0194] Inasmuch as (a) electron-emissive filaments 156B are vertically centered on gate openings 122 and (b) openings 122 are centered on removed spheres 46, the locations of filaments 156B are determined by spheres 46. The lateral area of filaments 156B is controlled by the diameter of spheres 46 and the lateral thickness of spacer portions 150B. Consequently, filaments 156B can provide highly uniform electron emission by suitably adjusting the sphere size, the sphere surface density, and the lateral thickness of spacers 150B.

[0195] The processes/process sequences of Figs. 5 - 7, 10, and 11 for manufacturing electron emitters having filamentary electron-emissive elements all entail depositing spacer material into the gate openings. However, gated electron emitters having electron-emissive filaments whose average diameter is considerably less than the average diameter of spheres 46 that define the filament locations can be fabricated without depositing spacer material into gate openings. Figs. 12a - 12i (collectively "Fig. 12") present an example of how a gated field-emission cathode is so manufactured in accordance with the invention.

[0196] In the process of Fig. 12, initial structure 40/42/44 is formed in substantially the same way as described above for the process of Fig. 2. See Fig. 12a which repeats Fig. 2a. Solid spherical particles 46 are likewise distributed across the top of insulating layer 44 according to the random, or largely random, technique utilized in the process of Fig. 2. Fig. 12b, which repeats Fig. 2b, illustrates the structure at this point.

[0197] Lower (or first) cover material is deposited on top of the structure to form a lower cover layer 160A on insulating layer 44 as shown in Fig. 12c. Lower cover layer 160A is located in the space between particles 44. The deposition of cover layer 160A is performed in such

a way that annular portions 160B of cover layer 160A are formed in the spaces below spheres 46 above layer 44. Portions 160C of the lower cover material accumulate simultaneously on the upper halves of spheres 46.

[0198] The deposition of the lower cover material is typically performed in substantially the same way as the spacer material deposition in the process of Fig. 11. The lower cover material is typically an electrical insulator. Alternatively, the lower cover material can be an electrical non-insulator, typically a metal such as chromium, nickel, molybdenum, titanium, or tungsten. In this case, part of cover layer 160A later forms part of the gate layer.

[0199] Upper (or second) cover material is deposited on top of the structure in a direction substantially perpendicular to the upper surface of insulating layer 44 to form an upper cover layer 162A on lower cover layer 160A in the space between spherical particles 46. See Fig. 12d. Very little (essentially none) of the upper cover material accumulates in the spaces below spheres 46 above lower cover material portions 160B. However, portions 162B of the upper cover material simultaneously accumulate on lower cover portions 160C. The total thickness of cover layers 160A and 162A is normally less than the average radius of spheres 46. This avoids having excess cover material portions 162B bridge to cover layer 162A.

[0200] Upper cover layer 162A normally forms at least part of the gate layer for the electron emitter. In that case, the upper cover material consists of electrically non-insulating gate material, typically a metal such as chromium, nickel, molybdenum, titanium, tungsten, or gold. Alternatively, the upper cover material can be an electrical insulator if lower cover layer 160A later becomes the gate layer.

[0201] Spherical particles 46 are now removed, once again typically according to the technique employed in the process of Fig. 2. In removing spheres 46, excess cover material portions 160C and 162B are simultaneously removed to produce the structure of Fig. 12e. Upper openings 164, which typically constitute gate openings, extend through upper cover layer 162A at the locations of removed spheres 46. Lower openings 166 similarly extend through lower cover layer 160A, specifically through cover portions 160B of layer 160A, at the locations of removed spheres 46. Each lower cover opening 166 is of smaller diameter than corresponding upper cover opening 164. Since particles 46 are largely spherical, both cover openings 164 and cover openings 166 are largely circular. Each lower opening 166 is centered on corresponding upper opening 164.

[0202] Using cover layers 160A and 162A as an etch mask, insulating layer 44 is anisotropically etched through cover openings 164 and 166 to form corresponding dielectric openings 168 through layer 44 down to lower non-insulating emitter region 42. See Fig. 12f. Item 44M is the remainder of insulating layer 44. Since each lower cover opening 166 is smaller than corresponding upper cover opening 164, the diameter of each dielectric opening 168 approximately equals the diameter of corresponding lower cover opening 166. Also, each dielectric opening 168 is vertically centered on corresponding cover opening 164.

[0203] Electrically non-insulating emitter filament material is electrochemically deposited into composite openings (or apertures) 166/168 to form precursor electron-emissive filaments 170 that contact lower non-insulating emitter region 42. See Fig. 12g. The deposition time is sufficiently long to completely fill dielectric openings 168 but not so long that any of filaments 170 contact upper cover layer 162A. The filament deposition can be terminated automatically in the manner described above for the process sequence of Fig. 9. Once again, the filament material normally is a metal such as nickel or platinum.

[0204] Using upper cover 162A as an etch mask, lower cover layer 160A is etched through upper cover openings 164 to remove annular cover portions 160B. Lower cover openings 166 are thereby widened to become lower cover openings 172 as shown in Fig. 12h. Item 160D is the remainder of lower cover layer 160A. The etch is typically performed in an anisotropic manner so that widened lower cover openings 172 do not undercut upper cover layer 162A.

[0205] Using cover layers 162A and 160D as an etch mask, insulating layer 44M is anisotropically etched through cover openings 164 and 172 to form corresponding dielectric open spaces 174 down to lower non-insulating region 42. Again, see Fig. 12h. Item 44N is the remainder of insulating layer 44M. Dielectric open spaces 174 may extend partially or fully through insulating layer 44N, Fig. 12h depicting the fully through case.

[0206] An electropolishing/sharpening operation is performed on precursor filaments 170 to provide them with sharpened tips that extend partially through lower cover openings 172. The resultant structure is shown in Fig. 12i. Electron-emissive filaments 170A are the sharpened remainders of precursor filaments 170. The electropolishing/sharpening operation is typically conducted in the manner described above for the process of Fig. 5.

[0207] In Fig. 12i, upper cover layer 162A is normally the gate layer. Alternatively, both upper cover layer 162A and lower cover layer 160D can serve together as the gate layer. As yet another alternative, lower cover layer 160D can be the gate layer. In this case, upper cover layer 162A typically consists either of electrically insulating material or is removed.

[0208] The electropolishing/sharpening operation can be done before creating dielectric open spaces 174. An etch having an isotropic component can be used to form open spaces 174 so that they undercut cover layers 160D and 162A. The formation of open spaces 174 can be deleted. Sharpened filaments 170A then laterally abut insulating layer 44M.

[0209] Regardless of how, when, and if dielectric open

spaces 174 are created and regardless of whether the gate layer is formed with one or both of cover layers 162A and 160D, each electron-emissive filament 170A is vertically centered on both corresponding upper cover opening 164 and corresponding lower cover opening 172. Since upper cover openings 164 are situated at the locations of removed spheres 46, the locations of filaments 170A are determined by spheres 46. The lateral area occupied by filaments 170A is controlled by the diameter of spheres 46 and the lateral width of annular cover material portions 160B. Appropriately adjusting the sphere size, the sphere surface density, and the lateral thickness of annular cover portions 160B enables the electron emitter of Fig. 12i to achieve highly uniform electron emission.

[0210] In the foregoing processes/process sequences, spherical particles 46 are utilized to directly define gate openings or to directly define openings utilized to define gate openings. Particles 46 can, however, be employed to first define solid regions that have the desired lateral shapes for the gate openings. These solid regions, normally circular, are then used to define the gate openings.

[0211] Figs. 13a - 13g (collectively "Fig. 13") illustrate an example of the front-end portion of such a fabrication process in which the gate openings for a gated field-emission cathode are created from solid regions whose shapes are defined by spherical particles 46 in accordance with the invention. The so-created gate openings normally have abrupt edges.

Consequently, the front-end process sequence of Fig. 13 is particularly suitable for being completed according to a back-end process sequence, such as that of Figs. 7e - 7j, in which formation of the electron-emissive elements entails providing spacer material in the gate openings. The process sequence of Fig. 13 begins with structure 40/42/44 of Fig. 2a, repeated here as Fig. 13a.

[0212] An electrically non-insulating intermediate layer 180, which later serves as a lower part of the gate layer, is deposited on insulating layer 44 as shown in Fig. 13b. Intermediate non-insulating layer 180 typically consists of a metal such as chromium or titanium. A pattern-transfer layer 182 is formed on intermediate layer 180. Pattern-transfer layer 182 may consist of various materials such as photoresist or inorganic dielectric material.

[0213] Particles 46 are distributed across the upper surface of pattern-transfer layer 182 using the random, or largely random, technique described above for the process of Fig. 2. Fig. 13c illustrates the structure at this point. The portion of pattern-transfer layer 182 not shadowed--i.e., not vertically covered--by particles 46 is removed as shown in Fig. 13d. Generally circular pedestals 182A are thereby formed as the remainder of layer 182. Each pedestal 182A underlies a corresponding one of particles 46.

[0214] When pattern-transfer layer 182 consists of photoresist, layer 182 is exposed to actinic radiation, typically ultraviolet light, using spherical particles 46 as an exposure mask to prevent the photoresist portions below particles 46 from being subjected to the actinic radiation. The exposed photoresist changes chemical composition. A development operation is then performed on the structure to remove the exposed photoresist, leading to the structure depicted in Fig. 13d. When layer 182 exists of inorganic dielectric material, on anisotropic etch is performed on layer 182 in a direction generally perpendicular to the upper surface of insulating layer 44 using particles 46 as an etch mask. The non-shadowed portion of layer 182 is removed during the etch, again leading to the structure of Fig. 13d.

[0215] Electrically non-insulating gate material is deposited on top of the structure. The gate material deposition is preferably done by an electrochemical technique using non-insulating intermediate layer 180 as the.deposition cathode. A deposition anode is situated in the deposition electrolyte above particles 46. During the electrochemical deposition, gate material accumulates on the exposed part of intermediate layer 180 to form an electrically non-insulating upper gate sublayer 184 as depicted in Fig. 13e.

[0216] Pedestals 182A and particles 46 are removed to produce the structure of Fig. 13f. Upper gate openings 186 extend through upper gate sublayer 184 at the locations of removed pedestals 182A below particles 46. The removal of pedestals 182A and particles 46 can be performed in various ways. For example, pedestals 182A can be removed with a suitable chemical or plasma etchant, thereby simultaneously removing particles 46. Alternatively, particles 46 can be removed after which pedestals 182A are removed.

[0217] Using upper gate sublayer 184 as an etch mask, non-insulating intermediate layer 180 is anisotropically etched through upper gate openings 186 to form corresponding intermediate openings 188 through intermediate layer 180 down to insulating layer 44. See Fig. 13g. Each intermediate opening 188 is vertically concentric with, and of substantially the same diameter as, overlying upper gate opening 186. The remainder 180A of intermediate layer 180 is now a lower gate sublayer, intermediate openings 188 thereby being lower gate openings. Accordingly, gate sublayers 180A and 184 constitute a composite gate layer in which each pair of corresponding gate openings 186 and 188 forms a composite gate opening.

[0218] Aside from the fact that the gate layer in the structure of Fig. 13g consists of sublayers 180A and 184 and except for associated labeling differences, the structure of Fig. 13g is substantially the same as the structure of Fig. 7d. Items 180A/184 and 186/188 in Fig. 13g respectively correspond to items 120A and 122 in Fig. 1d. Subject to these labeling differences, the structure of Fig. 13g can now be completed according to the spacer-based back-end process sequence of Figs. 7e - 7j.

[0219] Alternatively, using gate layer 180A/184 as an

etch mask, insulating layer 44 can be etched through gate openings 186/188 to form corresponding dielectric open spaces through layer 44 down to lower non-insulating region 42. Spacer material, typically an electrical insulator, can be conformally deposited on top of the structure and into the dielectric open spaces so as to leave depressions, similar to depressions 104 in Fig. 5c, in the spacer material in the dielectric open spaces. Spacer material at the bottoms of the dielectric open spaces is removed to convert the depressions into apertures that extend down to non-insulating region 42 after which filamentary-electron-emission elements are formed in the apertures. By appropriately adjusting the sphere size, the sphere surface density, and the thickness of the spacer material, the resultant electron-emitting device can provide highly uniform electron emission.

[0220] In each of the electron emitters that have filamentary electron-emissive elements such as filaments 106B, 116B, 130A, 134A, 146A, 156B, or 170A, the gate layer such as gate layer 60B, 120A, or 162A may be patterned into column electrode lines running perpendicular to the emitter row electrodes of lower non-insulating region 42 in the same manner that the gate layer is patterned in the above-mentioned processes that yield conical electron-emissive elements. With suitable patterning being applied to the gate layer of each field emitter that has electron-emissive filaments, the field emitter may alternatively be provided with separate column electrodes that contact portions of the gate layer and run perpendicular to the row electrodes as described above for the electron emitters having electron-emissive cones.

[0221] Electron-emissive elements 106B, 116B, 130A, 134A, 146A, 156B, and 170A are true filaments for which the ratio of length to maximum diameter is at least 2 and normally at least 3. The length-to-maximum-diameter ratio is preferably 5 or more. The portions of filaments 106B, 116B, 130A, 134A, 146A, 156B, and 170A below their tips are typically cylinders of circular transverse cross-sections. Nonetheless, the transverse cross-section can be slightly non-circular. In any case, the ratio of maximum diameter to minimum diameter for each filament 106B, 116B, 130A, 134A, 146A, 156B, or 170A is usually no more than 2.

Variations and Exemplary Applications

[0222] Fig. 14 illustrates the starting point for manufacturing implementations of the present field emitter in which lower non-insulating emitter region 42 consists of an electrically conductive layer 42A situated under an electrically resistive layer 42B. Conductive layer 42A normally consists of a metal such as nickel or chromium. Resistive layer 42B is typically formed with cermet, lightly doped polycrystalline silicon, or a silicon-carbon-nitrogen compound.

[0223] When conductive layer 42A is patterned into a number of parallel emitter row electrodes, resistive layer 42B may be patterned into the same number of resistive lines, each overlying a corresponding one of the row electrodes. Alternatively, resistive layer 42B may be a blanket (continuous) layer even though conductive layer 42A is patterned into parallel lines.

[0224] Figs. 15.1 and 15.2 respectively depict how the final structures of Figs. 2g and 5g appear when lower non-insulating region 42 consists of conductive layer 42A and resistive layer 42B. The lower ends of electron-emissive elements 58A and 106B contact resistive layer 42B. The resistance between each electron-emissive element and conductive layer 42A is at least 10^6 ohms, typically 10^8 ohms or more.

[0225] Fig. 16 depicts a typical example of the core active region of a flat-panel CRT display that employs an area field emitter manufactured according to the invention. Substrate 40 forms the backplate for the CRT display. Lower non-insulating region 42 is situated along the interior surface of backplate 40 and here consists of conductive layer 42A and overlying resistive layer 42B. Conductive layer 42A is divided into emitter-electrode lines (row electrodes) extending laterally parallel to the plane of Fig. 16.

[0226] A group of column electrodes 190, one of which is depicted in Fig. 16, are situated on the gate layer, here shown, for example, as gate layer 60B in the field emitter of Fig. 5g. Column electrodes 190 run perpendicular to the plane of Fig. 16. Column-electrode openings 192, one of which is likewise shown in Fig. 16, extend through column electrodes 190 down to the gate layer. Each column-electrode opening 192 exposes a multiplicity of the electron-emissive elements, here shown as electron-emissive filaments 106B in the field emitter of Fig. 5g.

[0227] A transparent, typically glass, faceplate 194 is located across from baseplate 40. Light-emitting phosphor regions 196, one of which is shown in Fig. 16, are situated on the interior surface of faceplate 194 directly across from corresponding column-electrode openings 192. A thin electrically conductive light-reflective layer 198, typically aluminum, overlies phosphor regions 196 along the interior surface of faceplate 194. Electrons emitted by the electron-emissive elements pass through light-reflective layer 198 and cause phosphor regions 196 to emit light that produces an image visible on the exterior surface of faceplate 194.

[0228] The core active region of the flat-panel CRT display typically includes other components not shown in Fig. 16. For example, a black matrix situated along the interior surface of faceplate 194 typically surrounds each phosphor region 196 to laterally separate it from other phosphor regions 196. Focusing ridges provided over the interelectrode dielectric layer help control the electron trajectories. Spacer walls are utilized to maintain a relatively constant spacing between backplate 40 and faceplate 194.

[0229] When incorporated into a flat-panel display of

the type illustrated in Fig. 16, a field emitter manufactured according to the invention operates in the following way. Light-reflective layer 198 serves as an anode for the field-emission cathode. The anode is maintained at high positive voltage relative to the gate and emitter lines.

[0230] When a suitable voltage is applied between (a) a selected one of the emitter row electrodes in lower non-insulating emitter region 42 and (b) a selected one of the column electrodes that are formed with or contact portions of the gate layer, the so-selected gate portion extracts electrons from the electron-emissive elements at the intersection of the two selected electrodes and controls the magnitude of the resulting electron current. Desired levels of electron emission typically occur when the applied gate-to-emitter parallel-plate electric field reaches 20 volts/μm or less at a current density of 1 mA/cm^2 as measured at the phosphor-coated faceplate of the flat-panel display when phosphor regions 196 are high-voltage phosphors. Upon being hit by the extracted electrons, the phosphor regions emit light.

[0231] Directional terms such as "upper", "lower", "down", and the like have been employed in describing the present invention to establish a frame of reference by which the reader can more easily understand how the various parts of the invention fit together. In actual practice, the components of an electron-emitting device may be situated at orientations different from that implied by the directional terms used here. The same applies to the way in which the fabrication steps are performed in the invention. Inasmuch as directional terms are used for convenience to facilitate the description, the invention encompasses implementations in which the orientations differ from those strictly covered by the directional terms employed here.

[0232] While the invention has been described with reference to particular embodiments, this description is solely for the purpose of illustration and is not to be construed as limiting the scope of the invention claimed below. For example, when spherical particles 46 consist of glass rather than polystyrene, higher processing temperatures can be employed during the steps extending from the deposition of particles 46 to their removal. The distribution of particles 46 across the interelectrode dielectric layer, the gate layer, or the primary layer can be performed electrophoretically or dielectrophoretically, typically according to the techniques described in Haven et al, co-filed International Patent Application PCT/US97/09197. An electropolishing operation can be conducted to round the edges of the gate layer at the gate openings.

[0233] One or more thin intermediate layers that perform various functions may be provided between insulating layer 44 and the gate layer. Such an intermediate layer may provide an adhesion function--i.e. the intermediate layer adheres well to both interelectrode dielectric 44 and the gate layer when the gate material does not itself adhere well to the interelectrode dielectric material. The intermediate layer is then subjected to processing steps akin to those applied to the gate layer, including the formation of intermediate openings corresponding to the gate openings.

[0234] A transparent electrically non-insulating layer situated between faceplate 194 and phosphors 196 and consisting, for example, of indium-tin oxide can be used as the anode in place of light-reflective layer 198. Substrate 40 can be deleted if lower non-insulating region 42 is a continuous layer of sufficient thickness to support the structure. Insulating substrate 40 can be replaced with a composite substrate in which a thin insulating layer overlies a relatively thick non-insulating layer that furnishes structural support.

[0235] In manufacturing large-area gated electron emitters, substrate 40 may be in the shape of a rectangular plate rather than a circular wafer which, after the formation of the electron-emissive elements, is cut into one or more rectangular plates. The electron-emissive elements can have shapes other than cones and filaments.

[0236] After creating a structure in which gate openings extend through a gate layer down to insulating layer 44 above lower non-insulating emitter region 42, the thickness of the gate layer can be increased by selectively depositing further electrically non-insulating gate material on the gate layer. The further gate material deposition can be performed by an electrochemical technique. In general, the further gate material deposition can be performed before or after removing particles 46.

[0237] The deposition termination technique described in conjunction with Fig. 9 can be employed to automatically terminate the electrochemical deposition of electron-emissive filaments in area electron emitters where the filament locations are defined by mechanisms not involving spheres 46. For example, the automatic termination technique of Fig. 9 could be applied to filaments deposited in openings created by photolithographic etching techniques or in openings defined by charged-particle tracks as in Macaulay et al, U.S. Patent 5,462,467.

[0238] The area electron emitters produced according to the manufacturing processes of the invention can be employed to make flat-panel devices other than flat-panel CRT displays. In particular, the present electron emitters can be used in general vacuum environments that require gated electron sources. Various modifications and applications may thus be made by those skilled in the art without departing from the scope of the invention as defined in the appended claims.

Claims

1. A method of fabricating an electron-emitting device, the method.comprising the steps of:

distributing a multiplicity of particles (46) over a

structure;
utilizing the particles to define corresponding locations for (a) a like multiplicity of primary openings (52, 64, 78) extending through a primary layer (50A, 62A, 72) provided over an electrically non-insulating gate layer (48A, 60) formed over an electrically insulating layer (44) in the structure and (b) a like multiplicity of corresponding gate openings (54, 66, 80, 82) extending through the gate layer such that each gate opening is vertically aligned to the corresponding primary opening;
etching the insulating layer through the primary openings (52 or 64) and the gate openings (54, 66, 80) to form corresponding dielectric openings (56, 68) substantially through the insulating layer down to a lower electrically non-insulating region (42) provided below the insulating layer;
depositing electrically non-insulating emitter material over the primary layer (50A, 62A, 72), through the primary and gate openings, and into the dielectric openings to form corresponding electron-emissive elements (58A, 70A) over the lower non-insulating region; and
removing the primary layer so as to substantially remove any of the emitter material (58B, 70B) accumulated over the primary layer.

2. A method as in Claim 1 wherein the distributing step entails depositing the particles directly over one of the insulating layer (44), the gate layer (60), and the primary layer (72).

3. A method as in Claim 1 wherein the distributing step entails distributing the particles over the insulating layer (44), the utilizing step comprising:

providing electrically non-insulating gate material (48A, 48B) over the insulating layer at least in space between the particles;
providing primary material (50A, 50B) over the gate material at least in space between the particles; and
removing the particles and substantially any material (48B, 50B) overlying the particles such that (a) the remaining primary material (50A) forms the primary layer with the primary openings (52) extending therethrough and (b) the remaining gate material (48A) forms the gate layer with the gate openings (54) extending therethrough.

4. A method as in Claim 1 wherein the distributing step entails distributing the particles over the gate layer (60), the utilizing step comprising:

providing primary material (62A, 62B) over the gate layer at least in space between the particles;
removing the particles and substantially any material (62B) overlying the particles such that the remaining primary material (62A) forms the primary layer with the primary openings (64) extending therethrough; and
etching the gate layer through the primary openings to form the gate openings (66).

5. A method as in Claim 1 wherein the distributing step entails distributing the particles over the primary layer (72), the utilizing step comprising:

providing further material (74A, 74B) over the primary layer at least in space between the particles;
removing the particles and substantially any material (74B) overlying the particles such that further openings (76) extend through the remaining further material (74A) at the locations of the so-removed particles;
etching the primary layer through the further openings to form the primary openings (78); and
etching the gate layer through the primary openings to form the gate openings (80, 82).

6. A method as in any of Claims 1 - 5 wherein each primary opening is laterally substantially no larger than the corresponding gate opening.

7. A method as in any of Claims 1 - 6 wherein the primary layer comprises inorganic dielectric material.

8. A method as in any of Claims 1 - 7 wherein the gate layer comprises metal through which it is difficult to accurately etch small openings.

9. A method as in Claim 8 wherein the gate layer comprises gold.

10. A method as in any of Claims 1 - 9 wherein the electron-emissive elements are formed generally in the shape of cones.

11. A method as in any of Claims 1-9 wherein the electron-emissive elements are formed generally in the shape of filaments.

12. A method as in any of Claims 1 - 11 wherein the particles are largely spherical.

13. A method as in any of Claims 1 - 12 wherein the electron-emissive elements are of substantially the same size.

14. A method as in any of Claims 1 - 13 wherein the

electron-emissive elements operate in field-emission mode.

15. A method as in any of Claims 1 - 14 further including the step of providing anode means (194, 196, 198) above, and spaced apart from, the electron-emissive elements for collecting electrons emitted by the electron-emissive elements.

16. A method as in Claim 15 wherein the anode means is provided as part of a light-emitting structure having light-emissive elements (196) for emitting light upon being struck by electrons emitted from the electron-emissive elements.

Patentansprüche

1. Verfahren zum Herstellen einer elektronenemittierenden Vorrichtung, welches Verfahren die Schritte umfasst:

Verteilen einer Vielzahl von Partikeln (46) über einer Struktur;

Nutzen der Partikel zur Festlegung entsprechender Stellen für (a) eine ähnliche Vielzahl von primären Öffnungen (52, 64, 78), die sich durch eine primäre Schicht (50A, 62A, 72) hindurch erstrecken, die über einer elektrisch nichtisolierenden Gatterschicht (48A, 60) vorgesehen wird und die über einer elektrisch isolierenden Schicht (44) in der Struktur erzeugt ist; und (b) eine ähnliche Vielzahl von entsprechenden Gatteröffnungen (54, 66, 80, 82), die sich durch die Gatterschicht derart erstrecken, dass jede Gatteröffnung vertikal mit der entsprechenden primären Öffnung ausgerichtet ist;

Ätzen der isolierenden Schicht durch die primären Öffnungen (52 oder 64) und der Gatteröffnungen (54, 66, 80) hindurch, um entsprechende dielektrische Öffnungen (56, 68) zu erzeugen, die im Wesentlichen durch die isolierende Schicht nach unten zu dem elektrisch nichtisolierenden Bereich (42) hindurch gehen, der unterhalb der isolierenden Schicht vorgesehen ist;

Abscheiden von elektrisch nichtisolierendem Emittermaterial über der primären Schicht (50A, 62A, 72) durch die primären und Gatteröffnungen hindurch und in die dielektrischen Öffnungen hinein, um entsprechende elektronemittierende fähige Elemente (58A, 70A) über den unteren nichtisolierenden Bereich zu erzeugen; und

Entfernen der primären Schicht, so dass im Wesentlichen sämtliches Emittermaterial (58B, 70B) entfernt wird, das sich über der primären Schicht angesammelt hat.

2. Verfahren nach Anspruch 1, bei welchem der Schritt des Verteilens das Abscheiden der Partikel direkt über einer der isolierenden Schichten (44), der Gatterschicht (60) und der primären Schicht (72) umfasst.

3. Verfahren nach Anspruch 1, bei welchem der Schritt des Verteilens das Verteilen der Partikel über der isolierenden Schicht (44) umfasst und der Schritt des Nutzens umfasst:

Bereitstellen von elektrisch nichtisolierendem Gattermaterial (48A, 48B) über der isolierenden Schicht mindestens in dem Raum zwischen den Partikeln;

Bereitstellen von primärem Material (48B, 50B) über dem Gattermaterial mindestens in dem Raum zwischen den Partikeln; sowie

Entfernen der Partikel und im Wesentlichen des gesamten Materials (48B, 50B), das über den Partikeln liegt, derart, dass (a) das verbleibende primäre Material (50A) die primäre Schicht mit den primären Öffnungen (52) erzeugt, die sich durch diese hindurch erstrekken, und (b) das verbleibende Gattermaterial (48A) die Gatterschicht mit den Gatteröffnungen (54) erzeugt, die sich durch diese hindurch erstrecken.

4. Verfahren nach Anspruch 1, bei welchem der Schritt das Verteilen der Partikel über der Gatterschicht (60) umfasst und der Schritt des Nutzens umfasst:

Bereitstellen von primärem Material (62A, 62B) über der Gatterschicht mindestens im Raum zwischen den Partikeln;

Entfernen der Partikel und im Wesentlichen des gesamten Materials (62B), das über den Partikeln liegt, derart, dass das verbleibende primäre Material (62A) die primäre Schicht mit den primären Öffnungen (64) erzeugt, die sich durch diese hindurch erstrecken; und

Ätzen der Gatterschicht durch die primären Öffnungen hindurch, um die Gatteröffnungen (66) zu erzeugen.

5. Verfahren nach Anspruch 1, bei welchem der Schritt des Verteilens das Verteilen der Partikel

über der primären Schicht (72) umfasst und der Schritt des Nutzens umfasst:

Bereitstellen von weiterem Material (74A, 74B) über der primären Schicht mindestens im Raum zwischen den Partikeln;

Entfernen der Partikel und im Wesentlichen des gesamten Materials (74B), das über den Partikeln liegt, derart, dass weitere Öffnungen (76) sich durch das verbleibende weitere Material (74A) an den Stellen der so entfernten Partikel erstrecken;

Ätzen der primären Schicht durch die weiteren Öffnungen, um die primären Öffnungen (78) zu erzeugen; und

Ätzen der Gatterschicht durch die primären Öffnungen, um die Gatteröffnungen (80, 82) zu erzeugen.

6. Verfahren nach einem der Ansprüche 1 bis 5, bei welchem jede primäre Öffnung lateral im Wesentlichen nicht größer ist als die entsprechende Gatteröffnung.

7. Verfahren nach einem der Ansprüche 1 bis 6, bei welchem die primäre Schicht anorganisches dielektrisches Material aufweist.

8. Verfahren nach einem der Ansprüche 1 bis 7, bei welchem die Gatterschicht Metall aufweist, durch das hindurch ein genaues Ätzen kleiner Öffnungen schwierig ist.

9. Verfahren nach Anspruch 8, bei welchem die Gatterschicht Gold aufweist.

10. Verfahren nach einem der Ansprüche 1 bis 9, bei welchem die zur Elektronenemission fähigen Elemente allgemein in Form von Kegeln erzeugt werden.

11. Verfahren nach einem der Ansprüche 1 bis 9, bei welchem die zur Elektronenemission fähigen Elemente allgemein in Form von Filamenten erzeugt werden.

12. Verfahren nach einem der Ansprüche 1 bis 11, bei welchem die Partikel größtenteils kugelförmig sind.

13. Verfahren nach einem der Ansprüche 1 bis 12, bei welchem die zur Elektronenemission fähigen Elemente weitgehend die gleiche Größe haben.

14. Verfahren nach einem der Ansprüche 1 bis 13, bei welchem die zur Elektronenemission fähigen Elemente im Feldemissionsmode betrieben werden.

15. Verfahren nach einem der Ansprüche 1 bis 14, ferner einschließend den Schritt des Bereitstellens einer Anodenvorrichtung (194, 196, 198) oberhalb und beabstandet von den zur Elektronenemission fähigen Elementen zum Aufnehmen von Elektronen, die durch die zur Elektronenemission fähigen Elemente emittiert werden.

16. Verfahren nach Anspruch 15, bei welchem die Anodenvorrichtung als ein Teil einer lichtemittierenden Struktur bereitgestellt wird, die über zur Lichtemission fähige Elemente (196) zum emittieren von Licht beim Auftreffen von Elektronen in der Lage ist, die von den zur Elektronenemission fähigen Elementen emittiert werden.

Revendications

1. Méthode de fabrication d'un dispositif émetteur d'électrons, la méthode comprenant les étapes de:

distribuer une multiplicité de particules (46) sur une structure;
utiliser les particules pour définir des emplacements correspondants pour (a) une multiplicité identique d'ouvertures primaires (52, 64, 78) s'étendant à travers une couche primaire (50A, 62A, 72) prévue sur une couche de porte non électriquement isolante (48A, 60) formée sur une couche électriquement isolante (44) dans la structure et (b) une multiplicité identique d'ouvertures correspondantes de porte (54, 66, 80, 82) s'étendant à travers la couche de porte de façon que chaque ouverture de porte soit verticalement alignée avec l'ouverture primaire correspondante;
attaquer la couche isolante à travers les ouvertures primaires (52 ou 64) et les ouvertures de porte (54, 66, 80) pour former des ouvertures diélectriques correspondantes (56, 68) sensiblement à travers la couche isolante jusqu'à une région électriquement non isolante inférieure (42) prévue en dessous de la couche isolante;
déposer un matériau d'émetteur électriquement non isolant sur la couche primaire (50A, 62A, 72) à travers les ouvertures primaires et de porte et dans les ouvertures diélectriques pour former des éléments émetteurs d'électrons correspondants (58A, 70A) sur la région non isolante inférieure; et
éliminer la couche primaire afin d'éliminer sensiblement tout le matériau émetteur (58B, 70B) accumulé sur la couche primaire.

2. Méthode selon la revendication 1, où l'étape de distribution consiste à déposer les particules directement sur l'une de la couche isolante (44), la couche de porte (60), et la couche primaire (72).

3. Méthode selon la revendication 1, où l'étape de distribution consiste à distribuer les particules sur la couche isolante (44), l'étape d'utilisation consistant à:

prévoir un matériau de porte électriquement non isolant (48A, 48B) sur la couche isolante au moins dans l'espace entre les particules;
prévoir un matériau primaire (50A, 50B) sur le matériau de porte au moins dans l'espace entre les particules; et
éliminer les particules et sensiblement tout matériau (48B, 50B) recouvrant les particules de façon que (a) le matériau primaire restant (50A) forme la couche primaire avec les ouvertures primaires (52) la traversant et (b) le matériau de porte restant (48A) forme la couche de porte avec des ouvertures de portes (58) la traversant.

4. Méthode selon la revendication 1, où l'étape de distribution consiste à distribuer les particules sur la couche de porte (60), l'étape d'utilisation consistant à:

prévoir un matériau primaire (62A, 62B) sur la couche de porte au moins dans l'espace entre les particules;
éliminer les particules et sensiblement tout matériau (62B) recouvrant les particules de façon que le matériau primaire restant (62A) forme la couche primaire avec les ouvertures primaires (64) la traversant; et
attaquer la couche de porte à travers les ouvertures primaires pour former les ouvertures de porte (66).

5. Méthode selon la revendication 1, où l'étape de distribution consiste à distribuer les particules sur la couche primaire (72), l'étape d'utilisation consistant à:

prévoir d'autre matériau (74A, 74B) sur la couche primaire au moins dans l'espace entre les particules;
éliminer les particules et sensiblement tout matériau (74B) recouvrant les particules de façon que d'autres ouvertures (76) s'étendent à travers l'autre matériau restant (74A) aux emplacements des particules ainsi éliminées;
attaquer la couche primaire à travers les autres ouvertures pour former les ouvertures primaires (78); et
attaquer la couche de porte à travers les ouvertures primaires pour former les ouvertures de porte (80, 82).

6. Méthode selon l'une quelconque des revendications 1-5, où chaque ouverture primaire est latéralement sensiblement pas plus grande que l'ouverture de porte correspondante.

7. Méthode selon l'une quelconque des revendications 1-6, où la couche primaire comprend un matériau diélectrique inorganique.

8. Méthode selon l'une quelconque des revendications 1-7, où la couche de porte comprend un métal à travers lequel il est difficile d'attaquer avec précision des petites ouvertures.

9. Méthode selon la revendication 8, où la couche de porte comprend de l'or.

10. Méthode selon l'une quelconque des revendications 1-9, où les éléments émetteurs d'électrons sont fermés généralement sous la forme de cônes.

11. Méthode selon l'une quelconque des revendications 1-9, où les éléments émetteurs d'électrons sont formés généralement sous la forme de filaments.

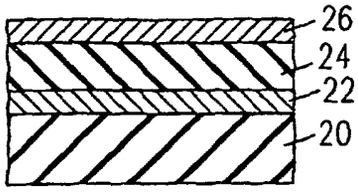
12. Méthode selon l'une quelconque des revendications 1-11, où les particules sont largement sphériques.

13. Méthode selon l'une quelconque des revendications 1-12, où les éléments émetteurs d'électrons sont sensiblement de la même dimension.

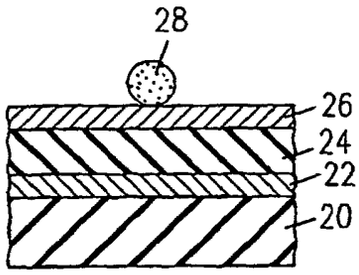
14. Méthode selon l'une quelconque des revendications 1-13, où les éléments émetteurs d'électrons fonctionnent en mode d'émission de champ.

15. Méthode selon l'une quelconque des revendications 1-14, comprenant de plus l'étape de prévoir un moyen formant anode (194, 196, 198) au-dessus et espacé des éléments émetteurs d'électrons pour collecter des électrons émis par les éléments émetteurs d'électrons.

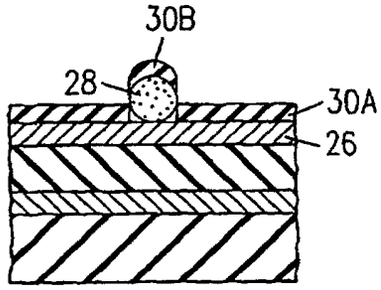
16. Méthode selon la revendication 15, où le moyen formant anode est prévu en tant que partie d'une structure photo-émettrice ayant des éléments photo-émetteurs (196) pour émettre de la lumière lorsqu'ils sont frappés par des électrons émis par les éléments émetteurs d'électrons.



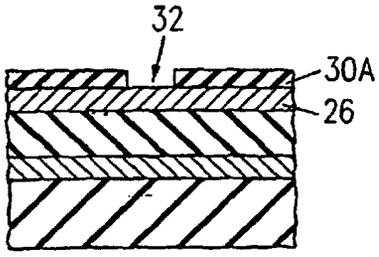
PRIOR ART
FIG. 1a



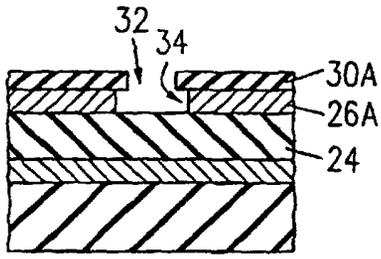
PRIOR ART
FIG. 1b



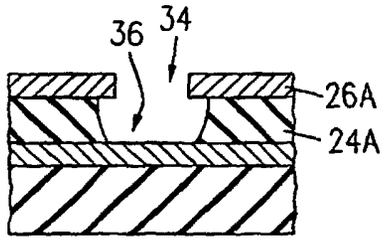
PRIOR ART
FIG. 1c



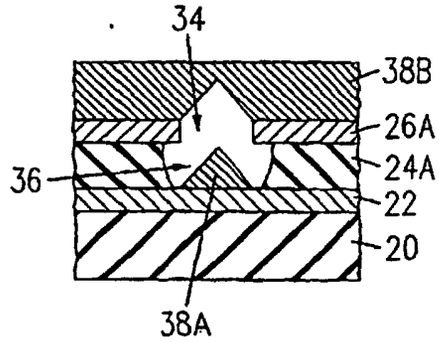
PRIOR ART
FIG. 1d



PRIOR ART
FIG. 1e



PRIOR ART
FIG. 1f



PRIOR ART
FIG. 1g

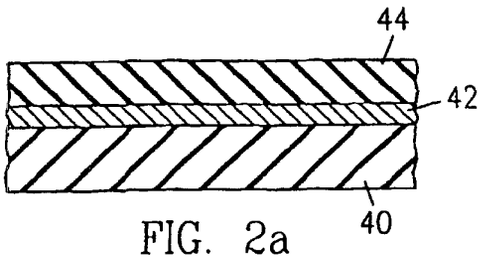


FIG. 2a

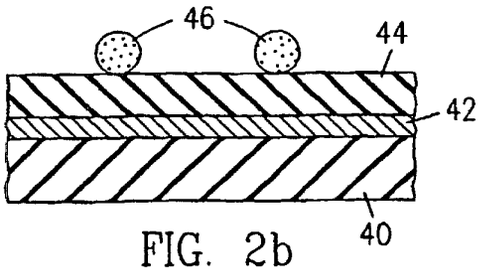


FIG. 2b

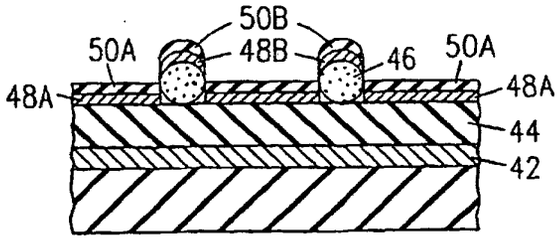


FIG. 2c

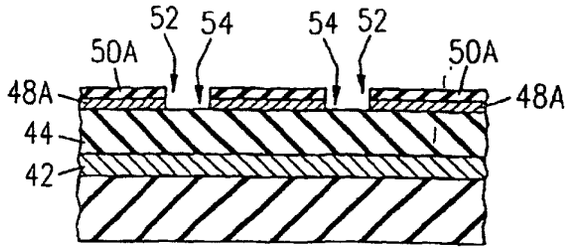


FIG. 2d

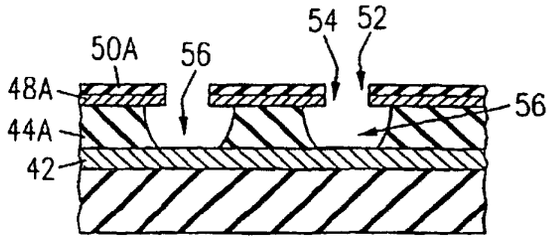


FIG. 2e

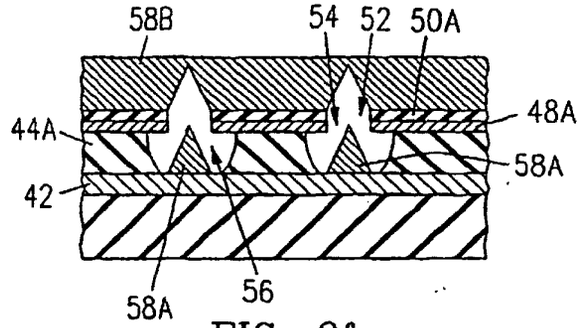


FIG. 2f

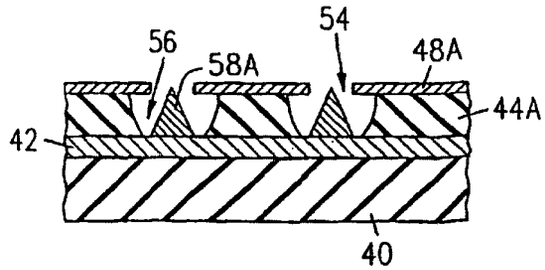


FIG. 2g

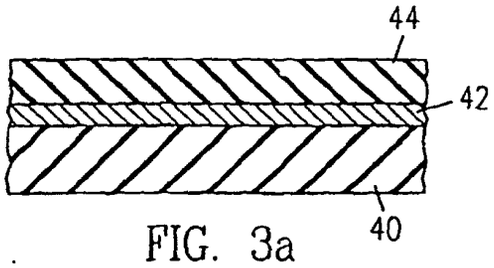


FIG. 3a

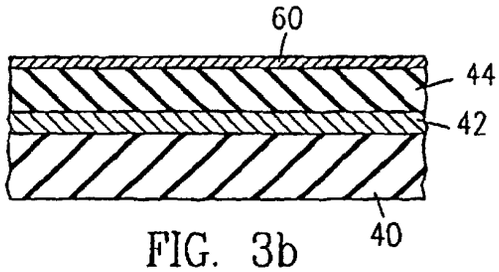


FIG. 3b

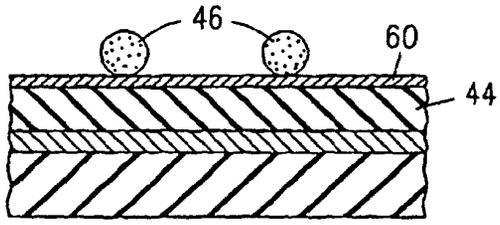


FIG. 3c

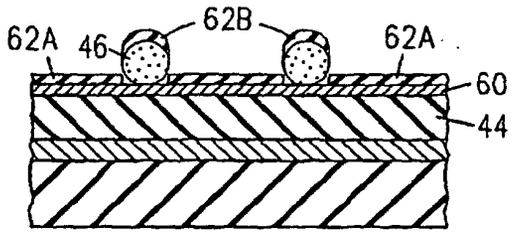


FIG. 3d

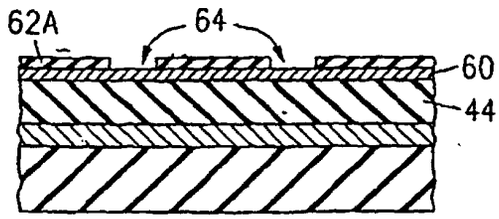


FIG. 3e

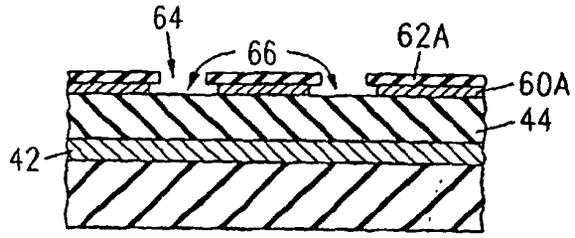


FIG. 3f

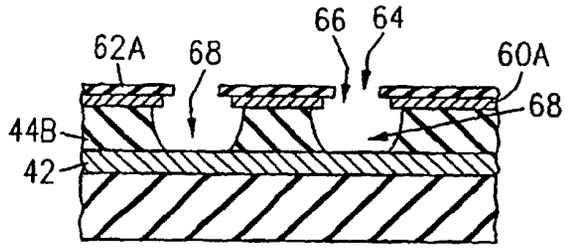


FIG. 3g

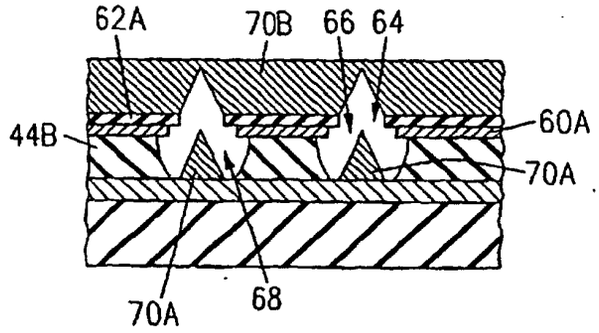


FIG. 3h

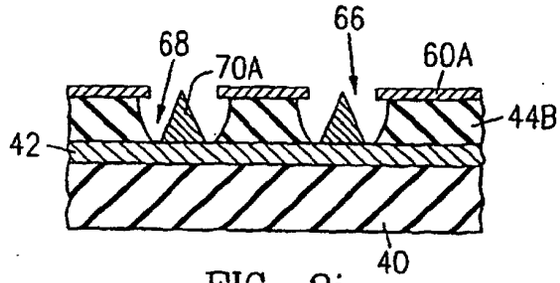


FIG. 3i

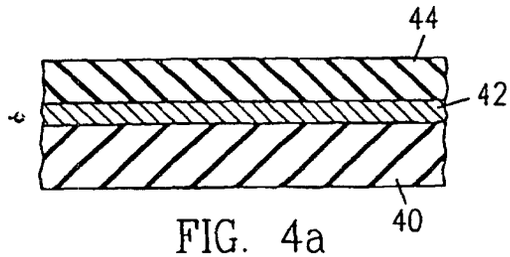


FIG. 4a

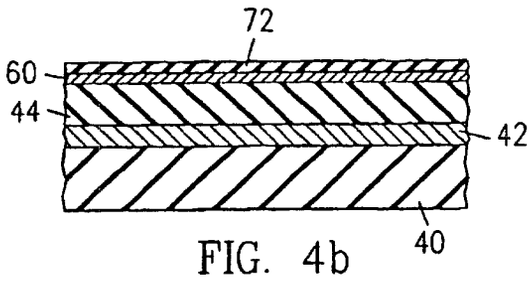


FIG. 4b

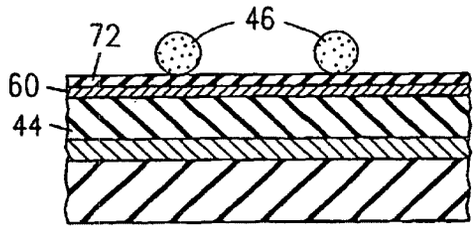


FIG. 4c

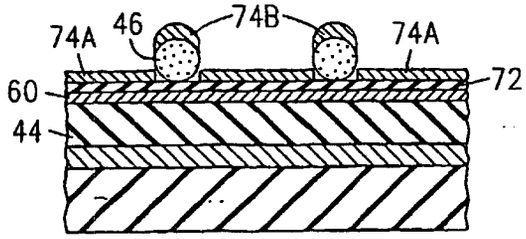


FIG. 4d

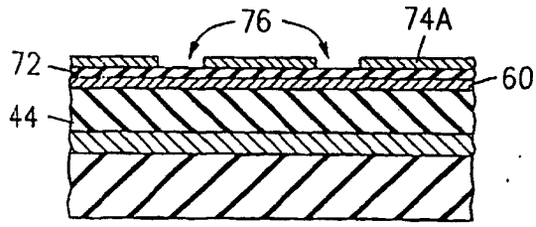


FIG. 4e

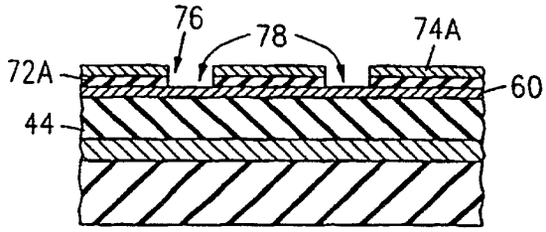


FIG. 4f

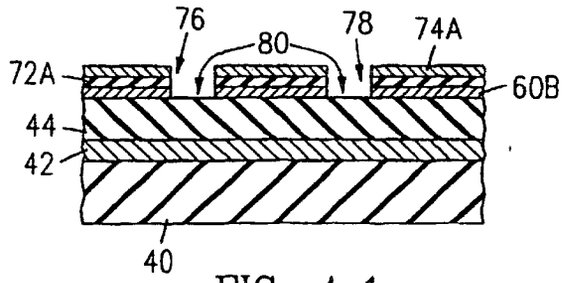


FIG. 4g1

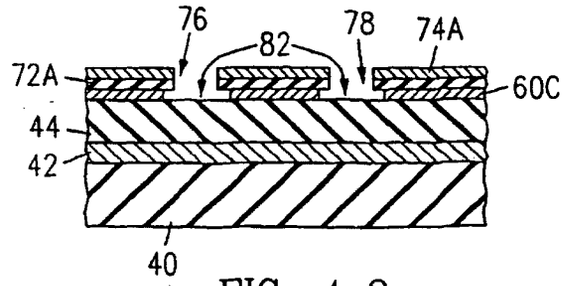


FIG. 4g2

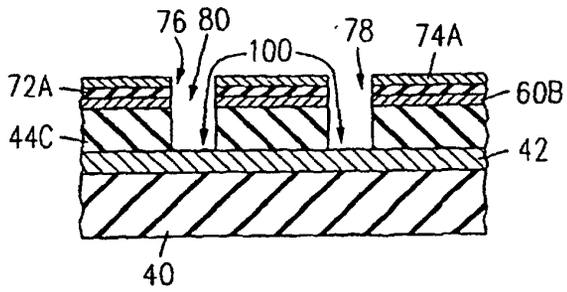


FIG. 5a

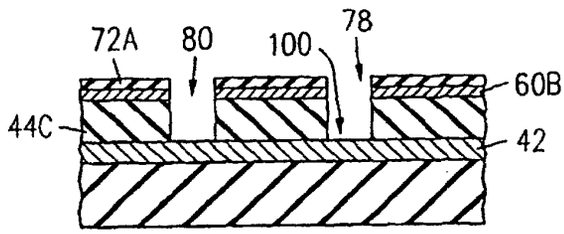


FIG. 5b

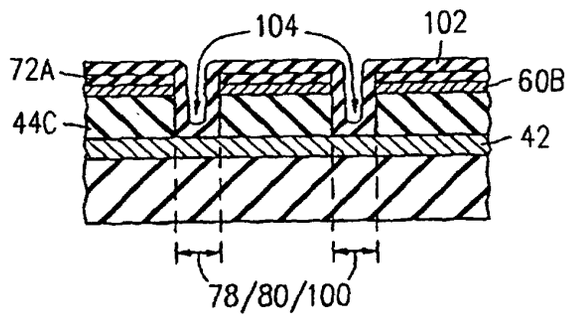


FIG. 5c

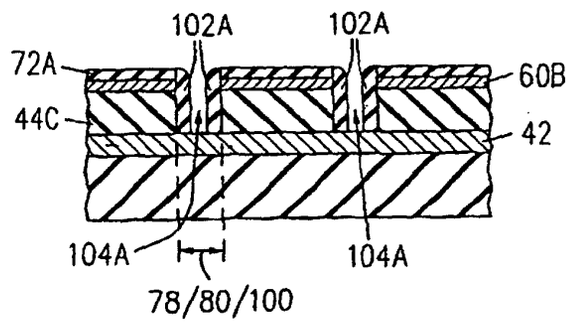


FIG. 5d

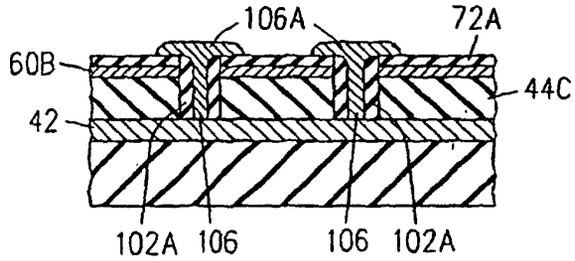


FIG. 5e

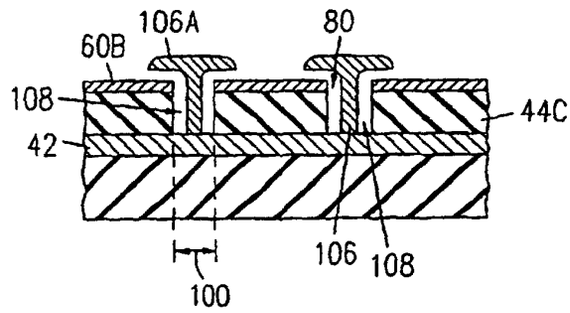


FIG. 5f

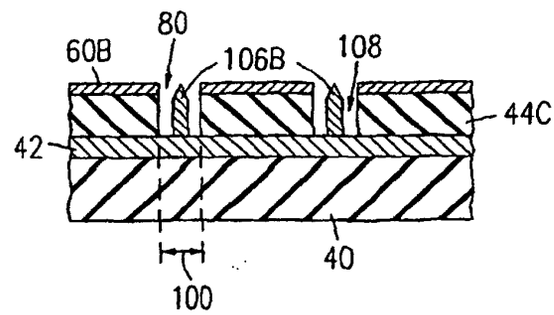


FIG. 5g

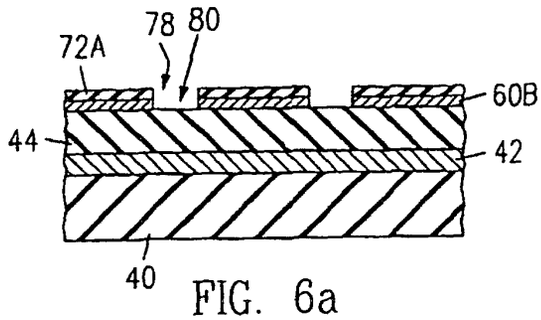


FIG. 6a

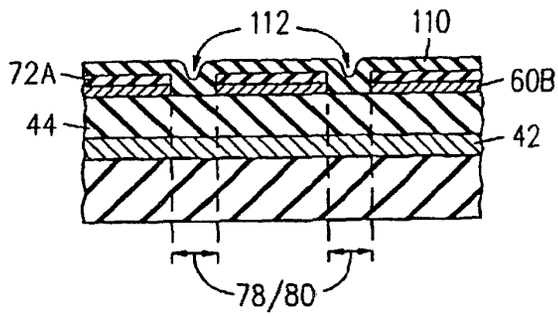


FIG. 6b

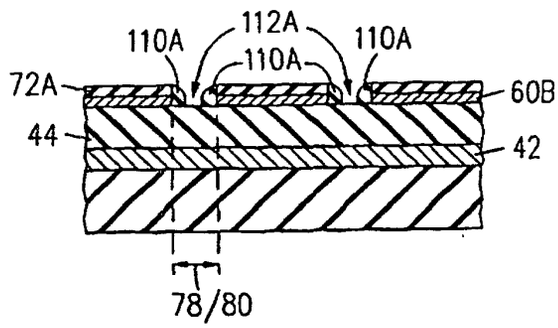


FIG. 6c

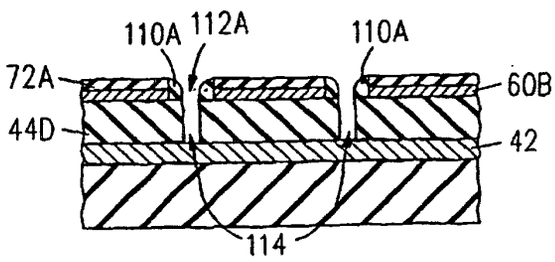


FIG. 6d

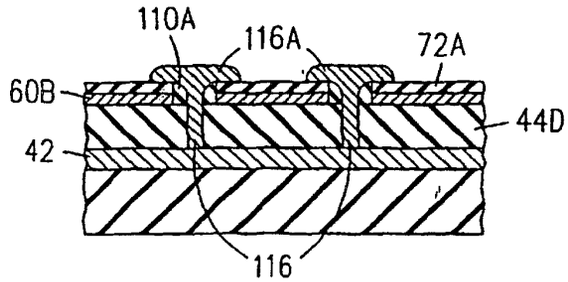


FIG. 6e

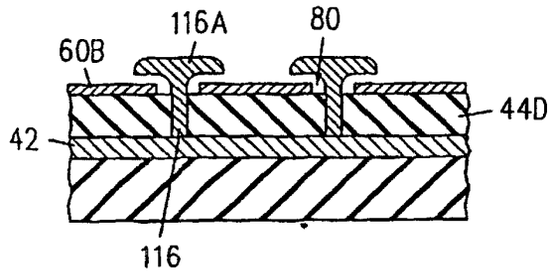


FIG. 6f

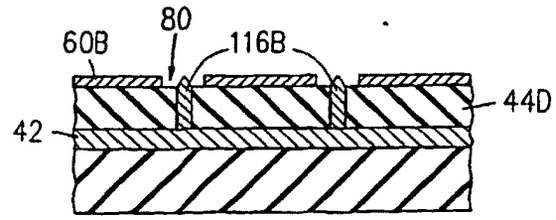


FIG. 6g

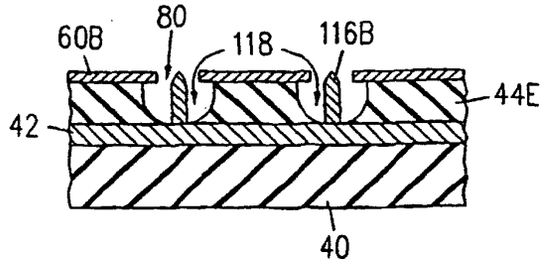


FIG. 6h

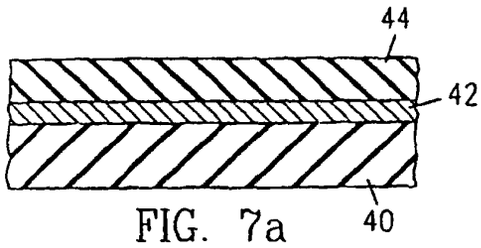


FIG. 7a

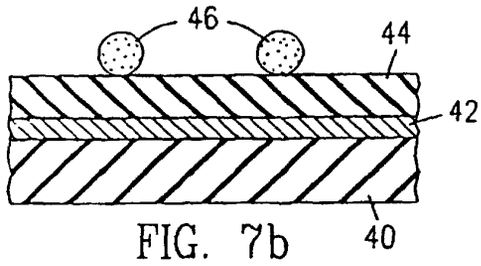


FIG. 7b

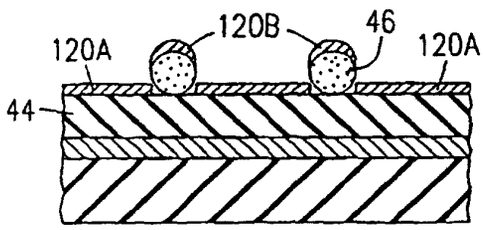


FIG. 7c

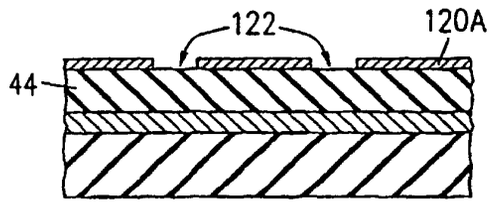


FIG. 7d

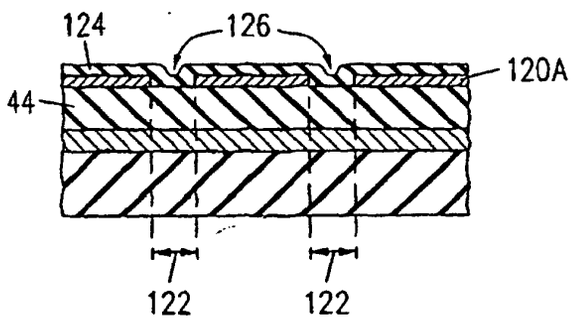


FIG. 7e

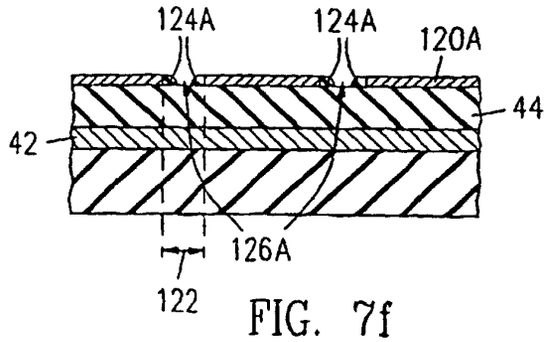


FIG. 7f

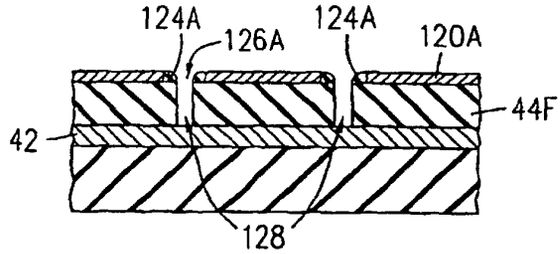


FIG. 7g

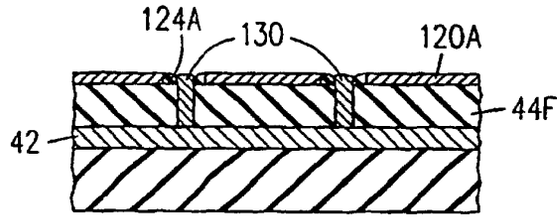


FIG. 7h

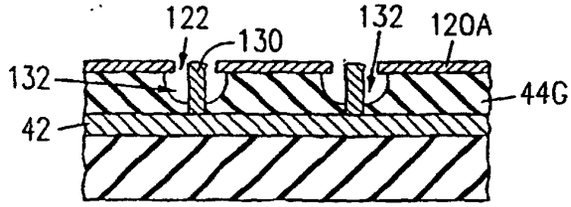


FIG. 7i

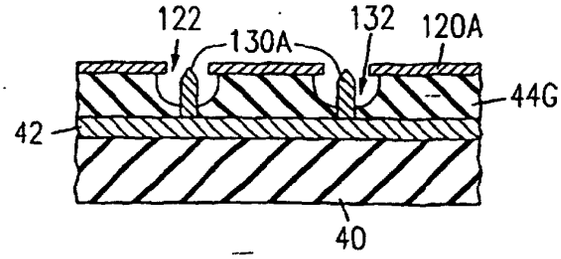


FIG. 7j

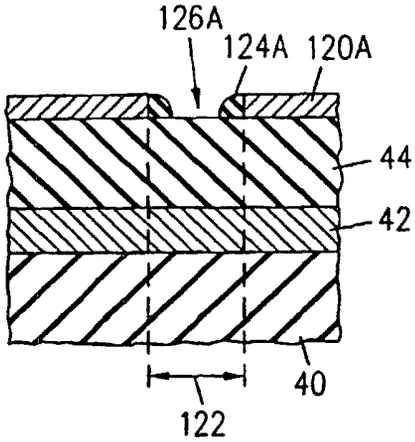


FIG. 8a

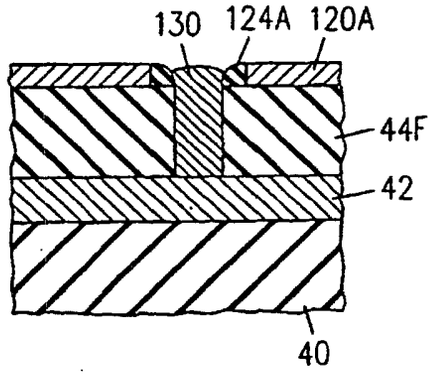


FIG. 8b

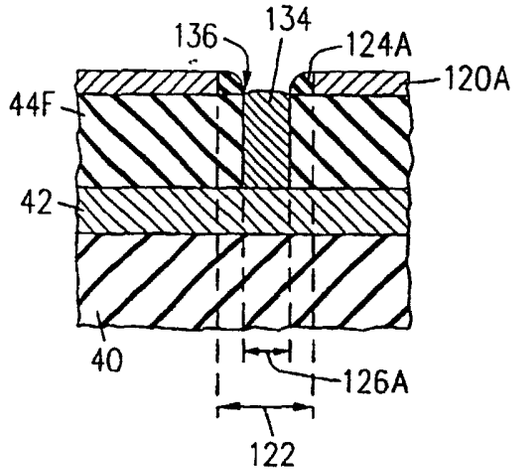


FIG. 9a

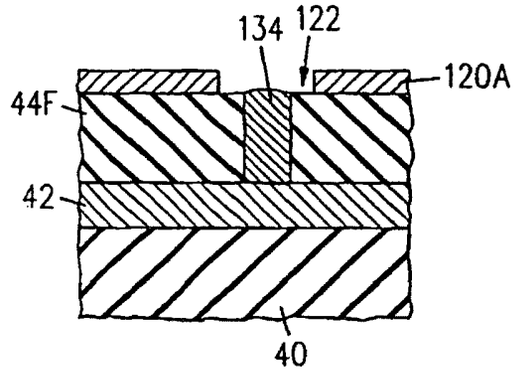


FIG. 9b

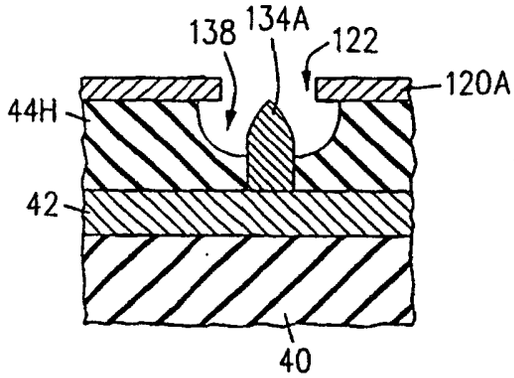


FIG. 9c

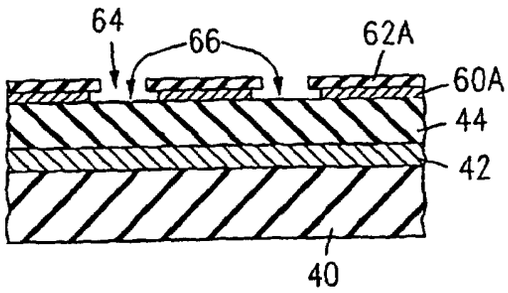


FIG. 10a

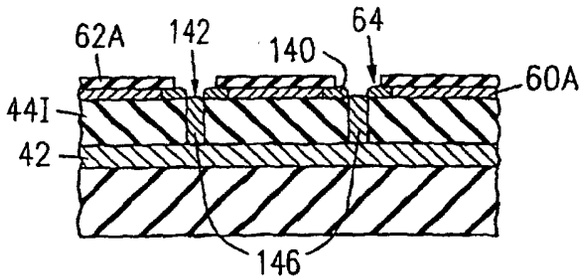


FIG. 10d

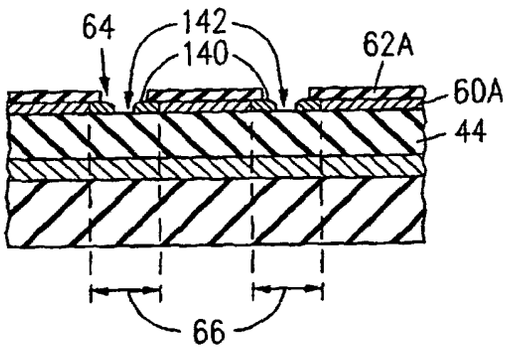


FIG. 10b

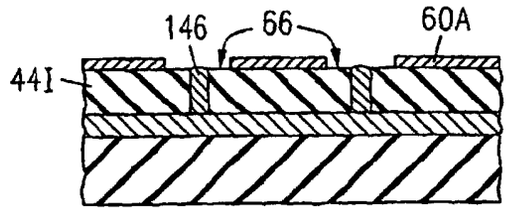


FIG. 10e

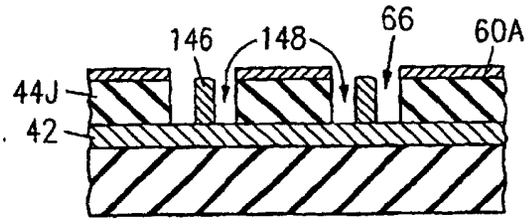


FIG. 10f

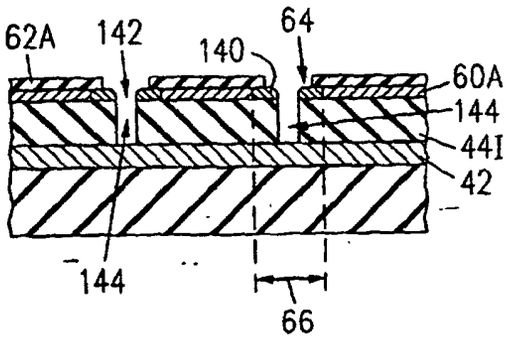


FIG. 10c

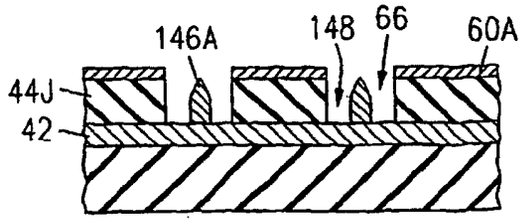


FIG. 10g

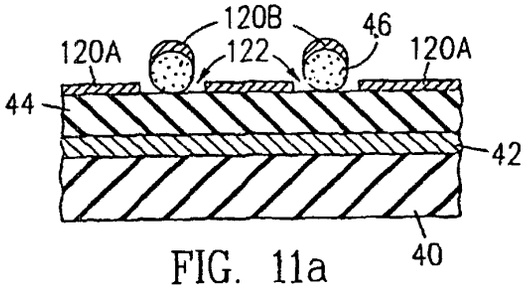


FIG. 11a

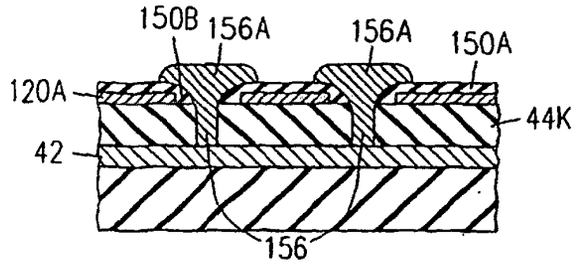


FIG. 11e

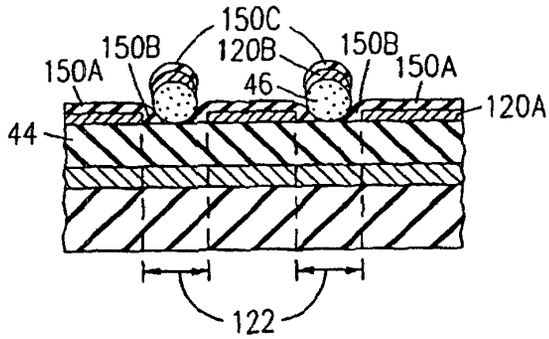


FIG. 11b

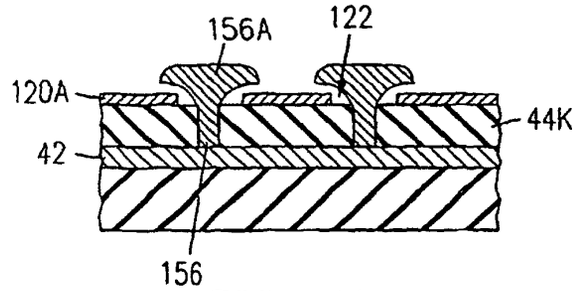


FIG. 11f

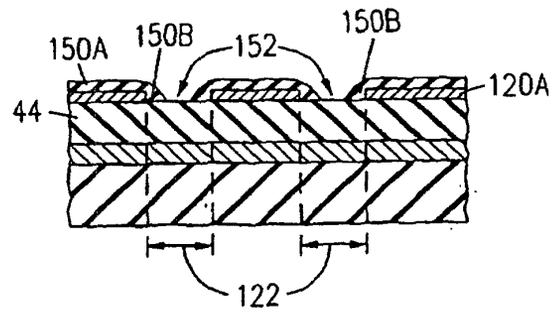


FIG. 11c

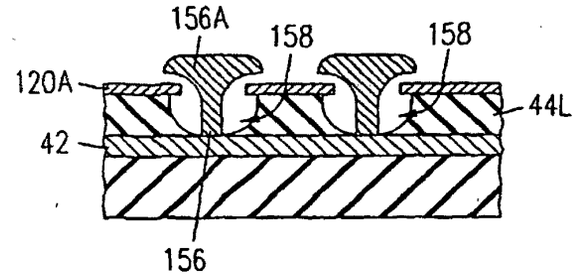


FIG. 11g

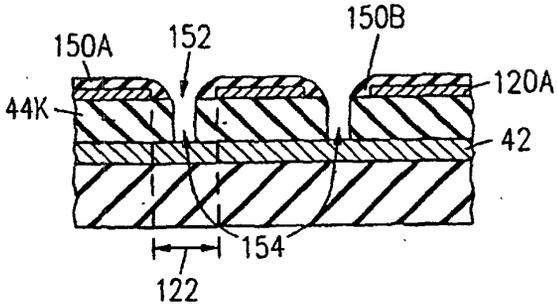


FIG. 11d

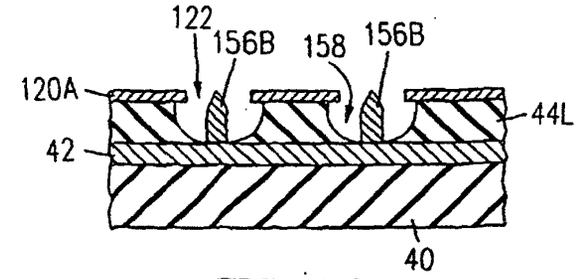


FIG. 11h

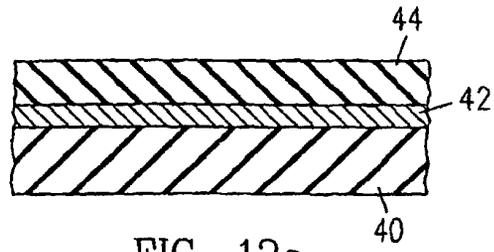


FIG. 12a

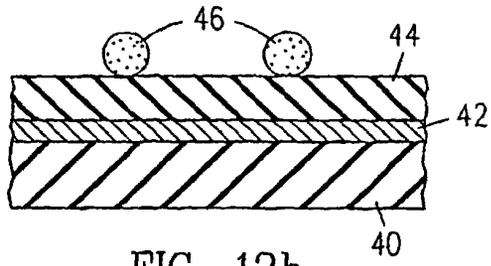


FIG. 12b

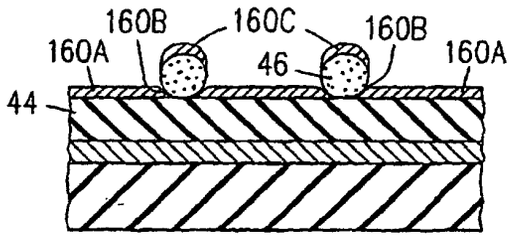


FIG. 12c

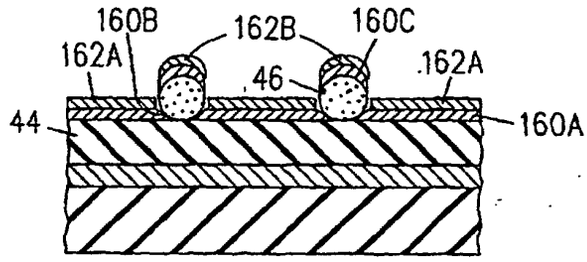


FIG. 12d

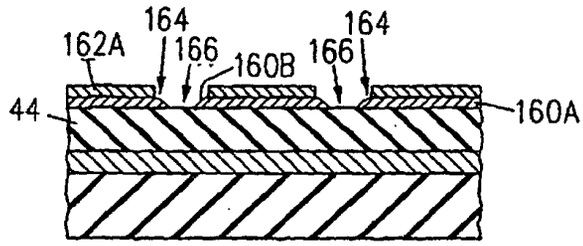


FIG. 12e

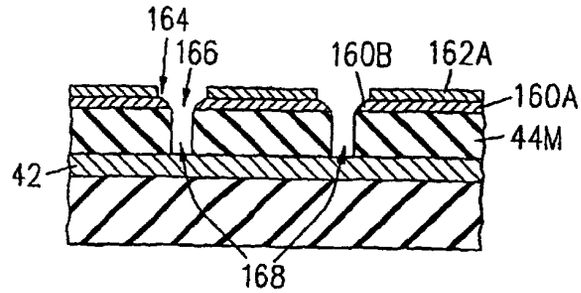


FIG. 12f

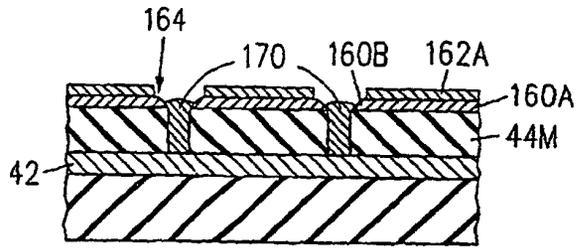


FIG. 12g

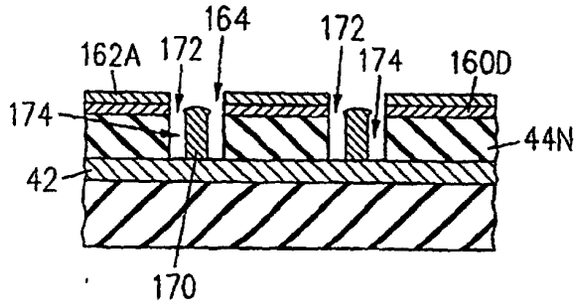


FIG. 12h

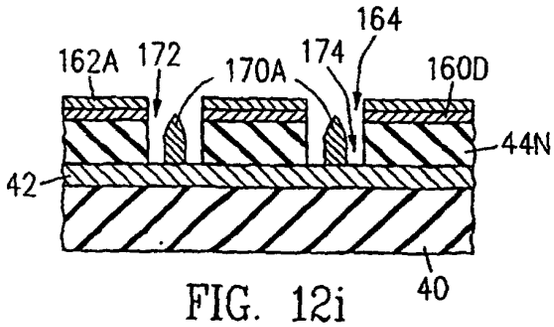


FIG. 12i

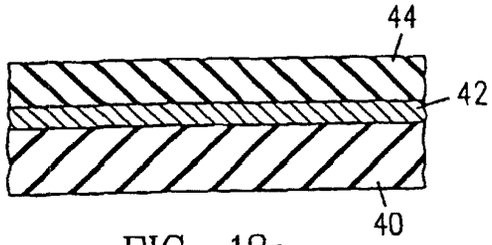


FIG. 13a

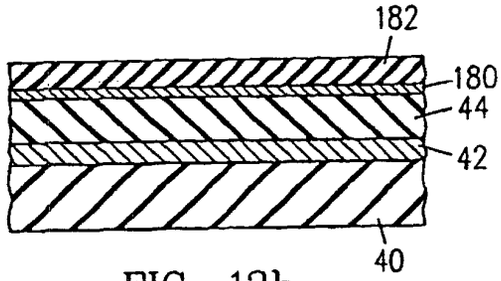


FIG. 13b

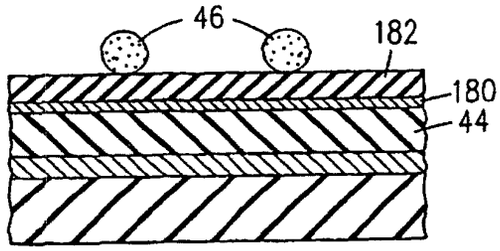


FIG. 13c

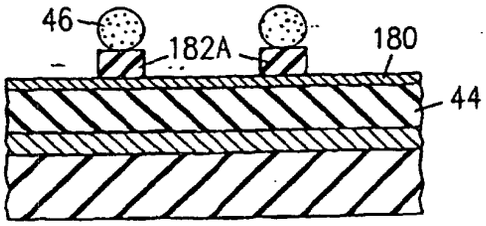


FIG. 13d

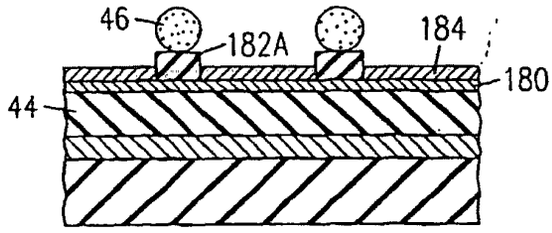


FIG. 13e

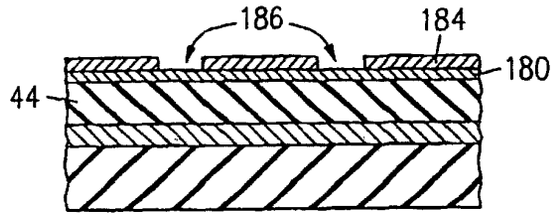


FIG. 13f

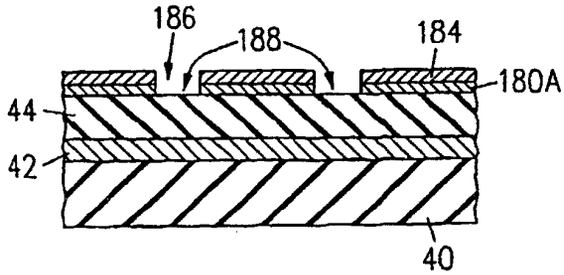


FIG. 13g

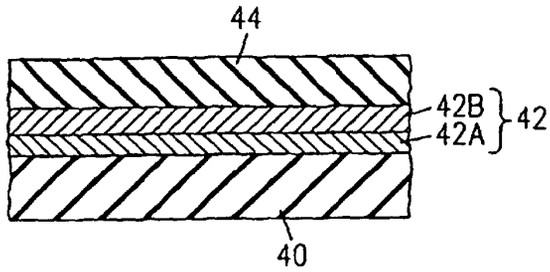


FIG. 14

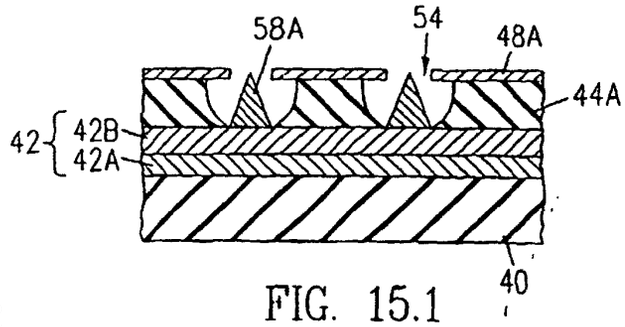


FIG. 15.1

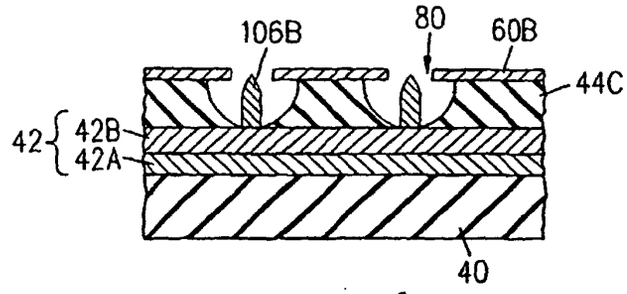


FIG. 15.2

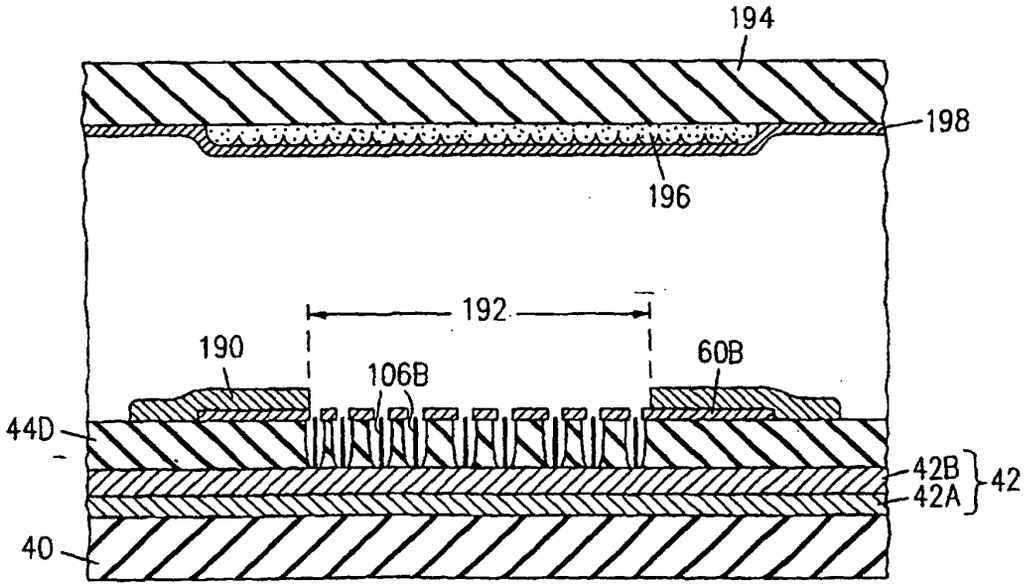


FIG. 16