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Remarks:
This application was filed on 11 - 01 - 1999 as a divisional application to the application mentioned under INID code 62.

(54) Low-power-consumption monitor standby system

(57) A computer system (233) comprising a central processing unit (CPU) (115;215), input apparatus (245, 251, 257), a video monitor (347; 447; 547), and comprising timer means (259) for monitoring activity of said input apparatus (245, 251, 257); signalling means (217) for signalling the video monitor to assume an alternative power state in response to output from the timer means; and power management means (339) for removing power from power using circuits in the monitor (347; 447; 547); characterised in that the video monitor (347; 447; 547) is capable of entering any one of two or more reduced power states in response to a specific command sent by the signalling means, in that specific commands are associated in the video monitor with specific reduced power states, and in that the video monitor enters an appropriate state according to the command sent by the signalling means.

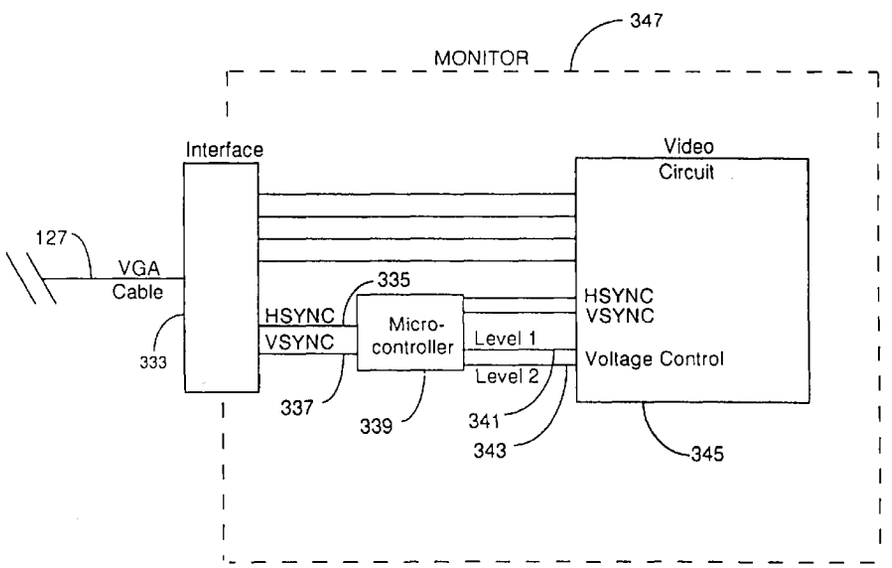

Fig. 3

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Description

[0001] The present invention is in the field of automatic power saving devices and pertains in particular to reduction of power consumption by computer video monitors.

[0002] A typical color video monitor may consume as much as 50 to 80 percent of the total electrical energy consumed by a personal computer (PC). A video monitor dissipates this energy as visible light emissions from screen phosphors, thermal waste, electromagnetic radiation, high-energy radiation and acoustic energy. Only the phosphor emissions are normally considered useful and then only when actively being watched by an observer. The radiation emissions have been a hotly debated source of concern regarding possible health risks from long-term exposure. Manufacturers incur considerable extra expense to reduce radiation emissions from video monitors. Some people are annoyed by the acoustic emissions produced by some monitors. Thermal losses from video monitors contribute an additional load on air conditioning equipment. The energy efficiency of video monitors has historically improved mostly as a result of advances in the electronic circuit components such as the increased use of integrated circuit (IC) devices. Cathode ray tube (CRT) technology has improved rather little in terms of energy efficiency.

[0003] The number of PC's in regular use is growing rapidly and has reached a point where they have become major consumers of electric power. The United States Environmental Protection Agency has issued power efficiency targets for computer manufacturers to design for in new systems. Low-voltage IC's use less energy, and microprocessor power management techniques allow a computer to reduce energy consumption when idling. Until a suitable replacement for the CRT or a more efficient CRT is developed it will be difficult to substantially improve personal computer energy efficiency.

[0004] What is needed is a way to shut down high-energy-consuming circuits in the video monitor when the computer determines that the display may be of no interest to anyone. This might be determined by a period of inactivity on input devices such a modem, mouse and keyboard. Many computers and video terminals use such a technique to activate a screen blanking circuit or a program that displays moving images (or no image) to avoid burning the screen phosphors. Activating an input device such as pressing a key or moving a mouse causes the previous screen image to be restored. This technique can be extended to reduce video monitor power consumption by signalling the microcontroller found in many recent design monitors, or an add-on device for "dumb" monitors, to shut down or restore some or all of the monitor's electrical power circuits. One key to accomplishing this end is a means of signalling a monitor to shut down to some selected level without adding to the signals presently provided to a monitor.

[0005] A screen blanker for the monitor of a computer system is disclosed in US-A-5059961, the system automatically clears the data image on the display screen if the computer has not been used for a predetermined length of time and re-displays the cleared data once the computer is operated again.

[0006] JP-A-1257893 discloses a system for powering down a display, including a control circuit which detects when a sync signal is or is not received by the display device, when there is no sync signal the power to the display is removed by means of a switch.

[0007] In IBM Technical Disclosure Bulletin vol. 34, No. 9 is disclosed a cathode ray tube monitor comprising a detector for detecting absence of HSYNC, or VSYNC signals sent by a host computer; and a power manager circuit coupled to the detector for reducing power consumption by power-using circuits in the cathode ray tube monitor; wherein the power manager circuit reduces power to power-using circuits in response to the detector detecting absence of said I-ISYNC, or VSYNC signals.

[0008] In an embodiment of the present invention a system is provided for a general purpose computer having a CPU, a memory means, a monitor, and video signal means for providing horizontal sync (HSYNC) and vertical sync (VSYNC) signals to the monitor, to signal the monitor to assume alternative states. The system comprises timing means for measuring periods of inactivity configured to reset to zero on input interrupts and to provide overflow signals at pre-set overflow values, and sync disabling means for interrupting at least one of the HSYNC and VSYNC signals to the monitor according to overflow states of the timing means. Power management means associated with said monitor may be included for selectively removing power from power-using circuits in said monitor in response to the absence of said at least one of said HSYNC and VSYNC signals.

[0009] In one embodiment the video signal means comprises video adapter circuitry having a VSYNC generator and an HSYNC generator, and the disabling means comprises a register associated with the video adapter circuitry, wherein one bit in the register is a vertical retrace polarity bit, and another bit is a horizontal retrace polarity bit. The timing means is provided by the CPU following a monitor power management instruction routine stored in the memory means, and SYNC signals are disabled by the CPU writing to the register. The monitor power management routine may be stored in the system BIOS.

[0010] In an alternative embodiment the system is implemented by an add-in time-out controller with sensing means for sensing user input interrupts, and the disabling means comprises at least one switch operable by the time-out controller and placed in a line carrying one of the HSYNC and VSYNC signals. In yet another alternative the system may be accomplished by an add-on (external) time-out controller connected to interface devices at the ports where user input devices are connect-

ed. The interface devices monitor input interrupts, and the add-on time-out controller is connected to an interrupt device at the monitor port for interrupting SYNC signals.

[0011] The disabling means may comprise separately operable switches in each of two lines one carrying said HSYNC signals and the other carrying said VSYNC signals. The disabling means may comprise a single switch interrupting two lines one carrying said HSYNC signals and the other carrying said VSYNC signals.

[0012] In another embodiment, the timing means comprises an add-on time-out controller connected to sensing devices interfaced at ports connected to user input devices comprising one or more of a modem, a pointer device, and a keyboard, and said SYNC disabling means is a device connected to said monitor, for interrupting HSYNC and VSYNC signals according to overflow states of said time-out controller.

[0013] In another aspect the invention involves a CRT monitor configured to respond to power level signals from a host computer. The monitor comprises a SYNC detector for monitoring the presence of VSYNC and I-ISYNC signals from the host, and power level control means for shutting down power circuitry in the CRT monitor in response. The detector may comprise a microcontroller sensing absence of SYNC signals and said power level control means is configured to operate in three power modes in response to signals from said microcontroller, a first mode having all circuits on, a second mode having all power circuits selectively operable by said power level control means off save a cathode heater remaining on, and a third mode having all power circuits selectively operable by said power level control means off. The fist mode being initiated in response to both of said HSYNC and VSYNC signals being sensed by said microcontroller at substantially operable levels. The second mode being initiated in response to one of said I-ISYNC and VSYNC signals being sensed by the microcontroller and the other not sensed. The third power mode being initiated in response to the other of said HSYNC and VSYNC signals being sensed and the remaining signal being not sensed. The third power mode may be initiated in response to both of said HSYNC and VSYNC signals not being sensed.

[0014] In yet another aspect a power system for a monitor is provided with an external SYNC detector placed in the monitor cable to the host. This controller drives a switch that controls AC mains power to the monitor.

[0015] A computer system according to the invention comprises timing means configured to reset to zero on system interrupts, SYNC disabling means for interrupting SYNC signals to a monitor, SYNC detector means associated with the monitor for sensing the presence of SYNC signals at the monitor, and power level control means associated with the monitor for shutting down power-using circuitry in the monitor in response to the presence of SYNC signals.

[0016] In yet another aspect a method is provided for saving power in a video display monitor, comprising steps of sensing input interrupts from user operated devices, resetting a timer to zero on receipt of such interrupts, providing a first power level signal to the monitor based on disabling at least one of a VSYNC and an HSYNC signal to the monitor, providing a second power level signal in a different configuration than for the first power level signal, sensing presence of the SYNC signals at the video monitor, and shutting down power circuitry in response to the power level signals. A cathode heater is left on for presence of the first signal, and power is shut off completely in response to receipt of said second signal.

[0017] The present invention in these several aspects provides a way to save power at a monitor, and minimise radiation emissions as well, in response to periods of inactivity, utilising to a great extent, existing elements and capabilities of a general purpose computer.

[0018] The invention will now be described in more detail, and by way of example only, with reference to the accompanying drawings, in which:

[0019] Fig. 1 is a largely schematic representation of a PC according to an embodiment of the present invention.

[0020] Fig. 2A is a largely schematic representation of a PC enhanced by an add-on device according to an alternative embodiment of the present invention.

[0021] Fig. 2B is a largely schematic representation of a PC enhanced by an add-in device according to another alternative embodiment.

[0022] Fig. 3 is a largely schematic representation of a microcontroller-based video monitor according to an embodiment of the present invention.

[0023] Fig. 4 is a largely schematic representation of a "dumb" monitor equipped with an add-in device according to an altemative embodiment of the present invention.

[0024] Fig. 5 is a largely schematic representation of an add-on device for controlling AC primary power to a monitor according to another alternative embodiment of the present invention.

[0025] Fig. 1 shows the functional elements of a preferred embodiment of the present invention capable of providing 3 distinct signals to a monitor to signal the monitor to adjust to as many as three states. In an embodiment of the invention, the states are selected levels of monitor power management (MPM). The signal to the monitor is based on interrupting one or the other or both HSYNC and VSYNC signals. In the embodiment shown in Fig. 1 a PC 111 comprises a Basic Input Output System (BIOS) 113 and a Video Graphics Adapter (VGA) 117. The invention will work equally well with other video adapters, as virtually all such adapters employ HSYNC and VSYNC signals. In some other adapters, equivalent means of interrupting the HSYNC and VSYNC signals would be used.

[0026] BIOS 113 includes instructions for MPM, which

can cause a central processing unit (CPU) 115 to change the state of sync-enable controls in VGA 117. In alternative embodiments instructions for implementing MPM might be embedded in operating system (OS) device driver routines or Terminate and Stay Resident (TSR) programs.

[0027] The MPM instructions monitor CPU 1 15 interrupts for input devices (not shown) such as the timer, keyboard and serial communication ports. MPM instructions advance a time-out counter on each timer interrupt and reset the count to an initial value on each monitored interrupt. The initial value of the MPM time-out counter may be fixed or adjustable. When the MPM time-out counter reaches a pre-set overflow value, due to cessation of monitored interrupts, instructions are executed that change the state of HSYNC Enable 124 and VSYNC Enable 126 control to disable output of horizontal synchronization signals (HSYNC) 123, produced by horizontal sync generator 122, and/or vertical synchronization signals (VSYNC) 125, produced by vertical sync generator 120, or both. A subsequent monitored interrupt causes execution of instructions that change the state of HSYNC Enable 124 and VSYNC Enable 126 control circuits to enable output of HSYNC 123 and VSYNC 125 signals from VGA 117.

[0028] In the case of a VGA controller, the enable/disable capability is through writing by the CPU into register 3C2 of the controller, wherein bits six and 7 are reserved for horizontal retrace polarity and vertical retrace polarity respectfiilly. HSYNC and VSYNC signals 123 and 125 are brought to interface 121 along with other signals, such as R, G, and B signals from D/A/converter 119. The signals are transmitted to a monitor on VGA cable 127 as is known in the art.

[0029] In an alternative embodiment, shown in Fig. 2A, useful for refitting existing computers, a current art PC 211 having a CPU 215 is enhanced by installation of a switch 231, which connects between a VGA 217 VSYNC output 225 and VSYNC input 226 to a video interface 221. In a color computer, R,G, and B signals are brought to interface 221 from DAC 219. An add-in time-out controller 229 comprising MPM instructions monitors input device activity as described above for Fig. 1. Time-out of all input devices causes instructions to be executed which change the state of program-controlled switch 231, blocking VSYNC input 225 to video interface 221. Resumption of monitored interrupts causes switch 231 to close, returning the VSYNC signals to line 226. A second switch 232 may be used in the I-ISYNC line to interrupt the HSYNC signals to line 224, and, in this embodiment, the add-in time-out controller controls both switches. In yet another alternative, one switch may be used to interrupt both HSYNC and VSYNC signals.

[0030] The functional blocks presented in Fig. 2A are an internal solution to an add-in hardware/software embodiment, and the blocks are not intended to be taken literally as hardware devices and interfaces. It will be apparent to one with skill in the art that there are many equivalent ways the functional blocks might be accomplished. The keyboard, mouse, and modem inputs are monitored by the add-in controller, and are made available as well to the CPU in the typical manner.

[0031] Fig. 2B shows an external solution for a hardware/software embodiment. In this solution an add-on time-out controller 259 is external to computer system 233, and each port that supports an input device and the video output port is fitted with an interface device connected to the add-on time-out controller. For example, interface 243 at COM port 241 used for a modem 245 monitors modem activity and reports to controller 259 on line 244. Interface 249 at keyboard port 247 monitors keyboard 251 activity and reports to controller 259 on line 250. Interface 255 at pointer port 253 monitors pointer 257 activity (mouse, joystick, trackball), and reports to controller 259 on line 256.

[0032] In this embodiment controller 259 accomplishes the timer functions and outputs signals on line 238 to interface device 237 at video port 235. Line 239 goes to the monitor. Device 237 interrupts HSYNC and VSYNC signals according to the overflow states of add-on controller 259.

[0033] A color video monitor 347 according to an embodiment of the present invention is shown in Fig. 3. Monitor 347 comprises an interface 333, a microcontroller 339 having MPM instructions according to the present invention and a video circuit (VC) 345 having voltage control circuitry. From interface 333 HSYNC pulses 335 and VSYNC pulses 337 go to microcontroller 339. Microcontroller 339 monitors the HSYNC signal 335 and VSYNC signal 337. The MPM instructions described above count the number of HSYNC pulses occurring between each pair of VSYNC pulses. Zero HSYNC pulses counted causes the MPM instructions in microcontroller 339 to change the voltage on Level-2 signal line 343. Similarly, an interval count of HSYNC 335 pulses greatly in excess of the maximum video scan rate for monitor 347, indicating a loss of VSYNC 337, causes microcontroller 339 to change the voltage on Level-1 signal line 341. Resumption of HSYNC 335 to VSYNC 337 pulse interval counts to a range from the minimum to the maximum scan rate causes MPM instructions in microcontroller 339 to restore quiescent voltage levels to Level-1 signal line 341 and Level-2 signal line 343.

[0034] When video circuit 345 senses an active voltage level on Level-1 signal line 341, it cuts off power to all circuits in monitor 347 except microcontroller 339, any power necessary to interface 333, and video circuit 345 power-control circuits (not shown). In this level I standby mode, power consumption of monitor 347 is reduced by more than 90 percent. If monitor 347 remains in level I standby for more than a few seconds, full warm-up time is required to reactivate it. An active voltage level on Level-2 signal line 343 causes video circuit 345 to cut off power to all circuits except those described above plus the CRT cathode heater. In level 2 standby mode

monitor 347 power consumption is reduced by 80 to 90 percent. Because the CRT is kept hot, reactivating monitor 347 from level 2 standby requires about 5 seconds or less. Reactivation of monitor 347 occurs when voltage on Level-1 signal line 341 and Level-2 signal line 343 returns to the quiescent state allowing video circuit 345 to activate power to all circuits of monitor 347.

[0035] Fig. 4 shows an alternative embodiment of the present invention in a monitor 447 with video circuits functionally similar to those described for the monitor shown in Fig. 3, including an interface 433 and a video circuit 445, but without a microcontroller. A sync detect circuit 451 compares pulse intervals for HSYNC 435 and VSYNC 437 against time-constants of adequate duration to allow for brief interruptions of sync pulses. Loss of HSYNC 435 pulses or VSYNC 437 pulses for periods longer than the associated time-constants causes sync detector circuit 451 to change Level-1 signal line 441 or Level-2 signal line 443 voltage to its active state as described for Fig. 3 and with the same results. Similarly, resumption of HSYNC 435 and VSYNC 437 pulses reactivates monitor 447 as described for Fig. 3 above.

[0036] Fig. 5 shows another alternative embodiment of the present invention suitable for add-on use with a monitor 547 having an interface 533. A sync detect circuit 551, in an external enclosure having pass-through connections, inserts into VGA cable 127. Sync detect circuit 551 monitors video signals on VGA cable 127 and compares the SYNC interval for one or the other of VSYNC and HSYNC to a time-constant in a manner similar to that described for Fig. 4 above. Loss of the monitored SYNC signal in VGA cable 127 for an interval longer than the time-constant causes sync detect circuit 551 to change the voltage on power-control line 561 to its active level, which in turn causes an electronically-control led switch 553 to open. Electronically-controlled switch 553 controls AC primary power from an electrical cord 559 to a receptacle for monitor 547 power supply cord 557. When electronically-controlled switch 553 opens, AC power to a DC power supply 555 is lost, thus causing total shutdown of monitor 547. Resumption of SYNC signals in VGA cable 127 video signal causes sync detect circuit 551 to change power-control line 561 to its quiescent state, thus causing electronically-controlled switch 553 to close, which restores AC power input to DC power supply 555 reactivating monitor 547.

[0037] Whilst particular embodiments of the invention have been described, alternatives will suggest themselves to those skilled in the art without departing from the scope of the invention as defined in the appended claims. Some of these alternatives have already been described, such as MPM instructions implemented in an OS device driver or TSR routines instead of the BIOS, single-level MPM instead of two-level MPM and an external video monitor power control device. Other methods of signalling MPM state changes to a monitor might include time-based coded sequences of frequency changes in HSYNC or VSYNC, coded values in the color signals, or no color signal for an extended period. Alternative embodiments of MPM routines might allow an operator to control MPM operation through command steps, such as menus, dialog boxes or command lines. Such controls might include shutting down monitor power at will by pressing a "hot key", typing a command line or other program interface step. Other features might allow the operator to change the idle time required to trigger MPM and toggle MPM monitoring on or off. Alternative MPM routines might also require an operator to type a password before enabling the transmission of normal video signals to the video monitor. Alternative devices for both built-in and post-manufacture modification to implement monitor power control might be devised. Embodiments of the present invention for monochromatic and grey-scale video adapters and monitors are also contemplated.

Claims

1. A computer system (233) comprising a central processing unit (CPU) (115;215), input apparatus (245, 251, 257), a video monitor (347; 447; 547), and comprising:

   timer means (259) for monitoring activity of said input apparatus (245, 251, 257);
   signalling means (217) for signalling the video monitor to assume an alternative power state in response to output from the timer means; and
   power management means (339) for removing power from power using circuits in the monitor (347; 447; 547);
   characterised in that the video monitor (347; 447; 547) is capable of entering any one of two or more reduced power states in response to a specific command sent by the signalling means, in that specific commands are associated in the video monitor with specific reduced power states, and in that the video monitor enters an appropriate state according to the command sent by the signalling means.

2. A computer system as in claim 1, comprising a video adapter (117; 217) for providing video signals, including colour, VSYNC, and HSYNC signals to the video monitor (347), wherein the signalling means comprises the CPU signalling the video adapter (117; 217) to encode at least first and second power management signals in the video signals provided to the video monitor (347; 447; 547).

3. A computer system as in claim 2, wherein the video adapter (117; 217) provides said at least first and second power management signals by interrupting at least one of the HSYNC or VSYNC signals.

4. A computer system as in claim 2 or 3, wherein the video adapter (117; 217) provides said at least first and second power management signals by using time based coded signals in the HSYNC or VSYNC signals, coded values in the colour signal or by interrupting signals in different configurations in response to different periods of inactivity of the input apparatus.

5. A computer system as in claim 1 or 2, wherein the timer means comprises control routines executed by the CPU (115, 215).

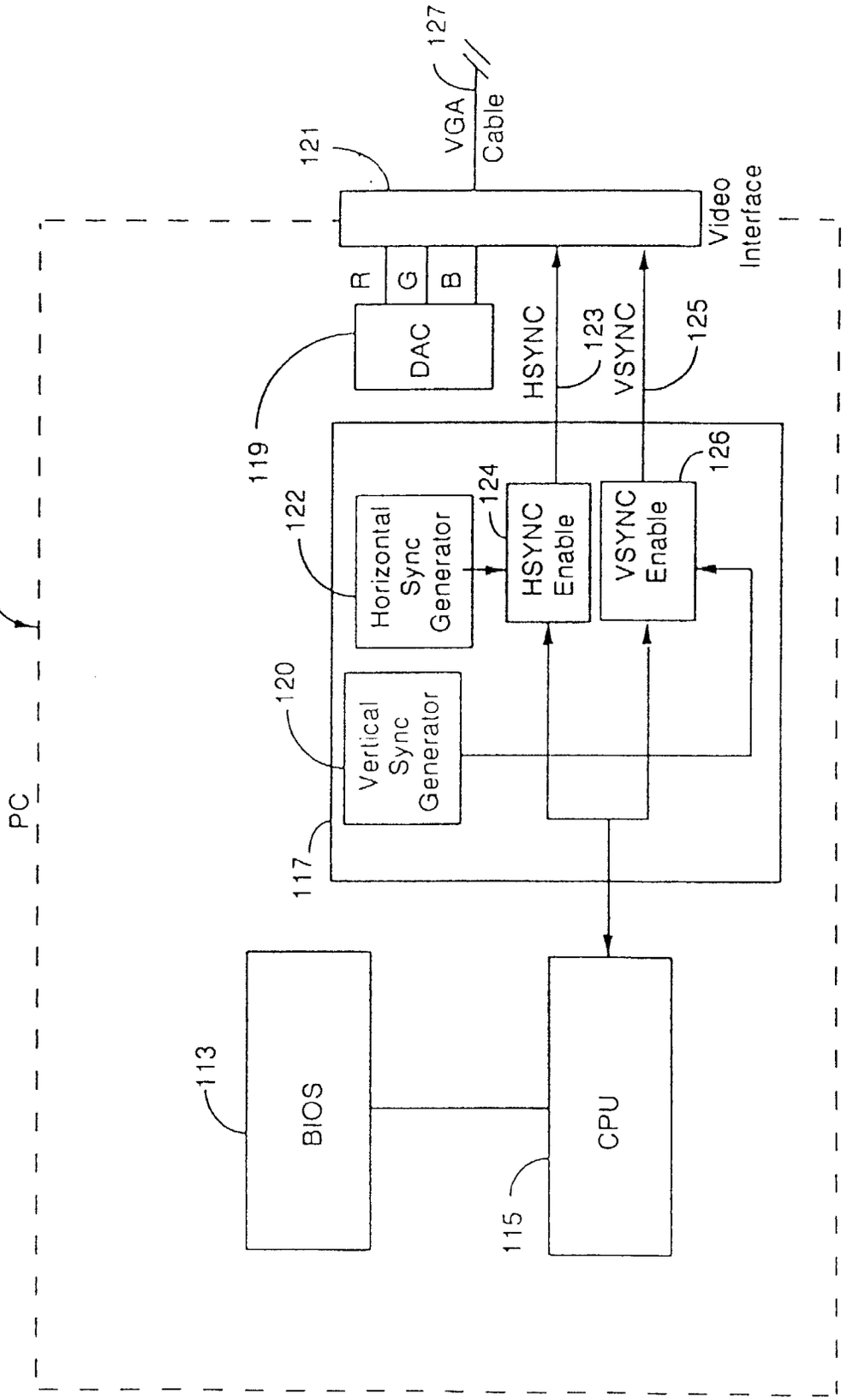
6. A computer system as in claim 5, wherein the control routines are provided in a system BIOS (113) in a programmable read only memory.

7. A computer system as in claim 2, wherein the timer means comprises an add-in time-out controller (259) including circuitry for detecting periods of inactivity of input apparatus, and the signalling means comprises a plurality of electrically-operable switches in lines carrying the colour, HSYNC, or VSYNC signals, the electrically-operable switches are operable by a signal from the add-in time-out controller (259), and the add-in time-out controller (259) interrupts the signals provided by the video adapter (117; 217) to the video monitor (347; 447; 547) in different configurations in response to different periods of inactivity of the input apparatus to provide said at least first and second power management signals.

8. A computer system as in claim 2, wherein the power management means comprises circuitry for monitoring the incoming signals provided by a video adapter (117; 217), and for controlling power use by circuitry other than the power management means in response to detection of said at least first and second power management signals provided to the monitor (347; 447; 547).

9. A computer system as claimed in claim 8, wherein the circuitry other than the power management means comprises a filament heater.

10. A computer system as claimed in claim 1, wherein the input apparatus comprises one or more of a keyboard (251), a modem (245), and a pointer device (257), and the timer means comprises an add-on time-out controller (259) connected to sensing devices interfaced at input ports for the input apparatus, the sensing devices (243, 249, 255) configured to detect periods of inactivity of the input apparatus, and the signalling means comprises circuitry interfaced to an output port for the colour, HSYNC, or VSYNC signals provided by a video adapter (117; 217) to the video monitor (347; 447; 547), the signalling means comprises a plurality of electrically operable switches for interrupting the signals provided by the video adapter (117; 217) to the video monitor (347; 447; 547).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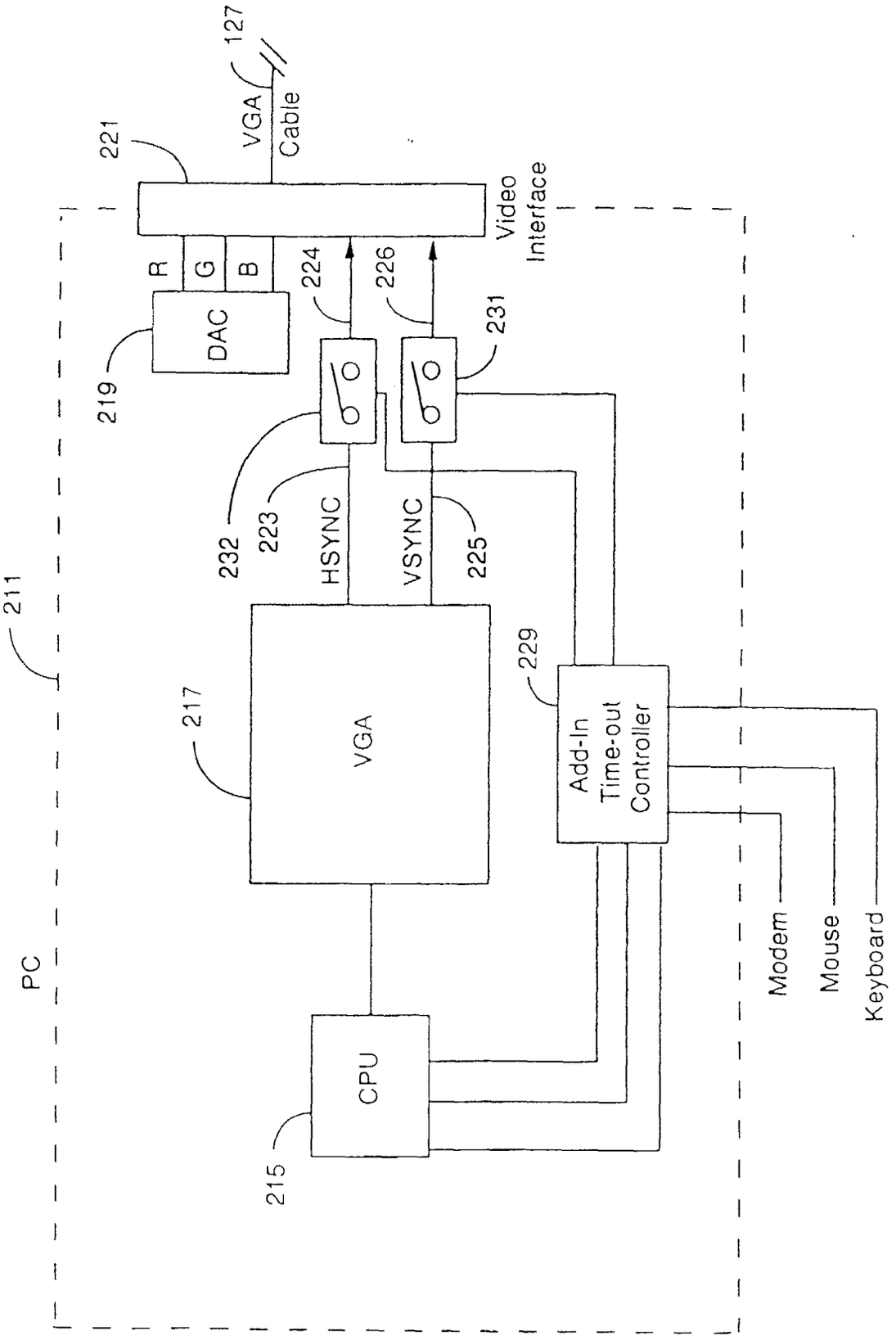
Video Interface
121
VGA Cable
127

Fig. 1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VSYNC
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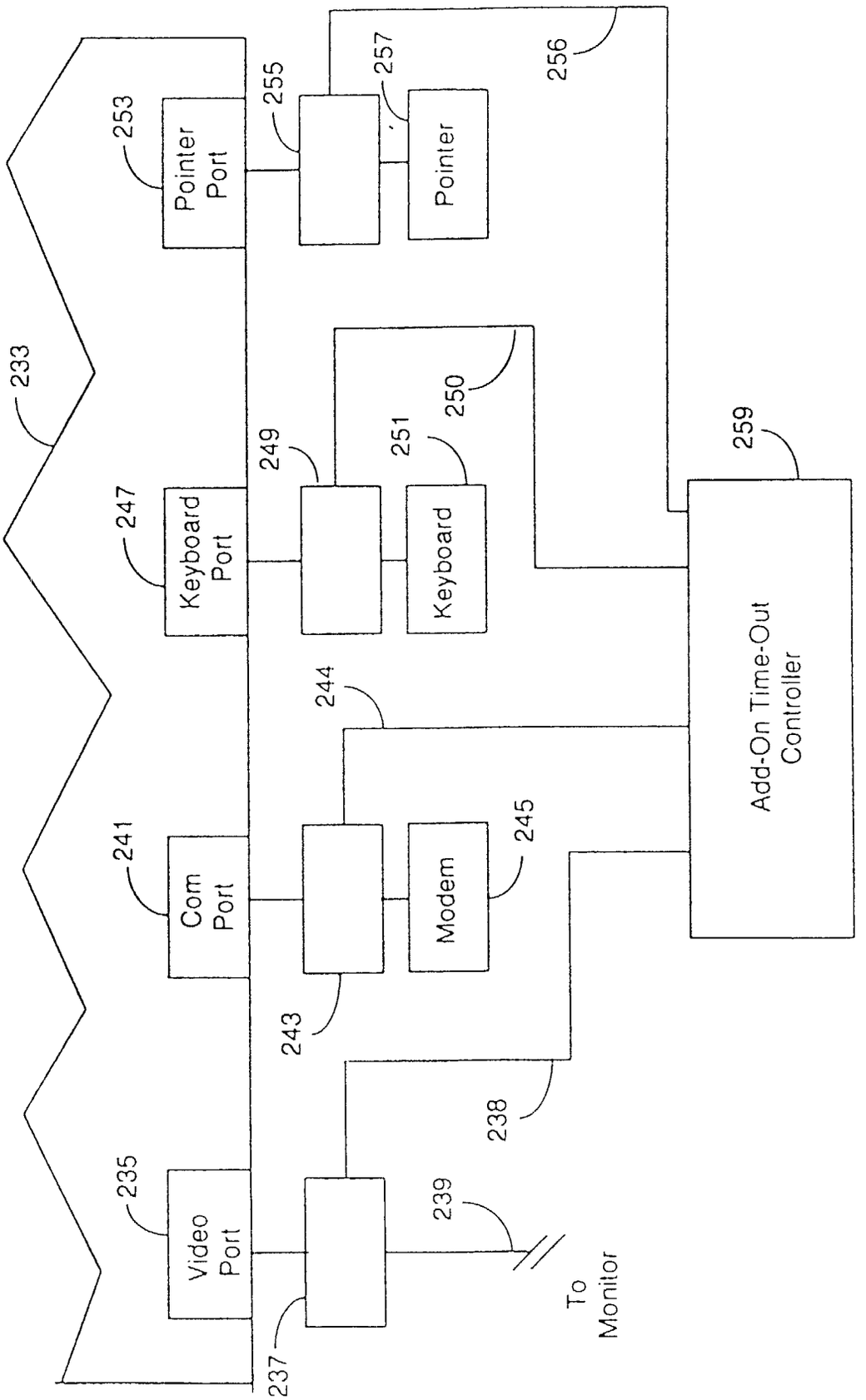
Add-In Time-out Controller
Modem
Mouse
Keyboard

Fig. 2A


233
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Keyboard Port
249
251
Keyboard
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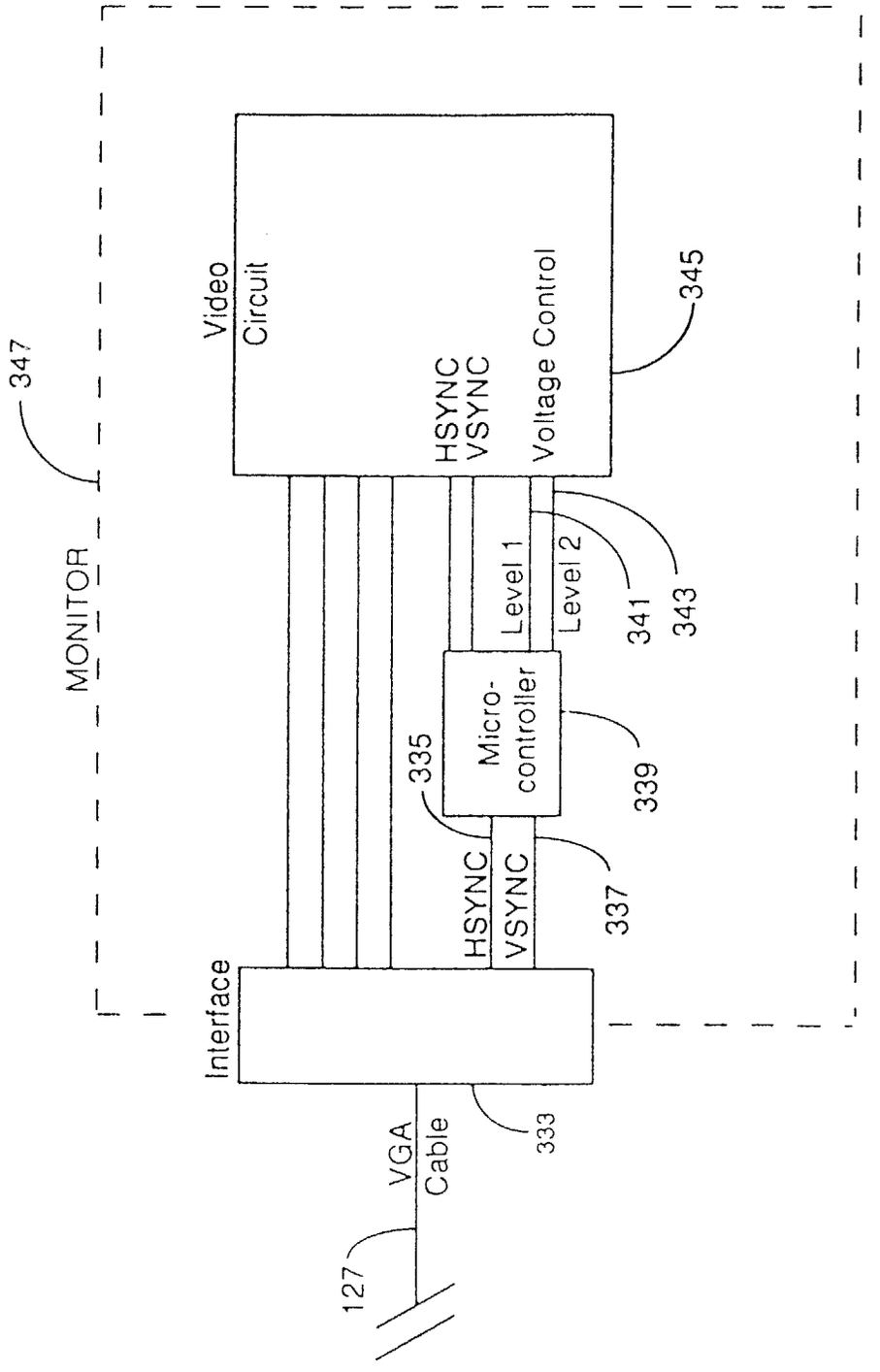
259
Add-On Time-Out Controller
244
241
Com Port
245
Modem
243
238
235
Video Port
239
To Monitor
237

Fig. 2B


347
MONITOR
Video
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HSYNC
VSYNC
Voltage Control
345
Level 1
Level 2
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Micro-
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HSYNC
VSYNC
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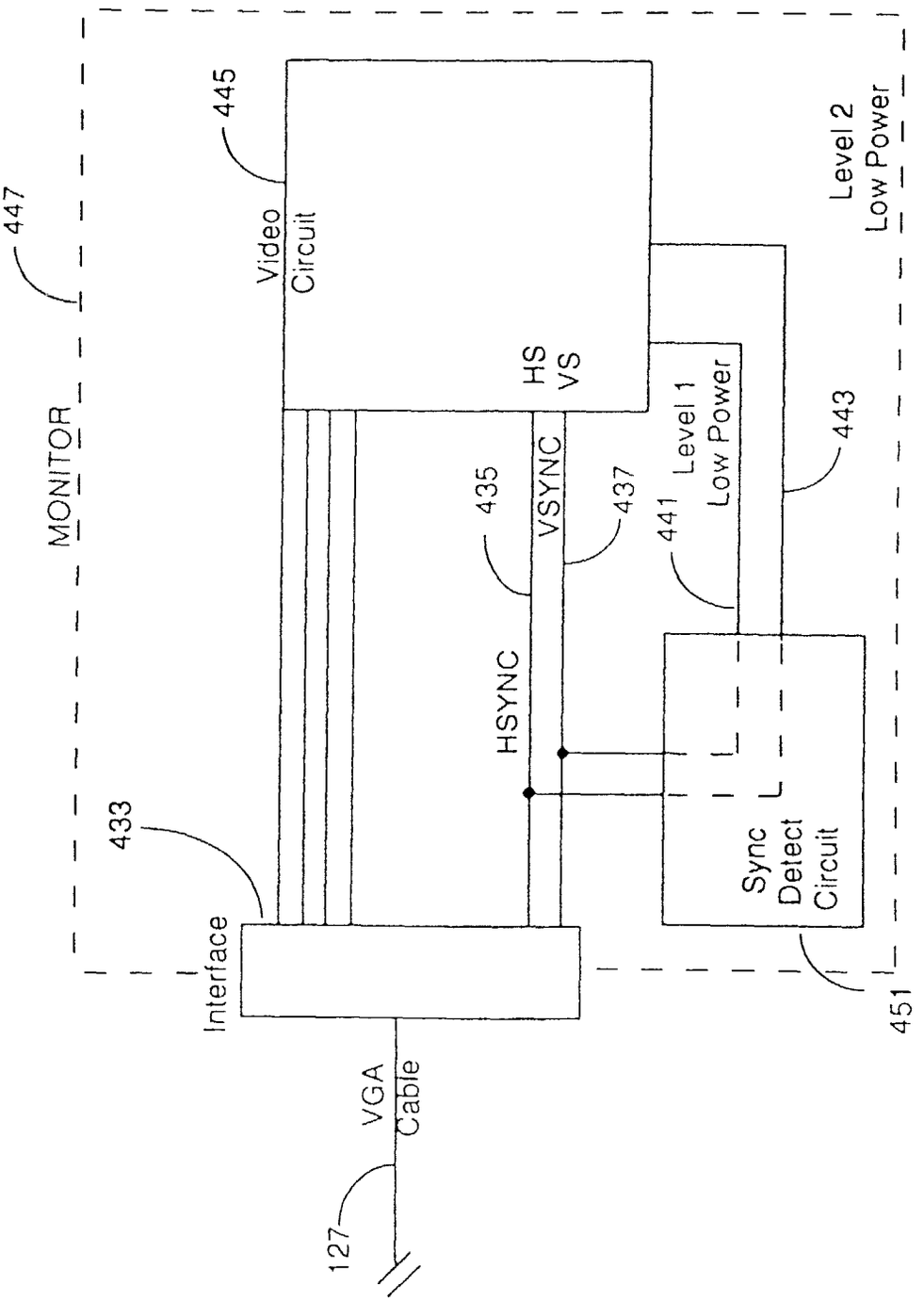
Interface
333
VGA
Cable
127

Fig. 3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Video
Circuit
HS
VS
Level 2
Low Power
443
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HSYNC
VSYNC
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Low Power
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Interface
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Detect
Circuit
451
VGA
Cable
127

Fig. 4

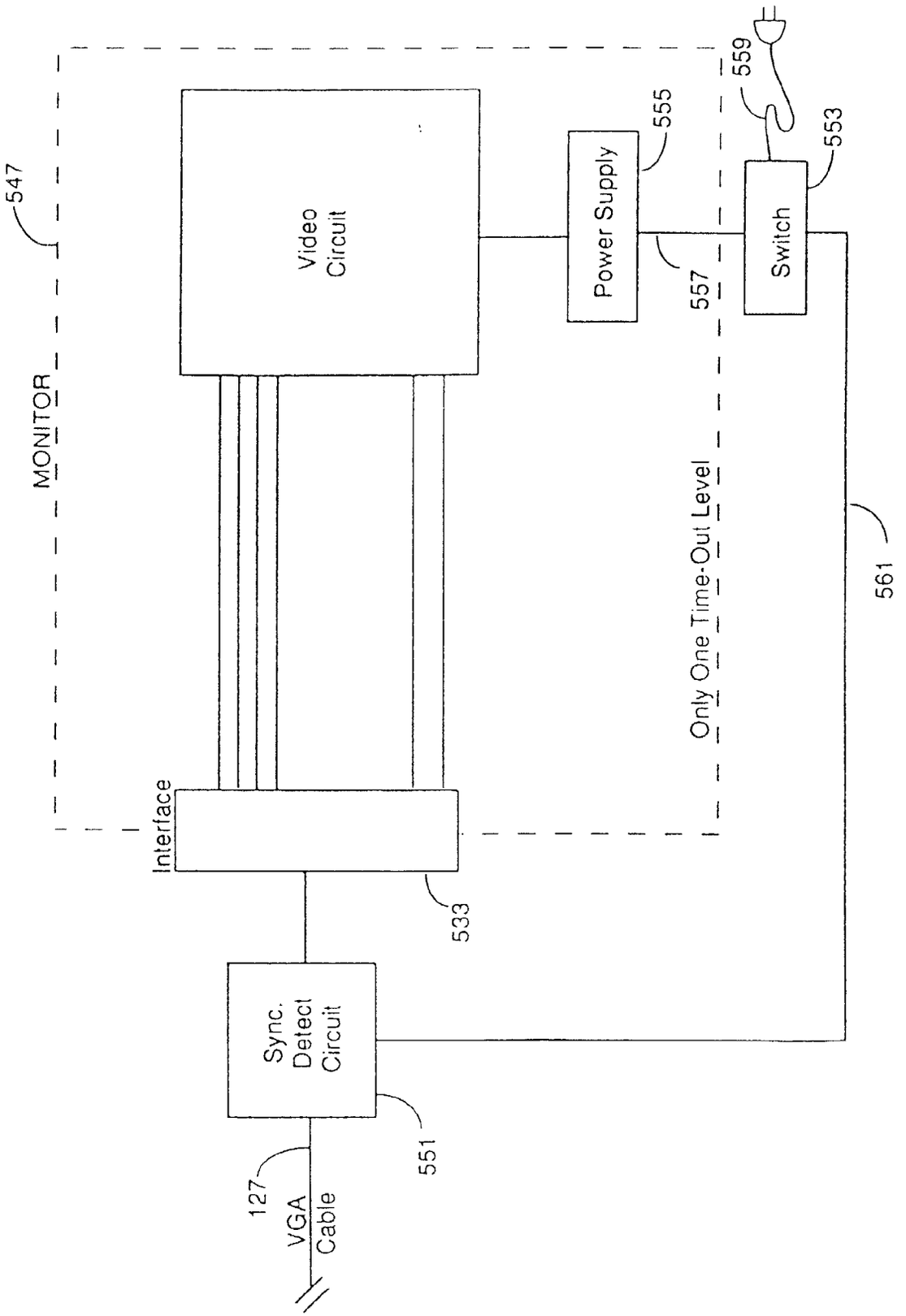
MONITOR
547
Video Circuit
Power Supply
555
559
553
Switch
557
Only One Time-Out Level
561
Interface
533
Sync. Detect Circuit
551
127
VGA Cable

Fig. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 20 0054

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	DE 92 01 166 U (SIEMENS NIXDORF INFORMATIONSSYSTEME) 9 April 1992 * page 2, line 36 - page 3, line 28; figures 1,2 * * page 4, line 9 - line 38; figure 5 *	1-4,8	G09G1/16 G06F1/32
A,D	US 5 059 961 A (CHENG TE J) 22 October 1991 * column 4, line 22 - line 56; figures 1,2 *	1-4,7,10	
A,D	ANONYMOUS: "Increasing Lifetime and Reliability of CRT Displays." IBM TECHNICAL DISCLOSURE BULLETIN, vol. 34, no. 9, pages 281-283, XP000301874 NEW YORK, US * the whole document *	1-10	
X,P A,P	GB 2 264 848 A (ICL PERSONAL SYSTEMS OY) 8 September 1993 * page 2, line 20 - line 28 * * page 3, line 25 - page 4, line 17 * * page 12, line 6 - page 14, line 5 * * figures 1-4 *	1-4,8,9 5-7,10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G G06F
X,P A,P	WO 93 15495 A (SIEMENS NIXDORF INF SYST) 5 August 1993 * abstract; figures 1-7 * * page 3, line 20 - page 3, line 30 * * page 4, line 33 - page 6, line 31 *	1-4,8,9 5-7,10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 April 1999	Van Roost, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 20 0054

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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20-04-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 9201166 U	09-04-1992	AT 129588 T	15-11-1995
		WO 9315495 A	05-08-1993
		DE 59300827 D	30-11-1995
		EP 0624272 A	17-11-1994
		ES 2078818 T	16-12-1995
		US 5774116 A	30-06-1998
US 5059961 A	22-10-1991	NONE	
GB 2264848 A	08-09-1993	FI 920935 A	03-09-1993
		US 5786813 A	28-07-1998
WO 9315495 A	05-08-1993	DE 9201166 U	09-04-1992
		AT 129588 T	15-11-1995
		DE 59300827 D	30-11-1995
		EP 0624272 A	17-11-1994
		ES 2078818 T	16-12-1995
		US 5774116 A	30-06-1998

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