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(72) Inventors:
• **Arimilli, Ravi Kumar**
Austin, Texas 78759 (US)
• **Dodson, John Steven**
Pflugerville, Texas 78660 (US)
• **Lewis, Jerry Don**
Round Rock, Texas 78681 (US)

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(71) Applicant: **International Business Machines
Corporation**
Armonk, N.Y. 10504 (US)

(74) Representative: **Burt, Roger James, Dr. et al**
IBM United Kingdom Limited
Intellectual Property Department
Hursley Park
Winchester Hampshire SO21 2JN (GB)

(54) **Cache coherency protocol with tagged state and historical information**

(57) A cache coherency protocol uses a "Tagged" coherency state to track responsibility for writing a modified value back to system memory, allowing intervention of the value without immediately writing it back to system memory, thus increasing memory bandwidth. The Tagged state can migrate across the caches (horizontally) when assigned to a cache line that has most recently loaded the modified value. Historical states relating to the Tagged state may further be used. The invention may also be applied to a multi-processor computer system having clustered processing units, such that the

Tagged state can be applied to one of the cache lines in each group of caches that support separate processing unit clusters. Priorities are assigned to different cache states, including the Tagged state, for responding to a request to access a corresponding memory block. Any tagged intervention response can be forwarded only to selected caches that could be affected by the intervention response, using cross-bars. The Tagged protocol can be combined with existing and new cache coherency protocols. The invention further contemplates independent optimization of cache operations using the Tagged state.

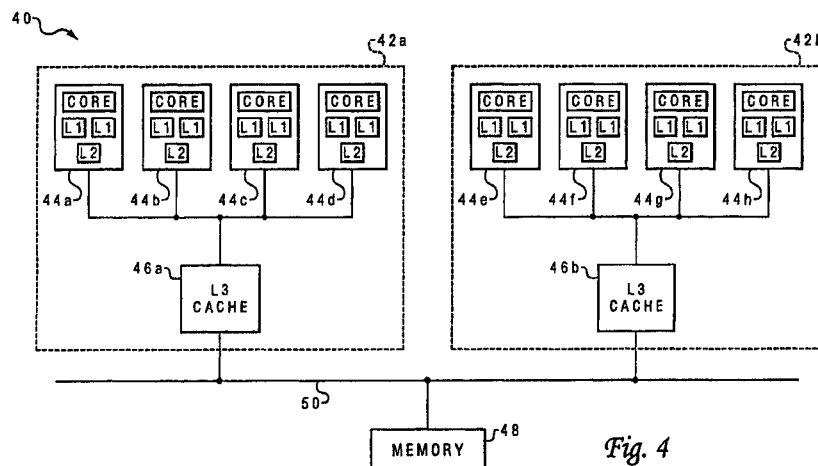


Fig. 4



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 1052

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	BORRILL P: "FUTUREBUS PROTOCOLS KEEP CACHE DATA CONSISTENT" COMPUTER TECHNOLOGY REVIEW, vol. 9, no. 10, 21 June 1989 (1989-06-21), page 36, 38 XP000054499 ISSN: 0278-9647 * the whole document *	1-7,9,10	G06F12/08
X	SWEAZY P ET AL: "A CLASS OF COMPATIBLE CACHE CONSISTENCY PROTOCOLS AND THEIR SUPPORT BY THE IEEE FUTUREBUS", PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, TOKYO, JUNE 2 - 5, 1986, NR. SYMP. 13, PAGE(S) 414 - 423, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS XP002039991 * page 33, middle column, line 9 - page 34, right-hand column, line 2; figures 2,3 *	1-7,9,10	
X	"CACHING ON FUTUREBUS" ELECTRONIC ENGINEERING, vol. 60, no. 739, 1 July 1988 (1988-07-01), page 31, 33/34, 36 XP000046105 ISSN: 0013-4902 * page 416, left-hand column, paragraph 3 - page 420, left-hand column, paragraph 4.2; figure 3 *	1-7,9,10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 3 August 1999	Examiner Ledrut, P
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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