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(54) Direct processing circuit for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in AC electric drives

(57) A direct processing circuit for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in AC electric drives, comprising means for integrating logic and digital functions. Said means are connected to a digital processor and are adapted to send digital signals to means for multiplying digital/analog signals. The multiplying means receive in input analog signals which are meant to be multiplied with the digital signals in order to obtain analog output signals as a function of preset numeric data. The means for integrating logic and digital functions drive the multiplying means in time-sharing mode.

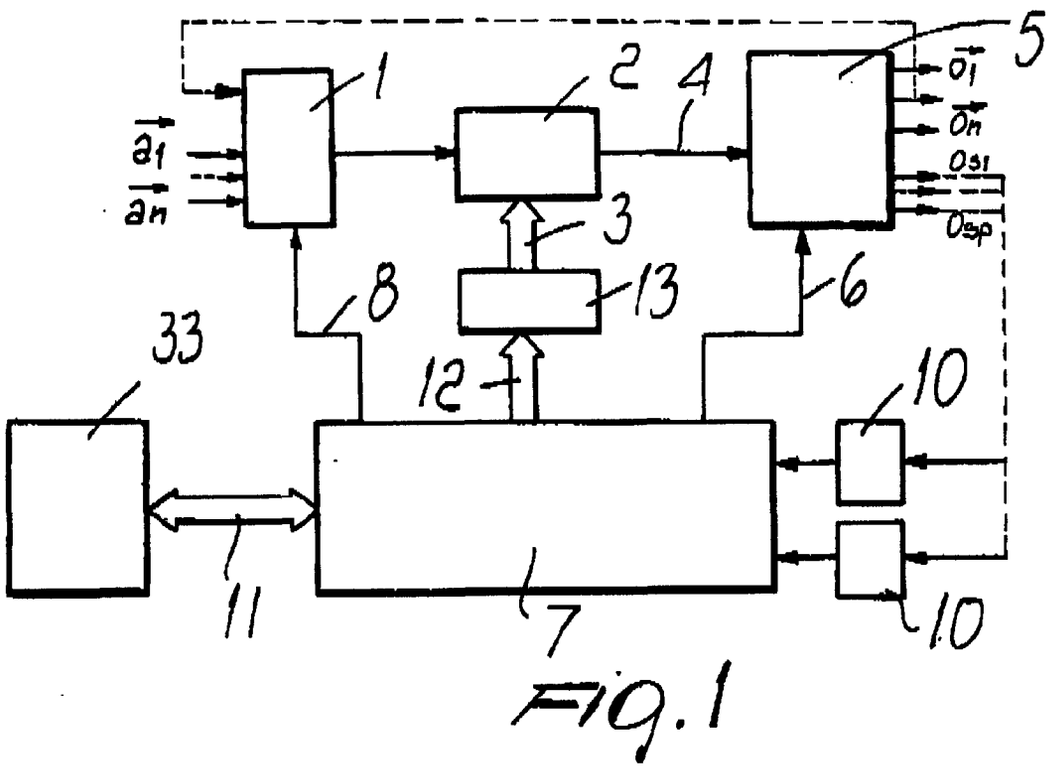

Fig.1

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Description

[0001] The present invention relates to a direct processing circuit for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in high-performance AC electric drives.

[0002] More particularly, the invention relates to a direct processing circuit for unifying the processing of analog and digital signals which is particularly suitable for use in power converters dedicated to the control of brushless and reluctance motors.

[0003] Currently, in the field of industrial automation and process control there is a distinct trend to switch to fully digital process, using microprocessors and/or DSPs (Digital Signal Processors).

[0004] Accordingly, in the processing device any analog input signals must be first converted into a digital form. This can entail problems due to discretization and to sampling (numeric and time resolution, truncations, etcetera) and high costs for providing A/D conversion means dedicated to the individual signals to be converted.

[0005] Sometimes there is a trend toward performing the A/D conversion directly on board the transducer, with a consequent use of serial communication buses.

[0006] At the same time, the process control architecture based on hierarchically-distributed intelligence has become widespread and particularly developed and commercially important.

[0007] Where it is necessary to provide interfacing with the physical process, there is a centralization of processing, conversion and transmission functions with adequate support for processing. This fact leads to the centralization of tasks, to the point of constituting a node of the distributed-intelligence architecture.

[0008] In the case of electric drives, the considerations mentioned above are currently applied in the part of the electronic converter which is dedicated to the control and monitoring functions. Therefore, the so-called "full digital drive" is increasingly widespread.

[0009] Practice has shown, however, that, next to undeniable advantages, this approach also entails technical advantages, already mentioned, and also entails higher costs of the product.

[0010] From the technical point of view, for drives it should also be noticed that an input signal always present in practice, especially in servo drives, is the signal coming from the position transducer of the mechanical movement in output. This signal is very often analog, for example when the transducer is a resolver.

[0011] Currently these signals are processed (demodulated etcetera) by using discrete components of the dedicated type, which are very expensive particularly for obtaining characteristics which are adapted for high-performance drives.

[0012] The aim of the present invention is to provide a direct processing circuit of analog and digital signals, particularly for the use in high performance AC drives, which is capable of unifying the processing of all the control signals by using, in a time-sharing mode, a single digital/analog conversion hardware to provide algebric functions and digital/analog and analog/digital conversions in zero-follower mode.

[0013] Within this scope, another object of the present invention is to provide a direct processing circuit for unifying the processing of analog and digital signals for controlling drive circuits which processes in different manners the components of an analog input vector, selected with an appropriate order, in order to generate a single analog output as a function of preset numeric data.

[0014] Another object of the present invention is to provide a direct processing circuit for unifying the processing of analog and digital signals for controlling drive circuits which provides, in an optimized manner, the functions of trigonometric calculation, particularly position signal demodulation, that arrive from an angular position transducer, and of digital/analog conversion.

[0015] Another object of the present invention is to provide a direct processing circuit for unifying the processing of analog and digital signals for controlling drive circuits combined with circuits which use numeric microprocessors.

[0016] Another object of the present invention is to provide a direct processing circuit for unifying the processing of analog and digital signals for controlling drive circuits which is highly reliable, relatively easy to provide and at competitive costs.

[0017] This aim, these objects and others which will become apparent hereinafter are achieved by a direct processing circuit for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in high performance AC electric drives.

[0018] The direct processing circuit according to the present invention is characterized in that it comprises means for integrating logic and digital functions which are connected to a digital processor and are suitable to send digital signals to means for multiplying digital/analog signals, said multiplying means receiving in input analog signals which are meant to he multiplexed with said digital signals in order to obtain analog output signals as a function of preset numeric data, said means for integrating logic and digital functions driving said multiplying means in a time-sharing mode.

[0019] Further characteristics and advantages of the invention will become apparent from the following detailed description of a preferred but not exclusive embodiment of the circuit according to the invention, illustrated only by way of non-limitative example in the accompanying drawings, wherein:

- Figure 1 is a conceptual block diagram of the circuit according to the present invention;
- Figure 2 is a block diagram of the configuration and of the means of the circuit according to the present invention, particularly adapted for vector and trigo-

nometric calculation, which is required for the monitoring of AC drives;

- Figure 3 is a block diagram which illustrates electrical circuit elements and electronic devices which are significant for the efficient provision of the functions shown in figure 2, according to the principle shown in Figure 1;
- Figure 4 is a circuit diagram of the excitation mode of a resolver the output signals of which are processed by the circuit according to the present invention; and
- Figure 5 is a view of the excitation waveform;
- Figure 6 is a schematic view of a method for unifying the processing of analog and digital signals implemented by the circuit according to the present invention.

[0020] In all the figures, identical reference numerals designate identical elements.

[0021] With reference to the above figures, Figure 1 is a conceptual block diagram of the direct processing circuit according to the present invention.

[0022] A plurality of analog input signals of the vectorial type, indicated by refernces a_1-a_n, are fed into multiplexing means 1, which select one signal at a time, which is fed into digital/analog multiplying means 2, which perform multiplication between the analog signal that arrives from the multiplexing means 1 and a digital input, designated by the reference numeral 3 and described hereinafter, in order to obtain in output an analog output signal 4 which is sent to sample-and-hold means 5, which are addressed by an address 6 emitted by means 7 for integrating digital and logic functions.

[0023] The means 7 also emit an input address 8 which is meant to drive the multiplexer 1 to select an analog input signal to be processed.

[0024] The outputs of the sample-and-hold means 5, which are meant to store the result of operations performed in the multiplying means 2, are of the analog type and are designated by O_1-O_n.

[0025] Some outputs are also fedback, as analog data, to the multiplexing means 1 and others are fedback to the logic and digital function integration means 7 after passing through second integrating means 10, which are connected to the digital and logic function integrating means 7.

[0026] The means 7 are bidirectionally connected to a digital processor 33 by means of a bus 11.

[0027] The numeric output data from the logic and digital function integration means 7, designated by the reference numeral 12, are converted into the digital inputs 3 by means of conversion tables 13 which are described hereinafter.

[0028] The conversion tables 13 are specifically created according to the type of operation required and performed on the basis of the numeric data 12.

[0029] The above-described circuit is suitable for performing numeric operations directly on analog-type signals (or on signals that are numeric but must be converted into analog signals or viceversa). Among the operations that the circuit is capable of performing, D/A conversion, sums and subtractions of analog signals modified numerically, execution of functions (trigonometric, exponential, etcetera) on the signals (by using the tables 13 that implement the chosen functions) can be mentioned.

[0030] The various functions are therefore executed one at a time, with a preset timing, and sequentially one after the other.

[0031] In many cases that are particularly interesting as regards application, the signals in input to the multiplexer I are of the vectorial type with just two components.

[0032] With reference now to Figure 2, the configurations and the means that are particularly adapted in the specific case are described. This layout illustrates means 15 which are suitable to invert the order of the two components of the analog input signals a_1-a_n, as required in order to use the special structures of the D/A multiplying means, designated by the reference numeral 2.

[0033] In detail. the inverting means 15 receive in input a signal 16 which controls the inversion of the order of the components. Said signal 16 comes from the logic and digital junction integration means 7 (such as for example a PGA, Programmable Gate Array). The D/A multiplying means 2 are represented. in this layout, by first multiplying means 21 and second multiplying means 22 which are arranged so as to multiply the two components of the analog vector signal fed to the multiplexing means 1.

[0034] Two channels. leading to said multiplying means 21 and 22 respectively, are defined.

[0035] A first channel, in output from the inverting means 15, is defined by a first gain K_4 through which the "upper" component of the signal a_H of the upper channel in output from the inverting means 15 passes. Said signal is then fed along two different paths to an adder node 25, directly in output from the gain K_4 and passing through a second gain β and the multiplying means 21.

[0036] The node 25 sums the signals that follow these two paths of the first channel.

[0037] The second channel relates to the "lower" component of the vector signal, which is designated by a_L and is sent to the second multiplying means 22 to be subsequently added in a node 27. Said node 27 receives in input the component in output from the node 25, designated by O_H, and the component in output from the multiplying means 22, designated by O_L.

[0038] The signal produced by the sum is then fed to amplifying means 30 and then sent to the sample-and-hold means 5.

[0039] As mentioned in relation to the block diagram of Figure 1, part of the analog outputs of the sample-and-hold means 5 is fed back to the multiplexer 1, while

another one of the analog outputs. which constitutes the position tracking error, is sent to error integrating means 31. Means 31 produce in output a velocity signal 32 which is particularly useful when using a position transducer of the resolver type, in which the position error signal is used to reconstruct and track the electrical angle of the resolver.

[0040] In the case of calculation of trigonometric functions, the tables 13 comprise the necessary entries for the sine and cosine functions, which can be accessed by various variables by means of the numeric data 12.

[0041] The multiplying means 21 and 22, provided for example by means of networks of the R-2R type, perform multiplication between an analog signal and a numeric datum, which can correspond to a conversion from digital to analog if the analog input is a constant.

[0042] In the circuit thus provided, the sine and cosine functions can be constructed appropriately as a sequence of segments described only in the angular interval between 0 and $\pi/4$. Due to the particular configuration of the circuit, it is in fact sufficient to consider the interval between 0 and $\pi/4$ to store the numeric values required to compose the trigonometric functions over the entire angular range. The fact that the sine is described and provided only for the angle between 0 and $\pi/4$, like the cosine, allows to improve the overall resolution of the system.

[0043] The constants K_4 and β are factors delimiting the variation range of the gain that can be applied to the upper channel and therefore to the component a_H in output from the order inverting means 15.

[0044] In practice, the circuit according to the invention unifies, in a time-sharing mode, the functions of programmable calculation, particularly of the trigonometric type, of decoding transducer signals (which have an analog information content) and D/A conversion. This is obtained by means of the specialization of D/A circuits (the multiplying means 21 and 22). Said means 21 and 22 are able to process in a differentiated manner the two components of the analog input vector. Such components are selected in an appropriate order so as to generate the individual analog output as a function of numeric data provided by the digital and logic function integration means 7 by means of the entries contained in the tables 13.

[0045] Figure 3 is a block diagram illustrating electrical circuit elements and electronic devices significant for the efficient provision of the functions indicated in Figure 2.

[0046] This diagram illustrates the means meant to attribute a sign to the components of the analog input vector signal, as required in order to determine the sign of the functions of the numeric data and therefore the sign of the analog output.

[0047] Sign reversing means 40 and 41 are connected in pairs in output to the inverting means 15. The outputs of the sign reversing means are sent to selecting means 50 and 51, which select the signal with the required sign and send it to the multiplying channels.

[0048] The multiplying means 21 and 22 are constituted by two R-2R networks 34 which are integrated in a single electronic device, performed in order to limit the uncertainty between the two networks. However, said uncertainty, which is generally equal to approximately 1%, is equivalent to the introduction of a small but significant gain error when an angular segment is selected.

[0049] Critical selections are at multiples of $\pi/4$. Accordingly, a fourth-harmonic error with respect to the argument is generated, and this requires a gain setting circuit (for the high channel with respect to the low channel) implemented on one of the two channels.

[0050] In the illustrated case, the higher channel has been selected by means of the gain K_4.

[0051] The currents in output from the R-2R networks 34 are added together by using an amplifier 35; the feedback of said amplifier is closed by means of a resistor R2 which is contained in the network 34 and has the same value as the resistor R of the R-2R network. By using the resistor R1, equal in value to the resistor R2, the signal in output from the gain K4 is added. The circuit described here corresponds to a particular embodiment of the adder nodes 25 and 27 shown in Figure 2.

[0052] The above-described circuit is. as a whole, particularly suitable to perform the accurate demodulation of the signals of a resolver.

[0053] In known AC drives, and particularly in high-performance AC drives used in servo drives, in most cases there is an angular position transducer, preferably provided by means of a resolver, which is usually connected mechanically to the shaft of the motor.

[0054] The analog vector signal with two components in output from the resolver is sent in input to the multiplexing means I as one of the input signals a_1-a_n.

[0055] The input signals, after passing through the inverting means 15, the sign reversing means 40, 41 and the selecting means 50, 51, are conveniently processed by means of functions contained in the tables 13. The input numeric data of tables 13 arrive from the digital and logic function integration means 7 and in particular from counting means 42, for example a numeric counter, the output numeric datum 45 of which represents the reconstructed electrical angle of the resolver. The analog signal in output from the block 30 represents, in the execution of this specific task, an error signal between the real angle and the reconstructed angle of the resolver which, after passing through the sample-and-hold means 5, produces the sampled tracking error signal 43. Said signal 43, after passing through the analog integrating means 31, which provide a signal which is proportional to the velocity, is converted into a signal whose frequency contains the velocity information. This is achieved by converting means 44 such as a voltage-controlled oscillator. The numeric datum 45 is therefore derived by numeric integration of the signal in output from the converting means 44 and represents the reconstructed angle of the resolver.

[0056] The numeric data 45 are also stored in a register 46 which is contained in the means 7, which also contain other registers which are generally designated by the reference numeral 47. The registers 47 contain other data derived from the numeric datum 45 and numeric data coming from the bus 11. The management of these registers is entrusted to the addressing logic means 48. In the execution of other operations, the tables 13 are addressed by numeric data contained in the register 46 or in the registers 47.

[0057] The resolver used to obtain the angular position of the mechanical angle is, in modern embodiments, of the brushless type. In any case, the resolver must be supplied (rotor voltage) by an AC voltage of appropriate frequency: a sinusoidal voltage, termed excitation voltage, is usually used.

[0058] The present invention allows to excite the resolver by using, instead of the sinusoidal voltage, a trapezoidal voltage, as derived efficiency from a square wave by natural switching, for example, of MOSFET transistors of a stage put downstream of integrating means 7.

[0059] In the specific case, the excitation signal of the resolver is obtained from a circuit shown in Figure 4.

[0060] The behavior over time of the resolver excitation signal, indicated by V_{ecc}, is plotted in Figure 5 together with the signals V_1 and V_2.

[0061] The signals V_1 and V_2 are generated by the logic and digital function integrating means 7. They are used as the control signals of the MOSFETs 60 and 61.

[0062] In the time period t_1, the signal V_2 assumes a value which is appropriate to keep the MOSFET 61 on, while the signal V_1 assumes a value which is adapted to keep the MOSFET 60 off. The voltage V_{ecc} is negative and its value is a function of the supply voltage V_1 and of the transformation ratio of the transformer 63.

[0063] In the time period t_2, both MOSFETs 60 and 61 are kept off. In this interval, due to the capacitors 64 and 65 and to the transformer 63, the voltage V_{ecc} switches, in a natural manner, from the negative value to a symmetrical positive value for which it is possible to bring the MOSFET 60 to the on state.

[0064] This value of the signal V_{ecc} is then maintained for all the period t_3 until the MOSFET 60 is brought to the off state again.

[0065] In the period t_4, in which both MOSFETs are off again, the opposite natural switching of the voltage V_{ecc} occurs, thus completing the periodic cycle, without any thermal and electromagnetic emissions correlated with forced switchings.

[0066] The main advantages of square-wave excitation are as follows.

[0067] The excitation system uses nondissipative stages. This fact allows to integrate the excitation stage even on signal boards, using surface-mount components. This is possible even in the case of low-impedance resolvers, which are needed in the case of long connections between the resolver mounted on the motor and the electronic demodulation circuit, executed according to the invention, which is physically provided in the converter.

[0068] Square-wave excitation is particularly useful when it is necessary to sample the signal supplied by the resolver. Differently from sinusoidal excitation, in which sampling should occur on the maximum of the waveform, which is difficult to define, in the case of square-wave excitation sampling occurs on a plateau after an adapted settling time. Accordingly, a time variation of the instant at which sampling occurs (within certain limits, of course) has a scarcely significant effect on the value of the sample, accordingly increasing the repeatability of the measurement, other conditions being equal.

[0069] A further advantage which arises from the use of the circuit according to the invention, particularly according to the block diagram of Figure 3, is that the decoding of signals arriving from the resolver by means of a tracking loop system is facilitated and simplified.

[0070] In the particular case of power converters dedicated to controlling brushless and reluctance motors, the circuit constitutes the means for processing the transducer signals of a resolver.

[0071] In practice it has been observed that the circuit according to the invention fully achieves the intended aim, since it allows to perform a method for unifying the processing of digital and analog signals by performing operations in time-sharing mode on said signals.

[0072] Said method for unifying the processing of analog and digital signals, particularly in AC electric drives, comprises the steps that are described hereinafter, referring to figure 6.

[0073] At step 100 analog input signals 99 are sent to multiplexing means 1 in order to select one of said analog input signals. At step 101 analog output signals are obtained from said multiplexing means 1 as a function of addressing signals 93 and predefined numeric data 98. At step 102 digital signals 96, derived from numeric data, are received. At step 103, in a time-sharing mode, a multiplication between said analog signals 99 and said digital signals 96 is performed in order to obtain analog output signals 92. At step 104 said analog output signals 92 are submitted to sample and hold processing obtaining signals 91. A part 93 of said analog output signals 91 is fed back, at step 105, to address said multiplexing means 1. Another part 90 of said analog output signals is sent, at step 105, to said integrating means 10. At step 106 said analog output signals 90 are integrated and sent, at step 107, to said logic and digital function integrating means 7. Frequency conversion of said analog output signals 90 is then performed at step 112.

[0074] The resulting analog signals 89 are stored in a register at step 113. At step 108 numeric data from means 7 are converted into digital signals by means of conversion tables storing functions to apply to said numeric data. Said digitale signal are send to be acquired (step 102) by said multiplying means.

[0075] Signals 97 and 95 are sent by said logic and digital function integrating means 7 for addressing said multiplying means (at step 103) and said sample-and-hold means (at step 104).

[0076] Signals 98 are sent by said logic and digital function integrating means 7 for addressing said multiplexing means (at step 101)

[0077] The processing circuit and the method thereof thus conceived are susceptible of numerous modifications and variations, all of which are within the scope of the inventive concept; all the details may also be replaced with other technically equivalent elements.

[0078] In practice. the devices and materials employed, so long as they are compatible with the specific use, as well as the dimensions, may be any according to requirements and to the state of the art.

Claims

1. A direct processing circuit for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in AC electric drives, characterized in that it comprises means for integrating logic and digital functions which are connected to a digital processor and are adapted to send digital signals to means for multiplying digital/analog signals, said multiplying means receiving in input analog signals which are meant to be multiplied with said digital signals in order to obtain analog output signals as a function of preset numeric data said means for integrating logic and digital functions driving said multiplying means in time-sharing mode.

2. The circuit according to claim 1, characterized in that it comprises multiplexing means adapted to receive in input analog vector signals for selecting one of said analog vector signals and subsequently sending it to said multiplexing means, said multiplexing means being addressed by said logic and digital function integration means.

3. The circuit according to claim 1, characterized in that it comprises sample-and-hold means which are adapted to receive in input the analog output signals of said multiplying means.

4. The circuit according to claim 3, characterized in that part of the outputs of said sample-and-ho1d means is sent in input to said logic and digital function integration means.

5. The circuit according to one or more of the preceding claims, characterized in that another part of said outputs of said sample-and-hold means is fedback in input to said multiplexing means.

6. The circuit according to one or more of the preceding claims, characterized in that the digital signals in input to said multiplying means are derived from numeric data output by said logic and digital function integrating means and converted by means of presettable conversion tables, said conversion tables storing functions to be applied to said numeric data.

7. The circuit according to one or more of the preceding claims, characterized in that it comprises second integrating means, which are adapted to receive in input said other part of said outputs of the sample-and-hold means and the output signals of which are input to said logic and digital function integrating means.

8. The circuit according to one or more of the preceding claims, characterized in that said sample-and-hold means are addressed by said logic and digital function integrating means.

9. The circuit according to one or more of the preceding claims, characterized in that it comprises means for inverting the order of the two components of said analog signals in output from said multiplexing means.

10. The circuit according to one or more of the preceding claims, characterized in that said multiplying means comprise first multiplying means and second multiplying means for the separate multiplication of the components of said analog signals in output from said multiplexing means.

11. The circuit according to one or more of the preceding claims, characterized in that it comprises sign reversing means and selecting means which are arranged between said means for inverting the order and said multiplexing means.

12. The circuit according to one or more of the preceding claims, characterized in that said analog signals in input to said multiplexing means comprise a vector signal with two components which originates from an angular position transducer of a motor shaft.

13. The circuit according to one or more of the preceding claims, characterized in that said angular position transducer is a resolver.

14. The circuit according to claim 13, characterized in that said multiplying means generate an analog angle error signal which is sent to said sample-and-hold means in order to generate a sampled error signal which is adapted to be sent to said second integrating means, which provide in output a signal

which is proportional to the analog velocity of said motor shaft to which said resolver is applied.

15. The circuit according to claim 14, characterized in that it has frequency converting means which are adapted to convert said signal proportional to the velocity into a corresponding frequency, said converted signal being sent to counting means, said converting means and said counting means being provided in said means for integrating logic and digital functions.

16. A direct processing method for unifying the processing of analog and digital signals in control and monitoring circuits, particularly in AC electric drives, characterized in that it comprises the steps of:

- obtaining analog output signals as a function of predefined numeric data;
- obtaining digital signals derived from numeric data which originate from means for integrating logic and digital functions and are converted into said digital signals;
- performing, in a time-sharing mode, a multiplication between said analog signals and said digital signals in order to obtain analog output signals.

17. A method according to claim 16, characterized in that it comprises a step of:

- sampling and holding said analog output signals and in sending part of said analog output signals to said logic and digital function integration means.

18. A method according to claim 16, characterized in that it comprises a preliminary step of:

- sending said analog input signals to multiplexing means in order to select one of said analog input signals.

19. A method according to one or more of claims 16 to 18, characterized in that it comprises the steps of:

- feeding back to said multiplexing means another part of said analog output signals;
- sending another part of said analog output signals to integrating means.

20. A method according to one or more of claim 19 characterized in that it comprises a step of:

- integrating the analog output signals sent to said integrating means;
- sending said analog output signals after their integration to said logic and digital function integrating means.

21. A method according to one or more of claim 20, characterized in that it comprises a step of:

- performing the frequency conversion of said analog output signals after their integration.

22. A method according to one or more of claims 21, characterized in that it also comprises a step of:

- storing said analog signals in a register after their frequency conversion.

23. A method according to one or more of claims 16 to 22, characterized in that it comprises the step of:

- converting the numeric data from said logic and digital function integrating means into digital signals by means of conversion tables which store functions to be applied to said numeric data.

24. A method according to claim 23, characterized in that it comprises the following step:

- sending said digital signals to said multiplynig means.

25. A method according to one or more of the previous claims, characterized in that it comprises the following step:

- addressing said multiplying means and said sample-and-hold means by signals derived from said logic and digital function integrating means.

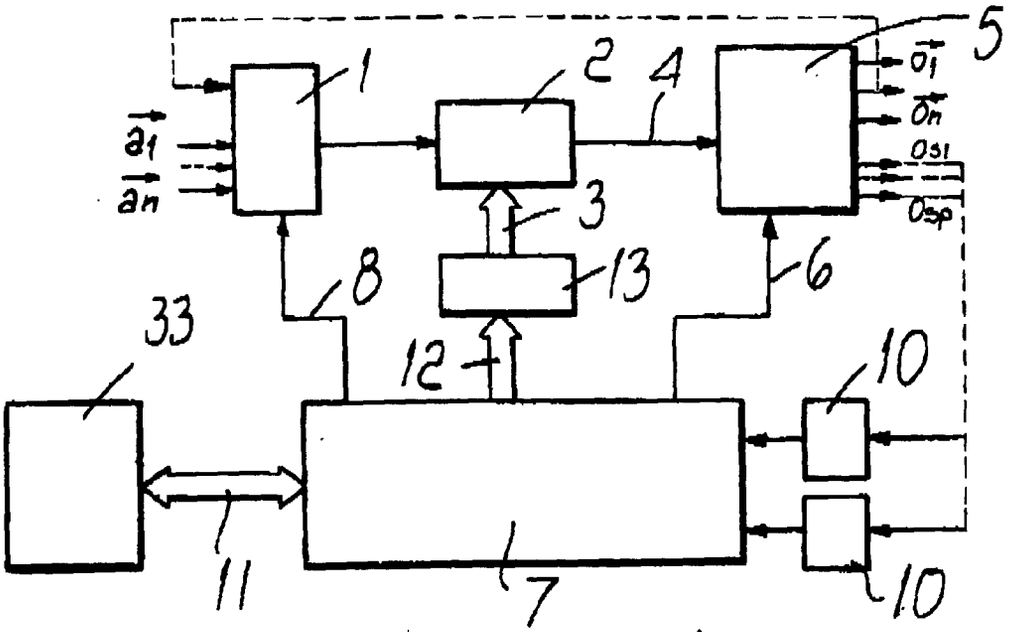


FIG. 1

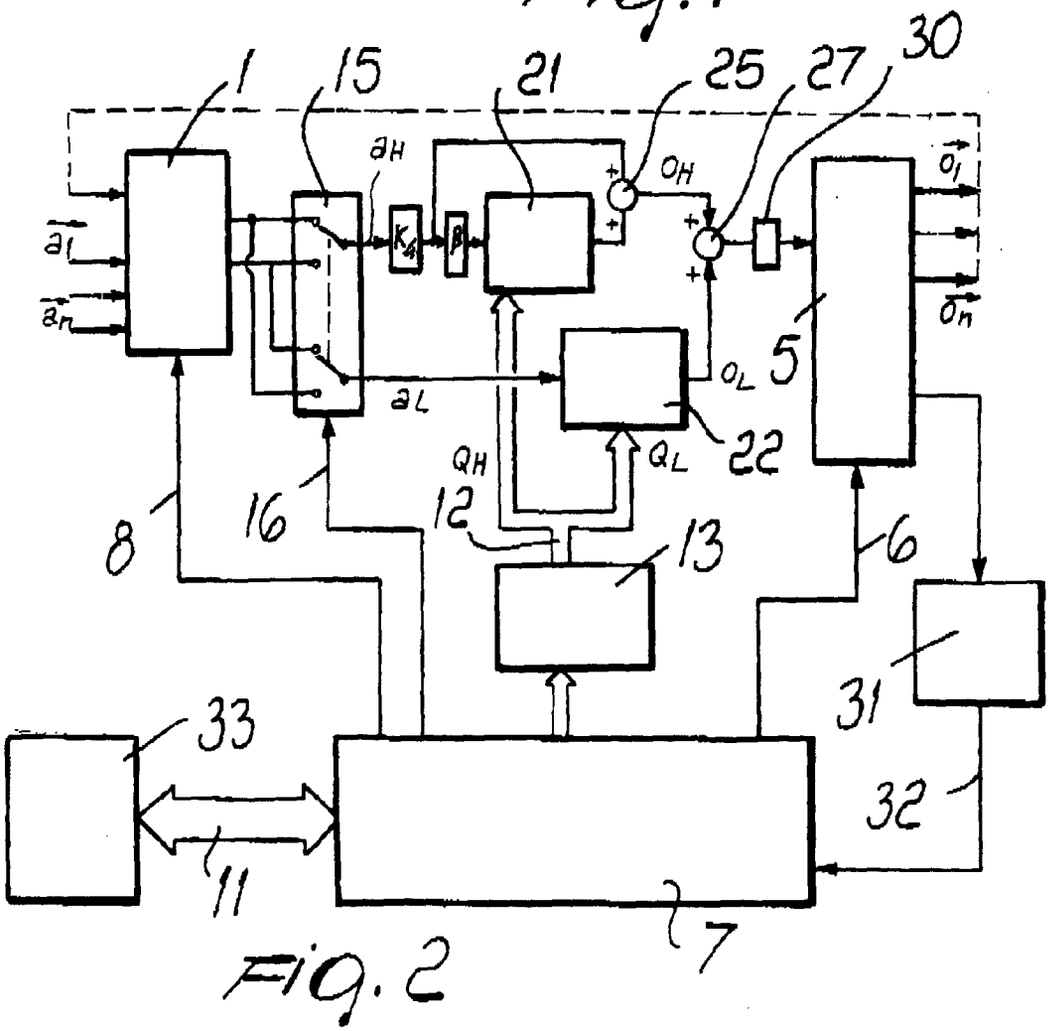
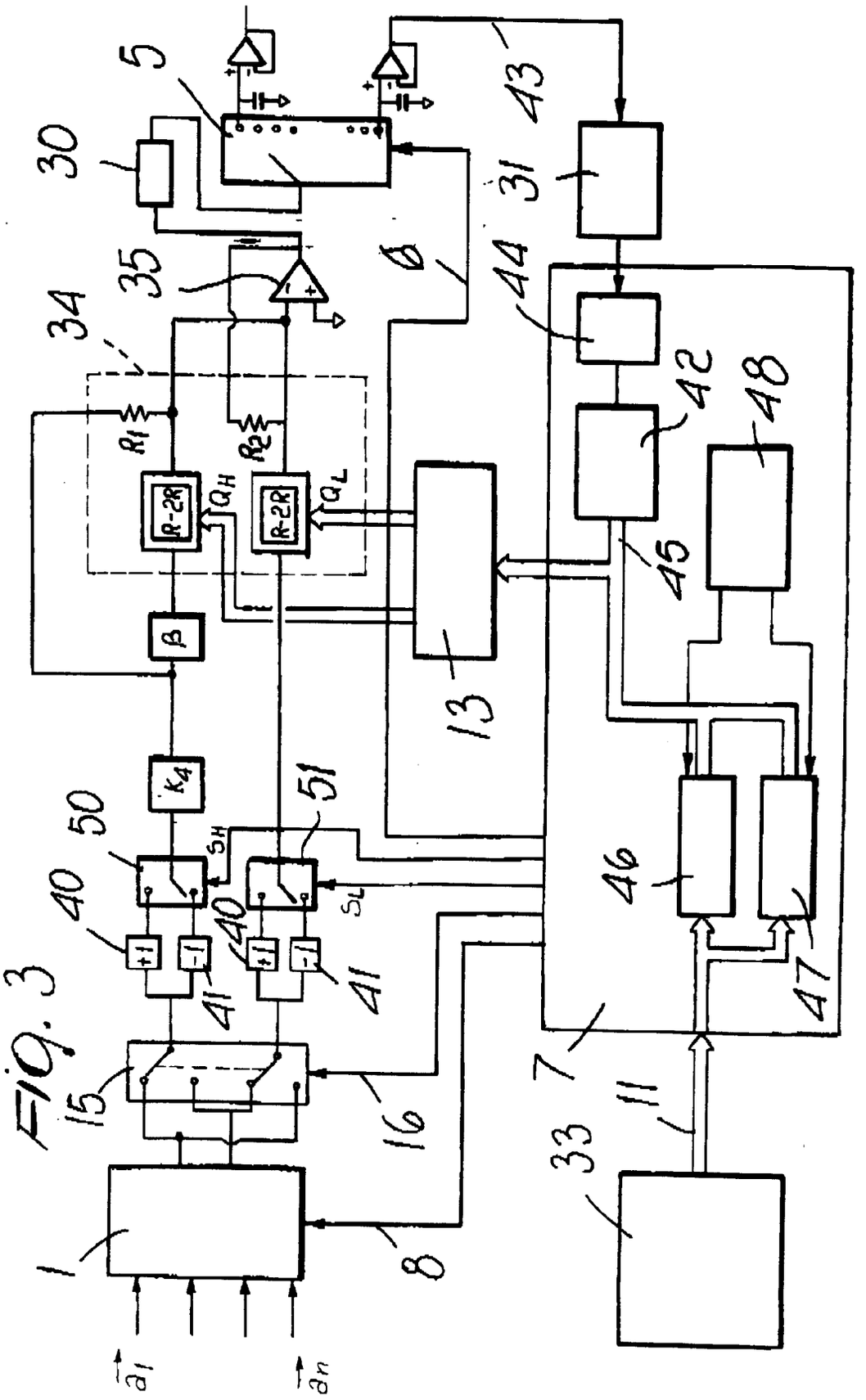


FIG. 2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51
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40
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-1
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FIG. 3

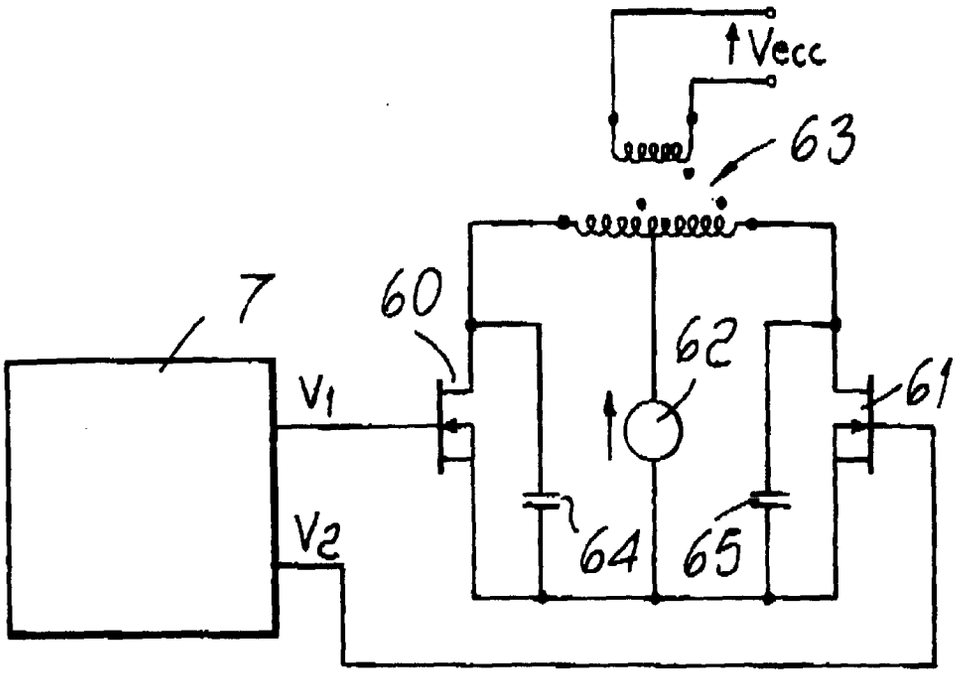

FIG. 4

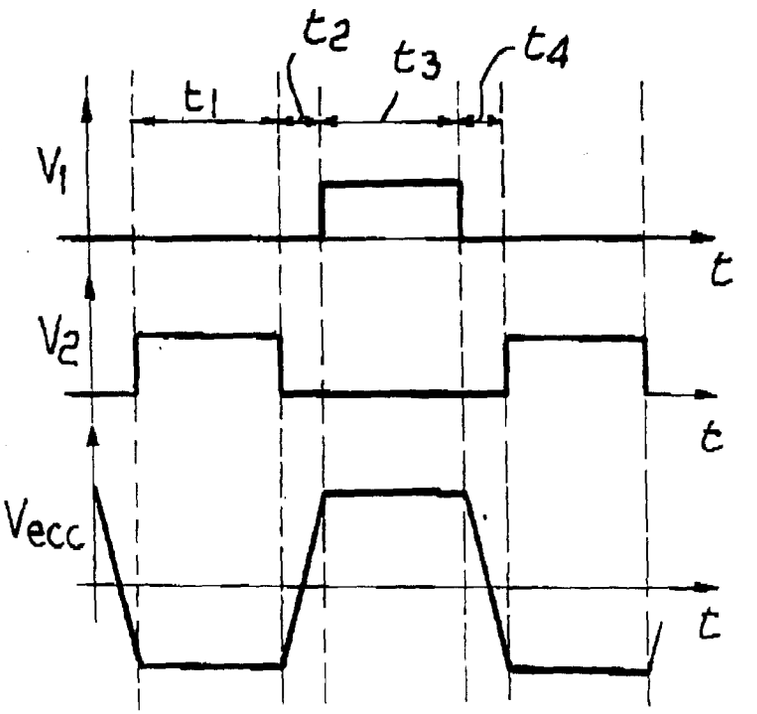

FIG. 5

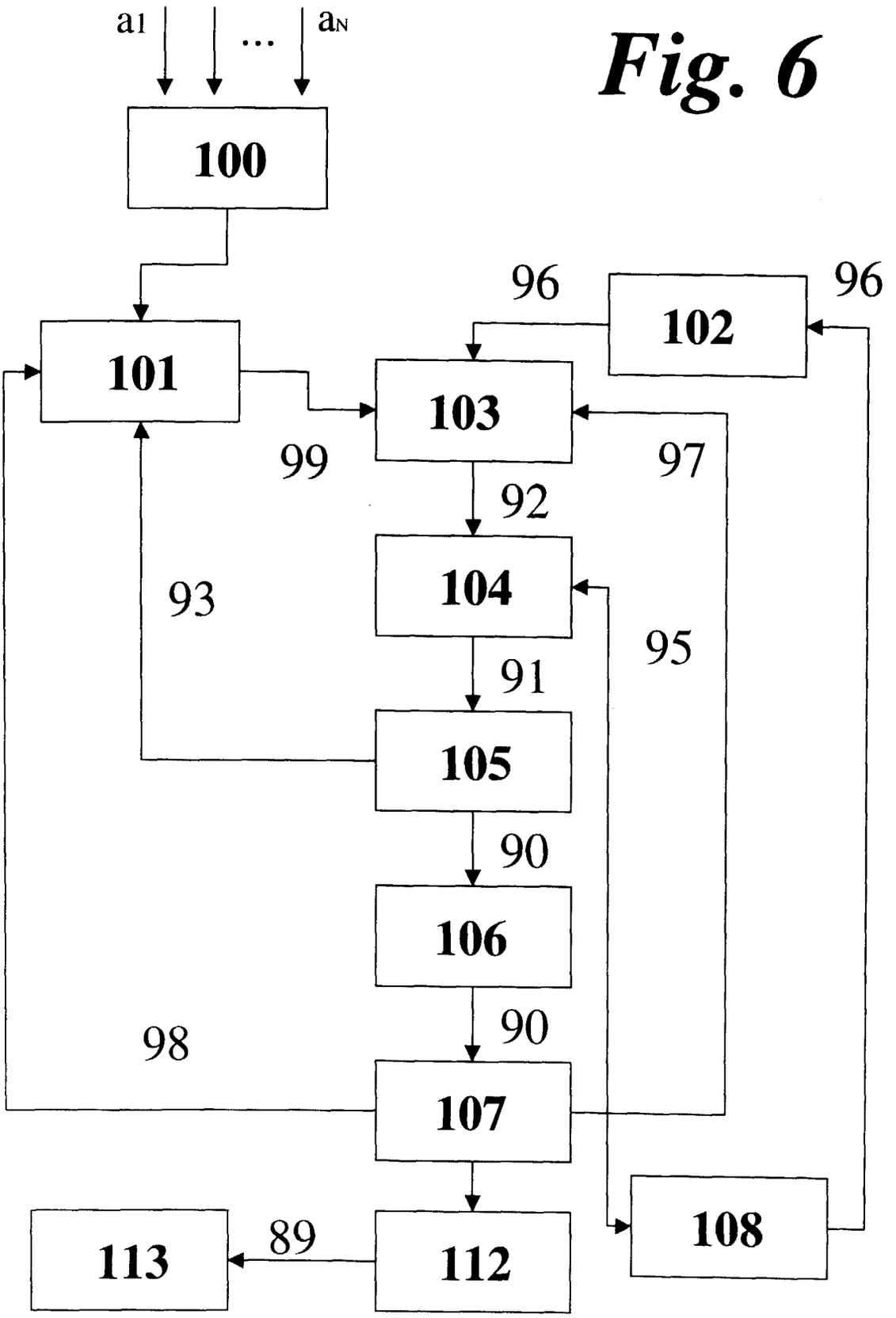
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Fig. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 20 1092

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 150 472 A (KOLLMORGEN TECH CORP) 7 August 1985 (1985-08-07) * abstract * * page 5, line 15 - page 9, line 4 * * page 15, line 23 - page 20, line 21 * * figures 1,5 *	1,6,16, 23,24	H02P5/40 G05B19/414
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 July 1999	Hurtado-Albir, J

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

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