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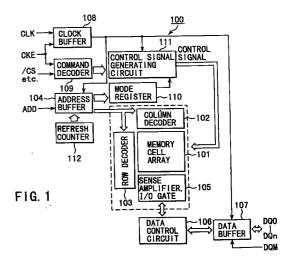
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(54) Semiconductor memory system, and access control method for semiconductor memory and semiconductor memory

In a semiconductor memory system, an SDRAM comprises a memory cell array (101) which is divided into a plurality of cell array blocks (21), a column decoder (102), a row decoder (103), and a sense amplifier circuit (105). In the SDRAM, a first operation mode with a first cycle time is set when successive access within a cell array block (21) is conducted, a second operation mode with a second cycle time shorter than the first cycle time is set when successive access covering the cell array blocks (21) being apart from each other is conducted and a third operation mode with a medium cycle time is set when successive access covering the cell array blocks (21) adjacent to each other is conducted. With the above constitution, a high speed access can be realized without provision of a specific accessory circuit while suppressing overhead for a semiconductor chip size.





EUROPEAN SEARCH REPORT

Application Number EP 99 10 8592

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Category	Citation of document with of relevant pass	indication, where appropriate, sages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

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