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(54) Voltage regulator

(57) A voltage regulator 10 comprises a differential amplifier arrangement 50,60,70 having a first 51 and second 52 inputs and an output 71. A switched capacitor feedback means 100 has an input connected to the output 71 of the amplifier arrangement via a first sampling means 101 and an output 71 of the amplifier arrangement via first sampling means 101 and an output connected to the second input 52 of the amplifier arrangement via a second sampling means 102.

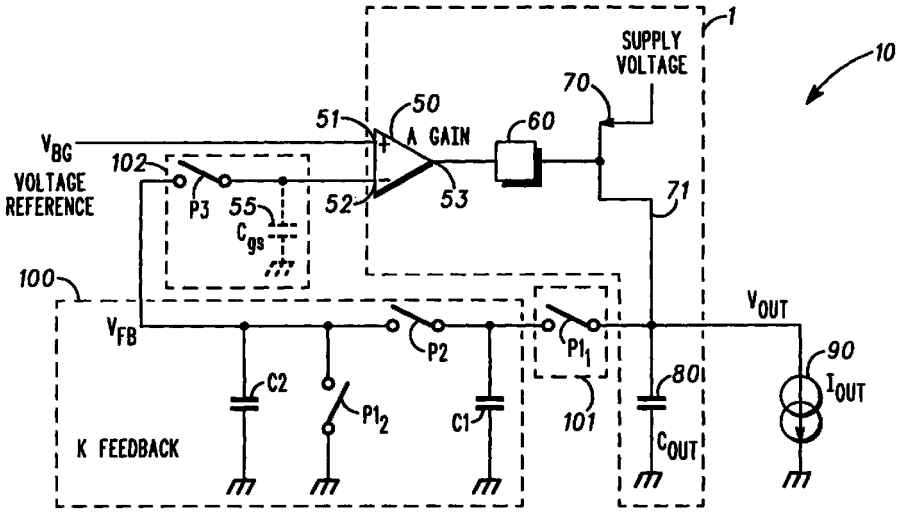


FIG.1

EP 0 981 077 A1

Description

Field of the Invention

[0001] The present invention relates to a regulator and a method of regulating a signal and in particular to a voltage regulator and a method of regulating a signal for use in portable communication devices.

Background of the Invention

[0002] A typical mobile phone has a number of voltage regulators several of which must be turned on, and therefore be consuming power while the phone is in standby mode. The power consumed by such voltage regulators typically accounts a major fraction of the total current consumed by the mobile phone when it is in standby mode. A conventional such voltage regulator may consume, for example, approximately 30 microamps.

[0003] A typical fully analogue voltage regulator such as is commonly found in portable communication devices such as mobile telephones has the basic structure of a differential amplifier arrangement having first and second differential inputs and an output from which the regulated voltage signal is taken and a feedback means in the form of a resistor ladder from which a feedback voltage is derived and input to one of the differential inputs where it is compared with a reference voltage which is applied to the other of the differential inputs. In order to ensure that a voltage regulator of this nature is stable (i.e. non oscillatory) the transfer function of the entire circuit must be such that for all frequencies below a certain cut off frequency at which the gain of the circuit has fallen to 0dB the phase change of the output signal is greater than 0. The differential amplifier arrangement of such a regulator will generally comprise three amplification stages, one amplification stage provided by a power P-MOSFET, another amplification stage associated with an intermediate transistor stage and a further amplification stage provided by an operational amplifier (op-amp). Each of these amplification stages will generate an associated pole in the transfer function of the entire circuit. A first pole ω_1 associated with the power P-MOSFET and its associated capacitor, a second pole ω_2 associated with the intermediate transistor stage and a third pole ω_3 associated with the op-amp. In order to achieve stability, the voltage regulator is generally designed to have the first pole ω_1 at a fairly low frequency, the second pole ω_2 at a much higher frequency and the third pole ω_3 at frequency which is sufficiently higher than that of ω_2 such that the additional phase roll off caused by ω_3 only occurs at a frequency above the cut off frequency at which 0 dB gain has been reached.

[0004] In order to ensure that the third pole ω_3 associated with the operational amplifier occurred at a sufficiently high frequency to ensure stable operation of the voltage regulator, in a conventional voltage regulator such as that described above, it was generally necessary to supply a current of at least 12 microamps to the operational amplifier. Furthermore, the resistor ladder feedback means would generally consume about 15 microamps.

[0005] It is therefore apparent, that in order to reduce the power consumption of a conventional regulator, the total resistance of the resistor ladder could be increased. However, such a solution is disadvantageous in terms of the amount of silicon required to implement the resistor ladder (because large resistors take up a lot of silicon) and in terms of the accuracy of the ratio of the regulated voltage to the feedback voltage attainable (because it is difficult to achieve good matching of large resistors). The power consumption could also be reduced by reducing the amount of current consumed by the operational amplifier. However this adversly impacts the stability of the regulator.

[0006] The present invention seeks to provide a regulator and a method of regulating a signal which would enable reduced current consumption in applications such as portable communication devices.

Summary of the Invention

[0007] According to the present invention there is provided a method of regulating a signal comprising the steps of generating a regulated signal by means of a differential amplifier arrangement having first and second differential inputs; sampling the regulated signal to generate a sampled regulator signal; applying the sampled regulated signal to the input of a feedback means; generating a feedback output signal whose value depends upon the sampled regulated signal; sampling the feedback output signal to generate a sampled feedback signal applying the sampled feedback signal to the first differential input of the differential amplifier arrangement and applying a referenced signal to the second differential input of the differential amplifier arrangement.

[0008] According to a second aspect of the present invention, there is provided a regulator comprising a differential amplifier arrangement having first and second differential inputs and an output for generating a regulated signal; a first sampling means for sampling the regulated signal to generate a sampled regulated signal; a feedback means having an input for receiving the sampled regulated signal and an output for generating a feedback output signal; and a second sampling means for sampling the feedback output signal to generate a sampled feedback signal; the arrangement being such that the first differential input receives the sampled feedback signal and the second differential input receives a reference signal.

[0009] As a result of sampling the regulated signal, the transfer function of the regulator as a whole is altered significantly, but upon performing a suitable analysis of the circuit, it is found that the effect on the transfer func-

tion is that at a frequency which is related to the sampling frequency the gain of the regulator rapidly falls to 0dB. This enables the requirement on the third pole ω_3 associated with the op-amp to be greatly relaxed. This in turn enables the amount of current which the op-amp needs to consume to be reduced significantly.

[0010] Preferably the feedback means comprises a switched capacitor arrangement. This gives rise to the significant advantage that only a very small amount of current is consumed by the feedback means.

[0011] According to a third aspect of the present invention, there is provided a regulator comprising a differential amplifier arrangement having a first and second differential input and an output for generating a regulated signal and feedback means for generating a feedback output signal which depends upon the regulated signal and applying the feedback output signal to the first differential input, wherein a reference signal is applied to the second differential input and wherein the feedback means comprises a switched capacitor arrangement.

Brief Description of the Drawings

[0012] In order that the present invention maybe better understood embodiments thereof will now be described by way of example only and with reference to the accompanying drawings in which;

FIG.1 is a schematic block diagram of a voltage regulator according to a first embodiment of the present invention;

FIG.2 is a schematic block diagram of a voltage regulator according to a second embodiment of the present invention;

FIG.3 is a schematic block diagram of a voltage regulator according to a third embodiment of the present invention.

FIG.4 is a graph of the magnitude of a sample and hold transfer function against frequency; and

FIG.5 is a graph of the phase of a sample and hold transfer function against frequency.

Detailed Description of the Invention

[0013] Referring to FIG.1, up conversion voltage regulator 10 comprises a basic voltage regulator architecture (excluding the feedback means) 1, a first sampling means 101, feedback means 100, and second sampling means 102. The basic voltage regulator architecture (excluding the feedback means) 1 comprises a differential amplifier arrangement 50,60,70 and an output capacitor 80 having capacitance COUT. The differential amplifier arrangement 50,60,70 comprises an op-amp 50 having a non inverting input 51, an inverting input 52, and an output 53 and an associated capacitance 55, an intermediate transistor gain stage 60 and a power transistor 70 the output 71 of the power transistor 70 forms the output to the differential amplifier arrangement 50, 60,70 and this is connected to one plate of the output capacitor 80 the other plate of which is connected to ground.

[0014] The first sampling means 101 comprises a first phase 1 switch $P1_1$ and is connected between the output 71 of the power transistor 70 and an input to the feedback means 100. The second sampling means 102 comprises a phase 3 switch P3 in combination with the associated capacitance 55 of the inverting input 52 to op-amp 50. The second sampling means 102 is connected between an output of the feedback means 100 and the inverting input 52 to op-amp 50. Feedback means 100 comprises a second phase 1 switch $P1_2$ a phase 2 switch P2 a first capacitor C1 and a second capacitor C2. Also shown in FIG.1 is a current sink 90 connected between the output 71 of the power transistor 70 and ground. Current drain 90 represents a load supplied by the voltage regulator.

[0015] Referring now to FIG.2, down conversion voltage regulator 20 comprises the same basic voltage regulator architecture (excluding the feedback means) 1 as for the up conversion voltage regulator 10 and the same reference numerals have been used to describe corresponding elements. Down conversion voltage regulator 20 further comprises a first sampling means 201 a second sampling means 202 and a feedback means 200. The first sampling means 201 comprises a first phase 1 switch $P1_{1'}$and a second phase 1 switch $P1_{2'}$. The second sampling means 202 comprises a phase 3 switch $P3'$ together with the associated capacitance 55 of the inverting input 52 to op-amp 50. Feedback means 200 comprises a third phase 1 switch $P1_{3'}$ a phase 2 switch $P2'$ prime a first capacitor $C1'$ a second capacitor $C2'$ and a third capacitor $C3'$.

[0016] With reference now to FIG.3, an up-down conversion regulator 30 again comprises the same basic voltage regulator architecture (excluding the feedback means) 1 of regulators 10 and 20 together with a first sampling means 301 a second sampling means 302 and a feedback means 300. First sampling means 301 comprises a first phase 1 switch $P1''$and a first phase 2 switch $P2_{1''}$. The second sampling means 302 comprises a phase 4 switch $P4''$together with the associated capacitance 55 of the inverting input 52 to the op-amp 50. Feedback means 300 comprises a second phase 1 switch $P1_{2''}$a second phase 2 switch $P2_{2''}$ a third phase 2 switch $P2_{3''}$ a phase 3 switch $P3''$ a first capacitor $C1''$ a second capacitor $C2''$, a third capacitor $C3''$ and a fourth capacitor $C4''$.

[0017] The basic operation of all three regulators 10,20, 30 is that of a differential amplifier arrangement having a negative feedback such that the differential amplifier arrangement 50,60,70 varies its output in such

a way as to maintain the voltage signals at the non inverting 51 and inverting 52 inputs substantially equal. The feedback means 100, 200, 300 acts to produce a voltage V_{FB} at the inverting input 52 which is proportional to the voltage V_{OUT} output by the differential amplifier arrangement 50,60,70 (i.e $V_{FB} = KV_{OUT}$ where K is the feedback means constant of proportionality). Since the reference voltage V_{BG} applied to the non-inverting input 51 ios a very stable reference voltage, the output voltage V_{OUT} will also be very stable (provided certain stability requirements of the regulator are met which are discussed in greater detail below) and will be given by $V_{OUT} = V_{BG}/K$. As will be seen below, K may be less than unity or more than unity depending upon the structure of the feedback means.

[0018] Referring now to FIG.1 in particular, the way in which the negative feedback signal is generated and fed back to the inverting input 52 of op-amp 50 will now be described. The switches $P1_1$ to P3 of the first and second sampling means 101, 102 and feedback means 100 are all controlled by a suitable clocking or control signal which in this case includes at least three phases (or rather at least 3 signals are provided having the same frequency but differing phases, the duty cycle of each signal being sufficiently small to prevent overlay) During the first phase switches $P1_1$ and $P1_2$are turned on while the other switches are turned off. During the second phase switch P2 is turned on while the other switches are turned off; and during the third phase switch P3 is turned on while the other switches are turned off. Thus during the first phase the first phase 1 switch $P1_1$ is closed and causes the first capacitor C1 to charge up to a voltage V_{OUT} corresponding to the voltage of the output 71 of the differential amplifier arrangement 50,60,70; at the same time the second phase 1 switch $P1_2$is also dosed and acts to discharge the second capacitor C2. Note that during the first phase the phase 2 switch P2 is open such that the first and second capacitors are effectively disconnected from one another. Thus, when phase 1 ends and the first and second phase 1 switches are opened again the first capacitor C1 will hold a voltage V_{OUT} and the second capacitor C2 will hold a voltage of 0 volts. Note that at the end of the first phase the feedback means 100 is effectively disconnected again from the output 71 of the differential amplifier arrangement 50,60,70, the voltage V_{OUT} having been sampled.

[0019] When phase 2 commences the phase 2 switch P2 is closed and the first and second capacitors C1, C2 are connected together in parallel some of the charge stored on the first capacitor C1 will therefore flow to the second capacitor C2 until the voltage across both capacitors C1, C2 is equal. The new voltage will be given by:-

$$V_{FB} = V_{OUT}.\ C1/C1 + C2)$$

[0020] During the third phase the phase 3 switch P3 is dosed and the voltage of V_{FB} generated by the feedback means 100 is sampled and applied to the inverting input 52. Note that the associated capacitance 55 effectively stores this value between samples so as not to present a fluctuating input voltage since the input to the op-amp 50 draws practically no current, provided the sampling frequency is sufficiently high, the requirement for a non fluctuating input voltage will be attained. Clearly, after phase 3 has finished and the phase 3 switch P3 is opened again the first phase will recommence and the cycle carry on as before.

[0021] Thus it can be seen that voltage applied to the inverting input 52 of op-amp 50 will given by $V(C_{GS}) = V_{OUT}.C1/ C1 + C2)$.

[0022] Since the amplifier arrangement 50,60,70 will act in such a way as to ensure that the voltages at both the inputs 51,52 to op-amp 50 are substantially identical we see that $V_{OUT} = V_{BG}.(C1 + C2)/C1$ where V_{BG} is a reference voltage signal supplied to the non inverting input 51 of op-amp 50 coming from a stable reference voltage generator such as a band gap reference voltage generator.

[0023] Referring now to FIG.2, the operation of down conversion regulator 20 is similar to that of up conversion regulator 10 as described above. Thus, during phase 1 the first phase 1 switch *P*1'is closed and causes the third capacitor *C*3' to charge up to voltage V_{OUT}. At the same time the second phase 1 switch $P1_{2'}$is also closed and causes the first capacitor*C*1' to charge up to voltage V_{OUT}. Meanwhile, the third phase 1 switch $P1_{3'}$ is also closed and causes the second capacitor *C*2' to discharge to 0 volts. During the second phase the phase 1 switches $P1_{1'}$,$P1_{2'}$ and $P1_{3'}$are all opened and the phase 2 switch *P*2'is dosed which, as before, causes the charge stored in the first capacitor *C*1'to flow the second capacitor *C*2' until the voltage across both of these capacitors are equal. At this point, the voltage of the V_{FB} at the output of the feedback means 200 will be given by

$$V_{FB} = V\ (C3') + V_{INT}$$

where V_{INT} is the voltage across the first and second capacitors *C*1',*C*2'and this implies $V_{FB} = V_{OUT} + V_{OUT}.\ C1/(C1 + C2)$. Using the same principles as before, it can therefore be seen that the output voltage V_{OUT} at the output 71 of the power transistor 70 will be given by $V_{OUT}=V_{BG}/K$ where

$$K = 1 + V_{OUT}\text{'}\ C1/(C1 + C2)$$

is the constant of proportionality of feedback means 200.

[0024] Since K is necessarily greater than 1 in this case, it can seen that V_{OUT} will be less than V_{BG} thus providing a down conversion regulator as required. Note

this is not possible to achieve with a conventional resistor ladder feedback means.

[0025] With reference now to FIG.3 up down conversion regulator 30 again operates in a similar way to the previously described regulators 10,20. During the first phase the first phase 1 switch *P*1"is turned on causing the third capacitor C3" to charge to V_{OUT} while the second phase 1 switch $P1_{2"}$ is also turned on and causes the fourth capacitor *C*4"to discharge to 0 volts. During phase 2, the first phase 2 switch *P*2'double prime is dosed causing the first capacitor *C*1"to charge to voltage V_{OUT}; the second phase 2 switch $P2_{2"}$is also closed and causes the second capacitor *C*2" to discharge to 0 volts; and the third phase two switch $P2_{3"}$closes causing the charge stored in the third capacitor *C*3" to flow to the fourth capacitor *C*4" until the voltage across these two capacitors *C*3",*C*4"is equal (note this voltage V (*C*3"/*C*4") is given by V (*C*3"/*C*4") = V_{out},*C*3"/(*C*3"+ *C*4")). During the third phase the phase 3 switch *P*3"is closed causing the charge stored in the first capacitor*C*1"to flow into the second capacitor C2 '' until the voltage across these capacitors is equal (note this voltage *V*(*C*1"/*C*2")is given by *V*(*C*1"/*C*2") = V_{out},C1"/(*C*1"+ *C*2") .By the end of the third phase, the voltage V_{FB} at the output of the feedback means 300 will be given by V_{FB} = *V*(*C*3"/*C*4")+ *V*(*C*1"/*C*2") which is equal to KV_{OUT} where *K* = *C*1"/(*C*1" + *C*2") + *C*3"/(*C*3 + *C*4").

[0026] The advantage of using the up/down conversion regulator 30 in place of either the up conversion regulator 10 or down conversation regulator 20 is that values of K close to unity can be achieved with capacitors having approximately the same capacitance (whereby the capacitors may be accurately matched). In the cases of the up conversion regulator 10 and down conversation regulator 20 it would be necessary to have capacitors with very different capacitances in order to achieve values of K close to unity. This would create problems with regards to accurate matching of the capacitors. As an approximate guide the up conversation regulator 10 is suitable for generating output voltages greater than 1.2 timed the reference voltage V_{BG} applied to the non verting input 51 of the op-amp 50. The down conversion regulator 20 is suitable for output voltages smaller than 0.8 times the reference voltage V_{BG}. The up/down conversion regulator is suitable for output voltages between 0.8 and 1.2 times the reference voltage V_{BG}.

[0027] Clearly an important consideration which applies to all three of the above described regulators 10,20, 30 will be in selecting the frequency with which each complete cycle is completed. This frequency may be termed the sampling frequency f_s. The main constraint on the selection of f_s is that f_s must be chosen to be sufficiently large to maintain stable operation of the regulator. However, the lower f_s the lower is the requirement on maximising the frequency f_3 associated with the third pole W_3 associated with op-amp 50 which in turn means that the current required to be consumed by op-amp 50 maybe reduced. In order to establish the minimum sample frequency f_s at which the regulator will be stable one needs to perform an AC sweep analysis on the complete circuit. To do this one needs to take into account not only the transfer function of the amplifier arrangement 50,60,70 which is unchanged from the conventional regulator, but also the transfer function associated with the feedback path. The transfer function associated with the feedback path is that of a sample and hold operation and this transfer function is known to have the form:

$$H(s) = K(1-e^{-T_s \cdot s})/s$$

$$\text{where } Ts = \frac{1}{f_s}, s = iw, w = 2\pi \cdot f_s$$

[0028] From this it follows that the gain is given by:-

$$|H(s)| = \sin c(w \cdot T_s/2)$$

which is shown in Figure 4 and the phase is given by:-

$$[H(s)] = -180 \cdot f/f_s$$

which is shown in Figure 5.

[0029] Thus for the purposes of understanding as a first order approximation, the sample and hold operation may be considered as a transfer function with a gain equal to 0dB up to half of the sampling frequency and a linear phase delay. At frequencies over the sampling frequency the gain can be considered to be so negatively large as to make the gain of the complete circuit zero or less. A typical suitable sampling frequency f_s may be of the order of a few Mhz.

Claims

1. A method of regulating a signal comprising the steps of generating a regulated signal by means of a differential amplifier arrangement have first and second differential inputs; sampling the regulated signal to generate a sampled regulated signal; applying the sampled regulated signal to the input of a feedback means; generating a feedback output signal; sampling the feedback output signal to generate a sampled feedback signal ; applying the sampled feedback signal to the first differential amplifier arrangement; and applying a reference signal to the second differential input of the differential arrangement.

2. A method as claimed in claim 1 wherein the feedback comprises a switched capacitor arrangement.

3. A method as claimed in either one of the preceding claims wherein the differential amplifier arrangement has a transfer function which has a first, second and third pole at a first second, and third increasing pole frequency respectively and wherein the regulated signal is sampled at a sampling frequency which is greater than twice the second pole but less than the third pole frequency.

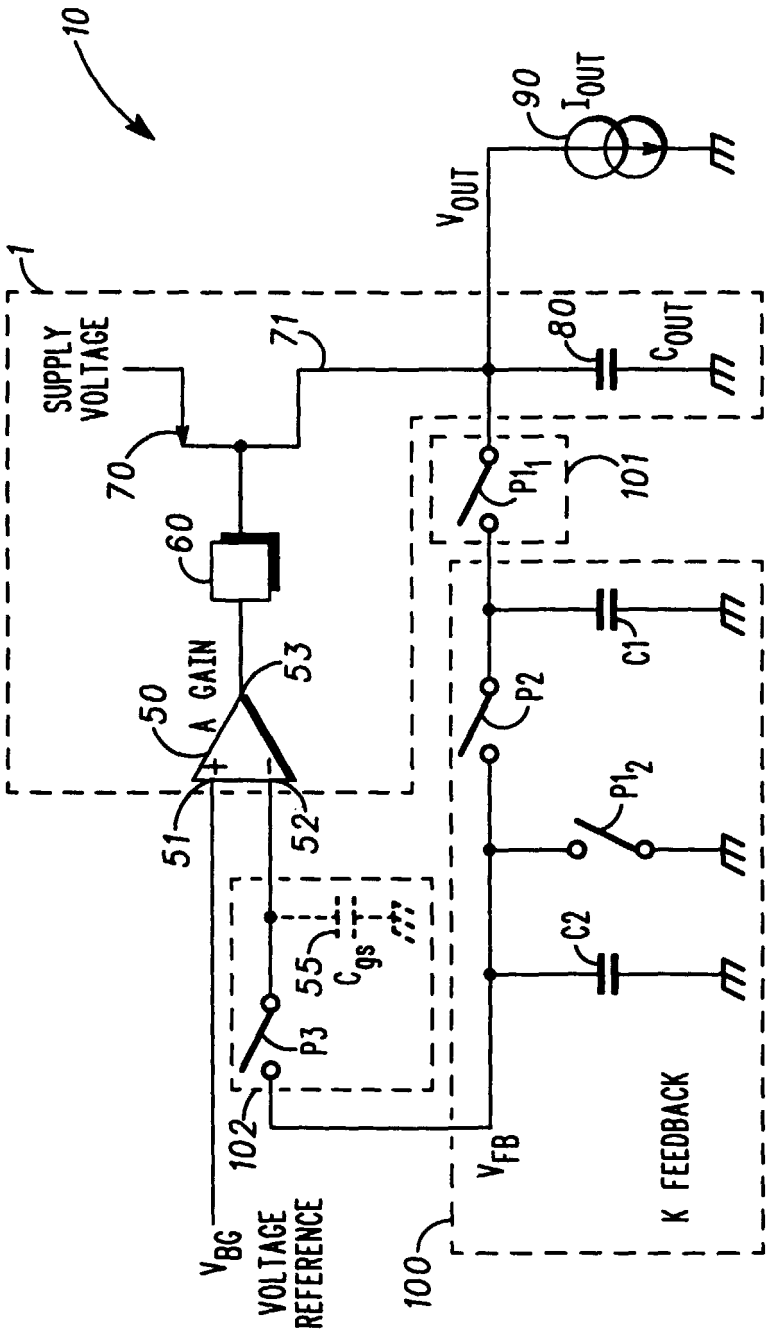
4. A method as claimed in any one of the preceding claims wherein the feedback output signal in such a way as to be greater than the sampled regulated signal whereby the regulated signal is made to be smaller than the reference signal.

5. A regulator comprising a differential amplifier arrangement having first and second differential inputs and an output for generating a regulated signal a first sampling means for sampling the regulated signal to generate a sampled regulated signal; a feedback means having an input for receiving the sampled regulated signal and an output for generating a feedback output signal; and a search sampling means for sampling the feedback output signal to generate a sampled feedback signal; the arrangement being such that the first differential input receives the sampled feedback signal and the second differential input receives a reference signal.

6. A voltage regulator as claimed in claim 5 wherein the feedback means comprises a switched capacitor arrangement.

7. A voltage regulator as claimed in either one of claim 5 or claim 6 further comprising a control means for generating one or more control signals for controlling the sampling frequency of the first and second sampling means.

8. A regulator comprising a differential amplifier arrangement having first and second differential inputs and an output for generating a regulated signal; and feedback means for generating a feedback output signal which depends upon the regulator signal and for applying the feedback output signal to the first differential input; wherein a reference signal is applied to the second differential input and wherein the feedback means comprises a switched capacitor arrangement.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1
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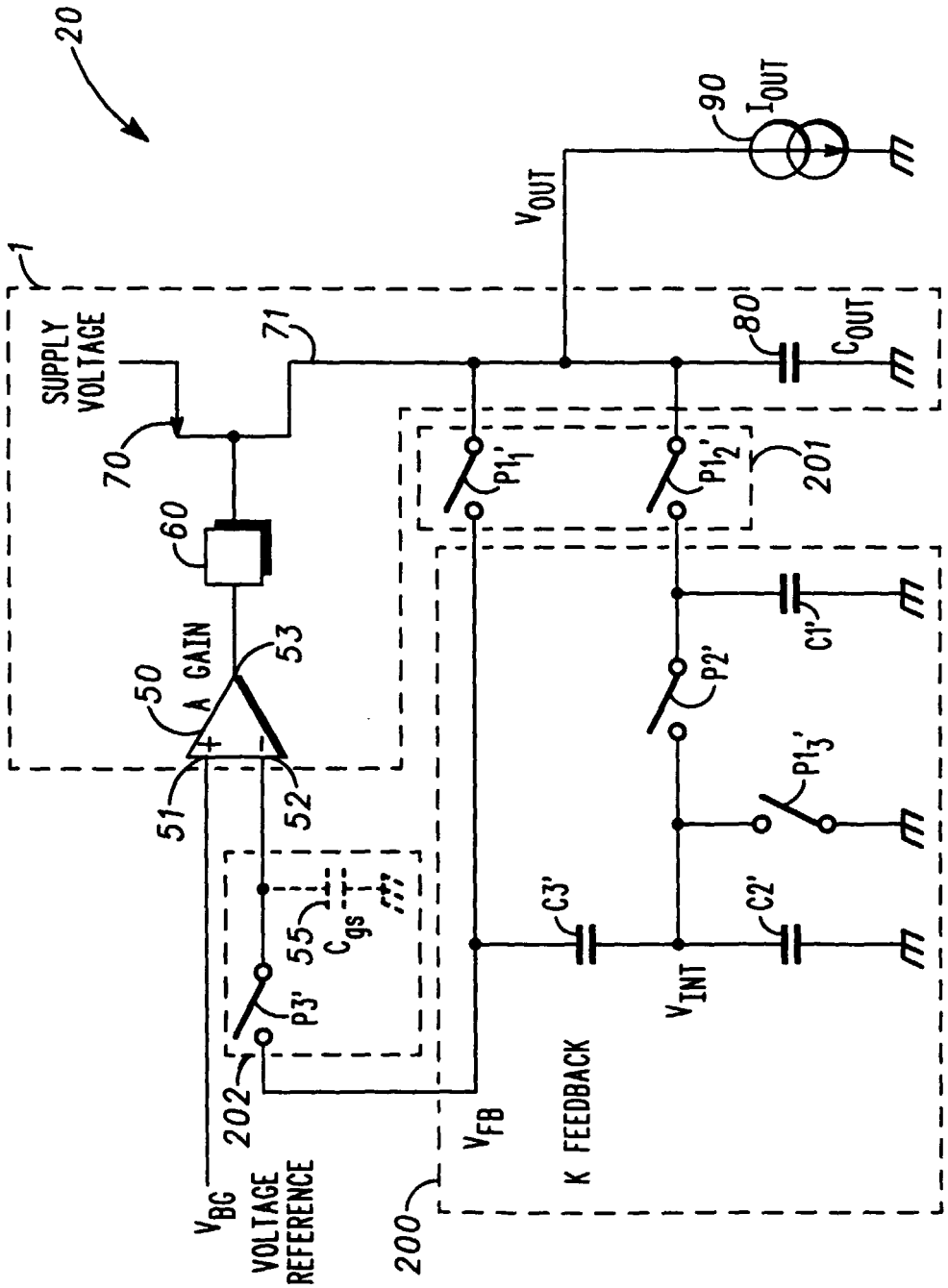
70
71
60
50
A GAIN
53
51
52
55
C_{gs}
P3
102
V_{BG}
VOLTAGE REFERENCE
V_{OUT}
90
I_{OUT}
80
C_{OUT}
$P1_1$
101
C1
P2
$P1_2$
C2
100
V_{FB}
K FEEDBACK

FIG.1


20
1
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70
71
60
50
A GAIN
53
51
52
55
C_{gs}
P3'
202
V_{BG}
VOLTAGE REFERENCE
200
V_{FB}
K FEEDBACK
V_{OUT}
90
I_{OUT}
80
C_{OUT}
$P1_1'$
$P1_2'$
201
P2'
C1'
$P1_3'$
C3'
C2'
V_{INT}

FIG.2

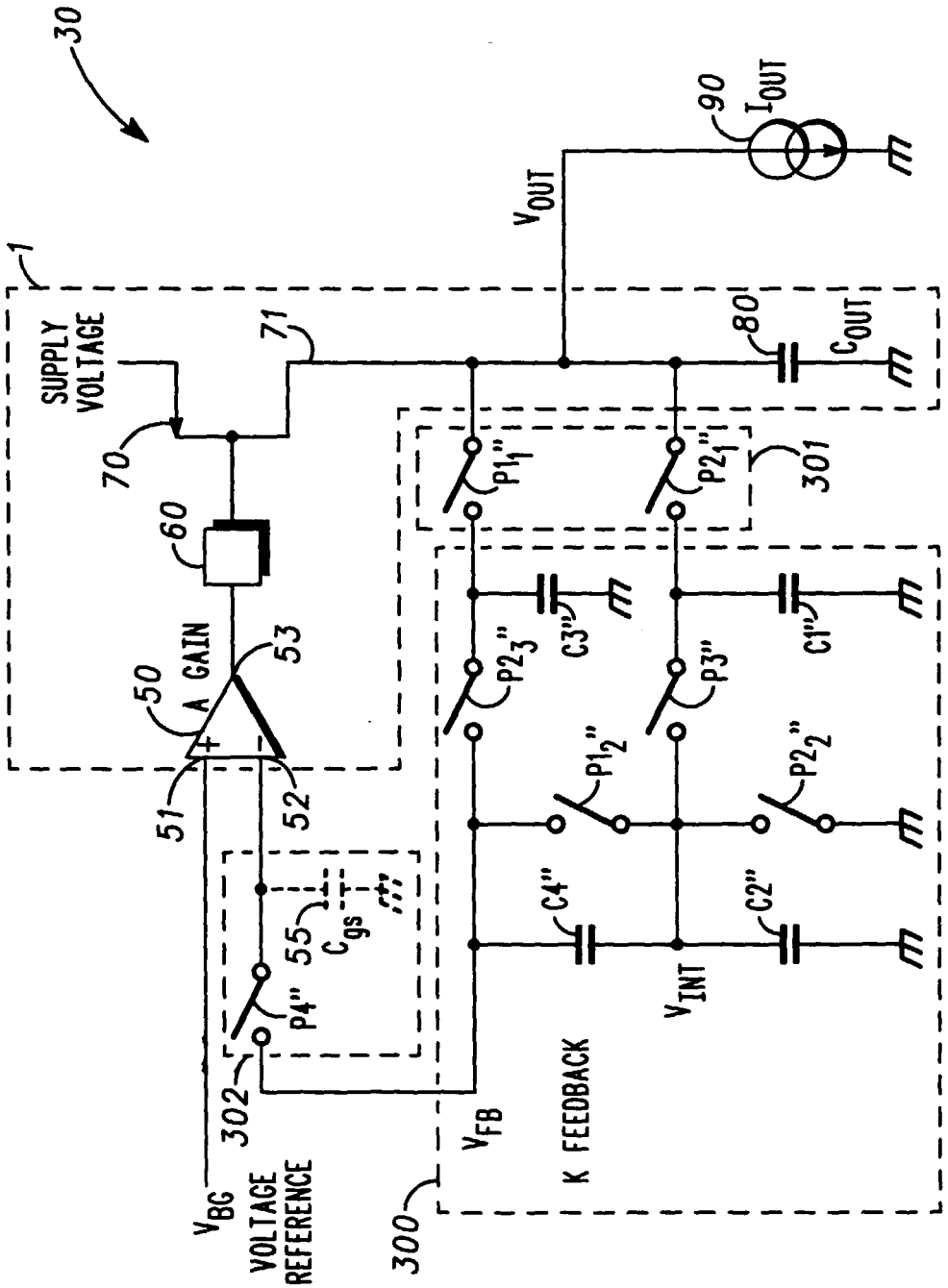
30
1
SUPPLY VOLTAGE
70
71
60
50
A GAIN
53
51
52
55
C_{gs}
P4"
302
V_{BC}
VOLTAGE REFERENCE
300
K FEEDBACK
V_{FB}
V_{INT}
V_{OUT}
90
I_{OUT}
80
C_{OUT}
301
$P1_1$"
$P2_1$"
$P2_3$"
C3"
P3"
C1"
$P1_2$"
$P2_2$"
C4"
C2"

FIG. 3

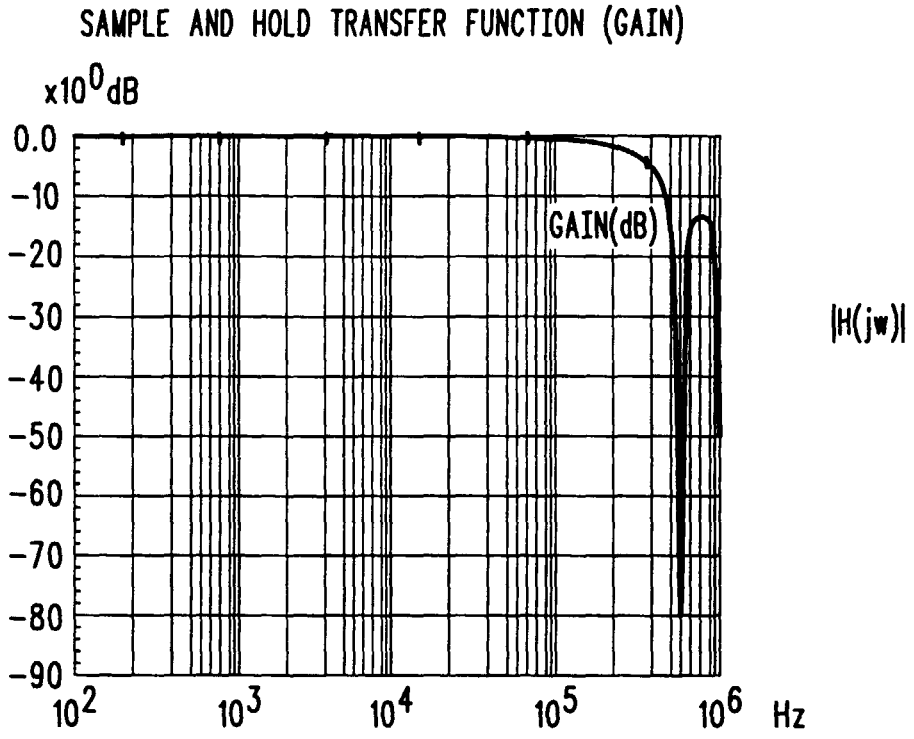
SAMPLE AND HOLD TRANSFER FUNCTION (GAIN)
x10^0 dB
0.0
-10
-20
-30
-40
-50
-60
-70
-80
-90
GAIN(dB)
|H(jw)|
10^2
10^3
10^4
10^5
10^6
Hz

FIG. 4

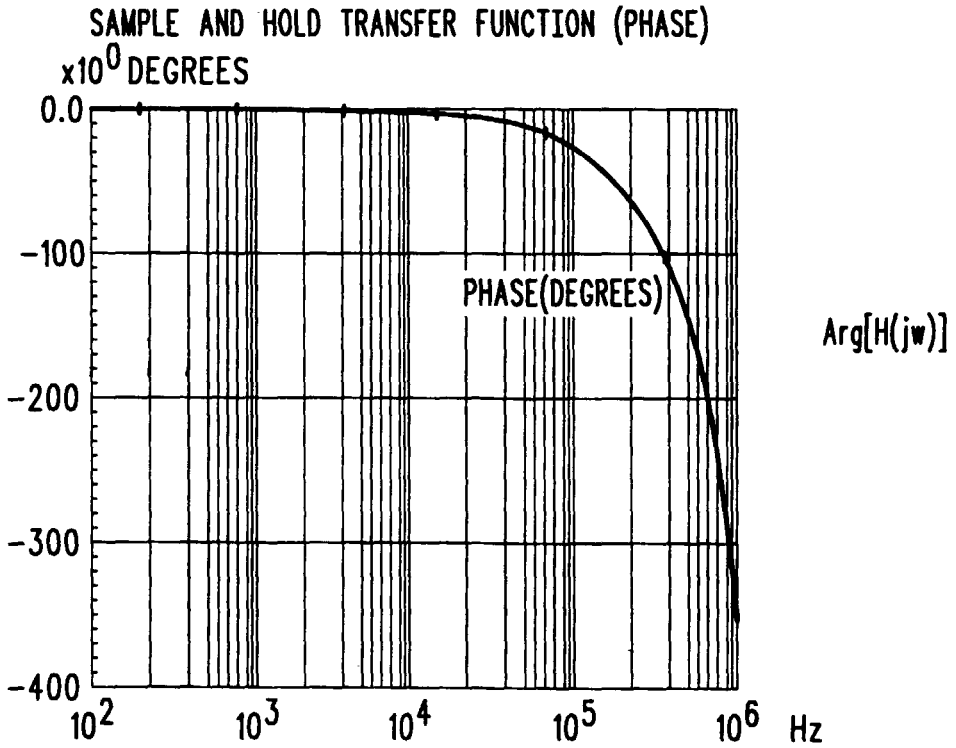
SAMPLE AND HOLD TRANSFER FUNCTION (PHASE)
x10^0 DEGREES
0.0
-100
-200
-300
-400
PHASE(DEGREES)
Arg[H(jw)]
10^2
10^3
10^4
10^5
10^6
Hz

FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 40 2065

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 547 916 A (TEXAS INSTRUMENTS INC ;TEXAS INSTRUMENTS LTD (GB)) 23 June 1993	1,2,5,6, 8	G05F1/575
A	* the whole document *	3,4,6,7	
A	US 5 686 820 A (RIGGIO JR SALVATORE RICHARD) 11 November 1997 * the whole document *	1-8	
A	US 4 728 811 A (IIDA TETSUYA ET AL) 1 March 1988 * the whole document *	2,6	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13 January 1999	Schobert, D

CATEGORY OF CITED DOCUMENTS

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13-01-1999

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