



(19)

Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 991 088 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
05.04.2000 Bulletin 2000/14

(51) Int. Cl.⁷: H01F 17/00, H01F 27/36

(21) Application number: 99119524.9

(22) Date of filing: 01.10.1999

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE**
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 02.10.1998 KR 9841680

(71) Applicants:
• Korea Electronics Technology Institute
Pyungtaek-Si, Kyunggi-Do (KR)
• Pilkor Electronics Ltd.
SUWON-SI, KYUNGGI-DO (KR)

(72) Inventors:
• Kang, Nam Kee
Seocho-Ku, Seoul (KR)
• Park, In Shig
Kiheung-eub, Yongin-Si, Kyunggi-Do (KR)

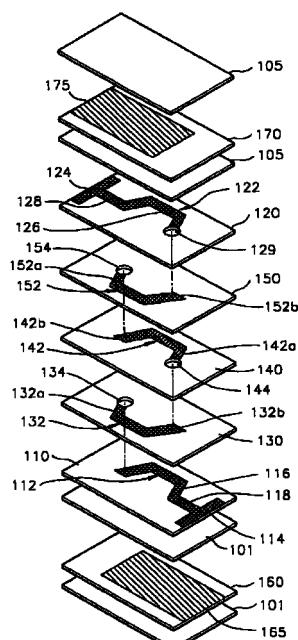
- Lim, Wook
Pyungtaek-Si, Kyunggi-Do (KR)
- Yoo, Chan Sei
1-Ga, Jung-Ku, Seoul (KR)
- Kim, Jong Dae
Kyunggi-Do (KR)
- Ko, Hyun Jong
Sungnam-Si, Kyunggi-Do (KR)
- Kim, Sang Cheol
Kyunggi-Do (KR)

(74) Representative:
von Samson-Himmelstjerna, Friedrich R., Dipl.-
Phys.
SAMSON & PARTNER
Widenmayerstrasse 5
80538 München (DE)

(54) Multilayer type chip inductor

(57) A multilayer type chip inductor having a pair of outermost sheets and a plurality of intermediate sheets stacked between the outermost sheets, includes a pair of shielding sheets each of which has a shielding pattern for preventing electromagnetic waves generated thereby from being emitted.

FIG.2



DescriptionField of the Invention

[0001] The present invention relates to a chip inductor; and, more particularly, to a multilayer type chip inductor capable of preventing electromagnetic waves generated thereby from being emitted.

Background of the Invention

[0002] In general, a multilayer type chip inductor is comprised of a stack of the sheets made of a ferrite or a dielectric material, having respective coil patterned conductors formed thereon, and connected electrically by the through holes in series with each other in a substantially zigzag fashion. Such a multilayer type chip inductor is used, for example, for suppressing noise or making a LC resonance circuit.

[0003] There is shown in Fig. 1 an exploded view of the conventional multilayer type chip inductor.

[0004] As shown, the conventional multilayer type chip inductor includes a pair of first cover plates 1, a pair of second cover plates 5, a first and a second outermost sheets 10, 20 having a generally rectangular shape, and a first, a second, a third intermediate sheets 30, 40, 50 stacked one above the other and interposed between the outermost sheets 10, 20. The cover plates and the sheets 1, 5, 10, 20, 30, 40, 50 are made of the ferrite or the dielectric material.

[0005] The first outermost sheet 10 is formed with a first electric terminal pattern 12. The electric terminal pattern 12 has a lateral strip portion 14 extending along a shorter side of the first outermost sheet 10 for electric connection with an end cap or like terminal member (not shown), a coiled portion 16 at a general central portion of the first outermost sheet 10, and a connecting portion 18 for connecting the lateral strip portion 14 with the coiled portion 16.

[0006] Similar to the first outermost sheet 10, the second outermost sheet 20 is formed with a second electric terminal pattern 22 having a lateral strip portion 24, a coiled portion 26 and a connecting portion 28. However, dissimilar to the first outermost sheet 10, the second outermost sheet 20 has a first through hole 29 at a free end of the coiled portion 26 thereof. The first through hole 29 is formed by perforating the second outermost sheet 20 and filled with a conductive material for establishing an electrical connection with neighboring pattern, as will be described later.

[0007] The first, the second, the third intermediate sheets 30, 40, 50 are, respectively, formed with a first, a second, a third coiled electric conductor patterns 32, 42, 52. The first conductor pattern 32 has a perforated ends 32a and a non-perforated end 32b. Similarly, the second and the third conductor patterns 42, 52 have a perforated and a non-perforated ends 42a, 42b and a perforated and a non-perforated ends 52a, 52b, respectively.

The perforated ends 32a, 42a, 52a are, respectively, formed with a second, a third, a fourth via holes 34, 44, 54. Each of the via holes 34, 44, 54 is formed by perforating the respective intermediate sheets 30, 40, 50 and filled with a conductive material for establishing an electrical connection with neighboring patterns, as will be described later.

[0008] When the above-mentioned sheets 1, 5, 10, 20, 30, 40, 50 are assembled together, the first outermost sheet 10 is positioned in a lowermost location.

[0009] The first intermediate sheet 30 is disposed above the first outermost sheet 10 in such a way that the perforated end 32a thereof is aligned with a free end of the first electric terminal pattern 12 of the first outermost sheet 10 and the first coiled electric conductor pattern 32 thereof is electrically connected with the first electric terminal pattern 12 of the first outermost sheet 10 through the second via hole 34 thereof.

[0010] Next, the second intermediate sheet 40 is installed above the first intermediate sheet 30 in such a way that the perforated end 42a and the non-perforated ends 42b thereof are, respectively, aligned with the non-perforated end 32b and perforated end 32a of the first intermediate sheet 30 and the second electric conductor pattern 42 thereof is electrically connected with the first electric conductor pattern 32 of the first intermediate sheet 30 through the third via hole 44 thereof.

[0011] Similarly, the third intermediate sheet 50 is installed above the second intermediate sheet 40 in such a way that the perforated end 52a and the non-perforated ends 52b thereof are, respectively, aligned with the non-perforated end 42b and perforated end 42a of the second intermediate sheet 40 and the third electric conductor pattern 52 thereof is electrically connected with the second electric conductor pattern 42 of the second intermediate sheet 40 through the fourth via hole 54 thereof.

[0012] Subsequently, the second outermost sheet 20 is disposed on the third intermediate sheet 50 in such a way that the free end of the second electric terminal pattern 22 thereof is aligned with the non-perforated end 52b of the third electric conductor pattern 52 of the third intermediate sheet 50 and the second electric terminal pattern 22 thereof is electrically connected with the third coiled electric conductor pattern 52 of the third intermediate sheet 50 through the first via hole 29 thereof through via holes 29, 34, 44, 54.

[0013] The forgoing arrangement allows the sheets 10, 20, 30, 40, 50 to be electrically connected with each other.

[0014] Finally, in order to protect the assembled multilayer chip inductor from the external influences, the first and the second cover plates 1, 5 are, respectively, installed below the first outermost sheet 10 and above the second outermost sheet 20.

[0015] In such a multilayer type chip conductor, when radio frequency signals are applied to the chip inductor through the terminal patterns, electromagnetic waves

are generated thereby and emitted therefrom, detrimentally affecting components adjacent thereto.

Summary of the Invention

[0016] It is, therefore, a primary object of the present invention to provide a multilayer type chip inductor equipped with a pair of sheets for preventing electromagnetic waves generated thereby from being emitted.

[0017] In accordance with one aspect of the present invention, there is provided a multilayer type chip inductor having a pair of outermost sheets and a plurality of intermediate sheets stacked between the outermost sheets, the inductor comprising a pair of shielding sheets each of which has a shielding pattern for shielding electromagnetic waves.

Brief Description of the Drawings

[0018] The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, wherein:

Fig. 1 shows an exploded perspective view of the conventional multilayer type chip inductor;

Fig. 2 illustrates an exploded perspective view of the multilayer type chip inductor in accordance with a first preferred embodiment of the present invention;

Fig. 3 describes an exploded perspective view of the multilayer type chip inductor in accordance with a second preferred embodiment of the present invention; and

Fig. 4 discloses an exploded perspective view of the multilayer type chip inductor in accordance with a third preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0019] An inventive multilayer type chip inductor in accordance with the present invention will be described using Figs. 2 to 4. It should be noted that like parts appearing in Figs. 2 to 4 are represented by like reference numerals.

[0020] Referring to Fig. 2, a first preferred embodiment of the present invention includes a pair of first cover plates 101, a pair of second cover plates 105, a first and a second shielding sheets 160, 170, a first and a second outermost sheets 110, 120 having a generally rectangular shape, and a first, a second, a third intermediate sheets 130, 140, 150 stacked one above the other and interposed between the outermost sheets 110, 120. The cover plates and the sheets 101, 105, 110, 120, 130, 140, 150, 160, 170 are made of a ferrite or a dielectric material.

[0021] The first outermost sheet 110 is formed with a first electric terminal pattern 112. The electric terminal pattern 112 has a lateral strip portion 114 extending along a shorter side of the first outermost sheet 110 for electric connection with an end cap or like terminal member (not shown), a coiled portion 116 at a general central portion of the first outermost sheet 110, and a connecting portion 118 for connecting the lateral strip portion 114 with the coiled portion 116.

[0022] Similar to the first outermost sheet 110, the second outermost sheet 120 is formed with a second electric terminal pattern 122 having a lateral strip portion 124, a coiled portion 126 and a connecting portion 128. However, dissimilar to the first outermost sheet 110, the second outermost sheet 120 has a first through hole 129 at a free end of the coiled portion 126 thereof. The first through hole 129 is formed by perforating the second outermost sheet 120 and filled with a conductive material for establishing an electrical connection with neighboring pattern, as will be described later.

[0023] The first, the second, the third intermediate sheets 130, 140, 150 are, respectively, formed with a first, a second, a third coiled electric conductor patterns 132, 142, 152. The first conductor pattern 132 has a perforated ends 132a and a non-perforated end 132b. Similarly, the second and the third conductor patterns 142, 152 have a perforated and a non-perforated ends 142a, 142b and a perforated and a non-perforated ends 152a, 152b, respectively. The perforated ends 132a, 142a, 152a are, respectively, formed with a second, a third, a fourth via holes 134, 144, 154. Each of the via holes 134, 144, 154 is formed by perforating the respective intermediate sheets 130, 140, 150 and filled with a conductive material for establishing an electrical connection with neighboring patterns, as will be described later.

[0024] The first and the second shielding sheets 160, 170 for shielding electromagnetic waves caused by the inductor are, respectively, formed with a first and a second shielding patterns 165, 175. Each of the shielding patterns 165, 175 has, for example, a rectangular shape. To be more specific, each of the shielding patterns 165, 175 extends from a shorter side of each of the shielding sheet 160, 170 toward an opposite shorter side thereof. Furthermore, the first and the second shielding sheets 160, 170 are, respectively, interposed between the first cover plates 101 and between the second cover plates 105 so as to prevent electromagnetic waves generated by the inductor from being emitted.

[0025] When the above-mentioned sheets 101, 105, 110, 120, 130, 140, 150 are assembled together, the first outermost sheet 110 is positioned immediately above the first cover plates 101.

[0026] The first intermediate sheet 130 is disposed above the first outermost sheet 110 in such a way that the perforated end 132a thereof is aligned with a free end of the first electric terminal pattern 112 of the first outermost sheet 110 and the first coiled electric conduc-

tor pattern 132 thereof is electrically connected with the first electric terminal pattern 112 of the first outermost sheet 110 through the second via hole 134 thereof.

[0027] Next, the second intermediate sheet 140 is installed above the first intermediate sheet 130 in such a way that the perforated end 142a and the non-perforated ends 142b thereof are, respectively, aligned with the non-perforated end 132b and perforated end 132a of the first intermediate sheet 130 and the second electric conductor pattern 142 thereof is electrically connected with the first electric conductor pattern 132 of the first intermediate sheet 130 through the third via hole 144 thereof.

[0028] Similarly, the third intermediate sheet 150 is installed above the second intermediate sheet 140 in such a way that the perforated end 152a and 152b thereof are, respectively, aligned with the non-perforated end 142b and perforated end 142a of the second intermediate sheet 140 and the third electric conductor pattern 152 thereof is electrically connected with the second electric conductor pattern 142 of the second intermediate sheet 140 through the fourth via hole 154 thereof.

[0029] Subsequently, the second outermost sheet 120 is disposed on the third intermediate sheet 150 in such a way that the free end of the second electric terminal pattern 122 thereof is aligned with the non-perforated end 152b of the third electric conductor pattern 152 of the third intermediate sheet 150 and the second electric terminal pattern 122 thereof is electrically connected with the third coiled electric conductor pattern 152 of the third intermediate sheet 50 through the first via hole 129 thereof.

[0030] The forgoing arrangement allows the sheets 110, 120, 130, 140, 150 to be electrically connected with each other through via holes 129, 134, 144, 154.

[0031] On the other hand, the first cover plates 101 between which the first shielding sheet 160 is interposed and the second cover plates 105 between which the second shielding sheet 170 is interposed are, respectively, installed below the first outermost sheet 110 and above the second outermost sheet 120. In this case, the second shielding sheet 170 is positioned in such a way that, when the second shielding sheet 170 is turned 180° on an imaginary plane parallel thereto, the second shielding pattern 175 thereof is aligned with the first shielding pattern 165 of the first shielding sheet 160. This protects the inductor from the external influences, preventing electromagnetic waves generated thereby from being emitted.

[0032] An inventive multilayer chip inductor in accordance with a second preferred embodiment of the present invention will now be described with reference to Fig. 3.

[0033] This embodiment is similar to the first one, except that a pair of shielding patterns 265, 275 are positioned at a central portion of each of the shielding sheets 160, 170. To be more specific, the shielding pat-

terns 265, 275 are not contacted with the sides of the shielding sheets 160, 170.

[0034] An inventive multilayer chip inductor in accordance with a third preferred embodiment of the present invention will now be described with reference to Fig. 4.

[0035] This embodiment is similar to the first one, except that a pair of shielding patterns 365, 375 are, respectively, divided into two portions 365a, 365b and 375a, 375b. One portion 365a of the shielding pattern 365 extends from one shorter side of the shielding sheet 160 and terminates at a generally intermediate portion of a longer side of the shielding sheet 160, and the other portion 365b of the shielding pattern 365 extends from an opposite shorter side of the shielding sheet 160 and terminates at a generally intermediate portion of the longer side of the shielding sheet 160. The portions 375a, 375b have an identical shape as that of the portions 365a, 365b.

[0036] In such a multilayer type chip inductor, by providing inductor with the shielding sheets, it is possible to prevent electromagnetic waves generated thereby from being emitted.

[0037] While the present invention has been described with respect to certain preferred embodiments only, other modifications and variations may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A multilayer type chip inductor having a pair of outermost sheets and a plurality of intermediate sheets stacked between the outermost sheets, the multilayer type chip inductor comprising:
35 a pair of shielding sheets each of which has a shielding pattern for shielding electromagnetic waves.
2. The multilayer type chip inductor of claim 1, further comprising a pair of first cover plates installed on one outermost sheets and a pair of second cover plates disposed on the other outermost sheets, for protecting the inductor from external influences.
- 40 3. The multilayer type chip inductor of claim 2, wherein the shielding sheets are, respectively, interposed between the first cover plates and the second cover plates.
- 45 5. The multilayer type chip inductor of claim 3, wherein the shielding sheets are disposed in such a way that, when one shielding sheet is turned 180° on an imaginary plane parallel thereto, the shielding pattern thereof is aligned with the shielding pattern of the other shielding sheet.
- 50 6. The multilayer type chip inductor of claim 1, wherein

each of the shielding sheets has a rectangular shape, and each of the shielding patterns extends from a shorter side of each of the shielding sheets toward an opposite shorter side thereof.

5

6. The multilayer type chip inductor of claim 1, wherein each of the shielding patterns is positioned at a central portion of each of the shielding sheets in such a way that it is not contact with the sides of the shielding sheets. 10
7. The multilayer type chip inductor of claim 1, wherein each of the shielding patterns is divided into two portions, one portion of the shielding pattern extending from one shorter side of the shielding sheet and terminates at a generally intermediate portion of a longer side of the shielding sheet, and the other portion of the shielding pattern extending from another shorter side of the shielding sheet and terminates at a generally intermediate portion of 15 20 the longer side of the shielding sheet.

25

30

35

40

45

50

55

FIG. 1
(*PRIOR ART*)

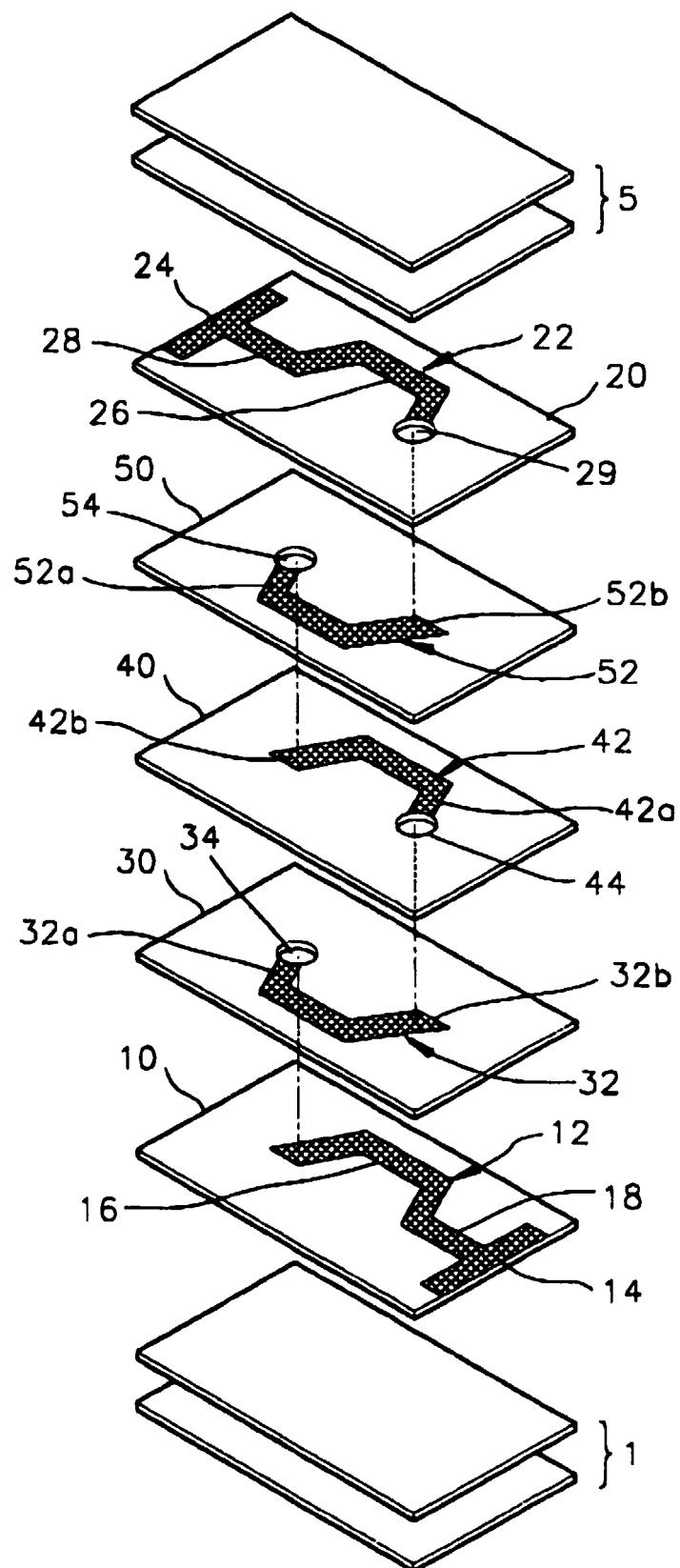


FIG.2

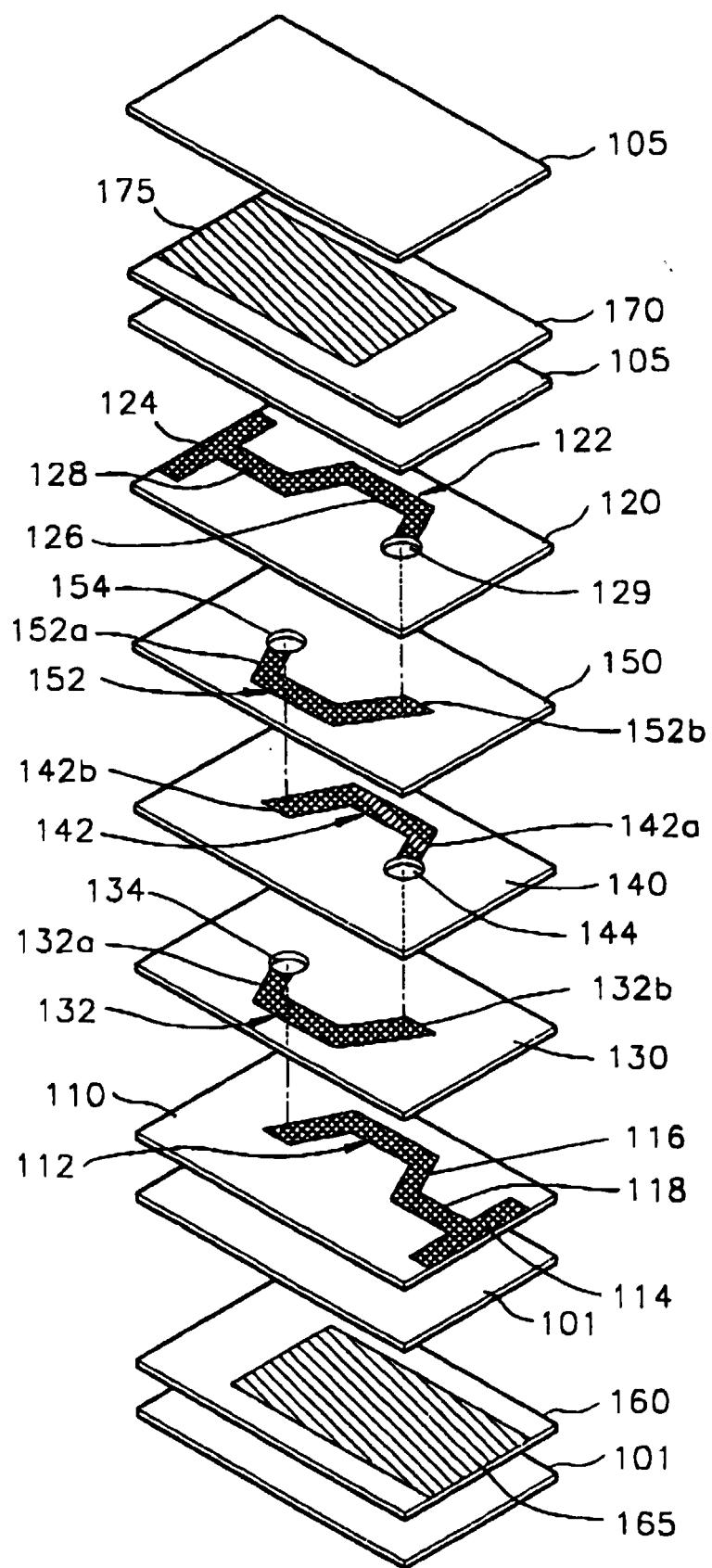


FIG. 3

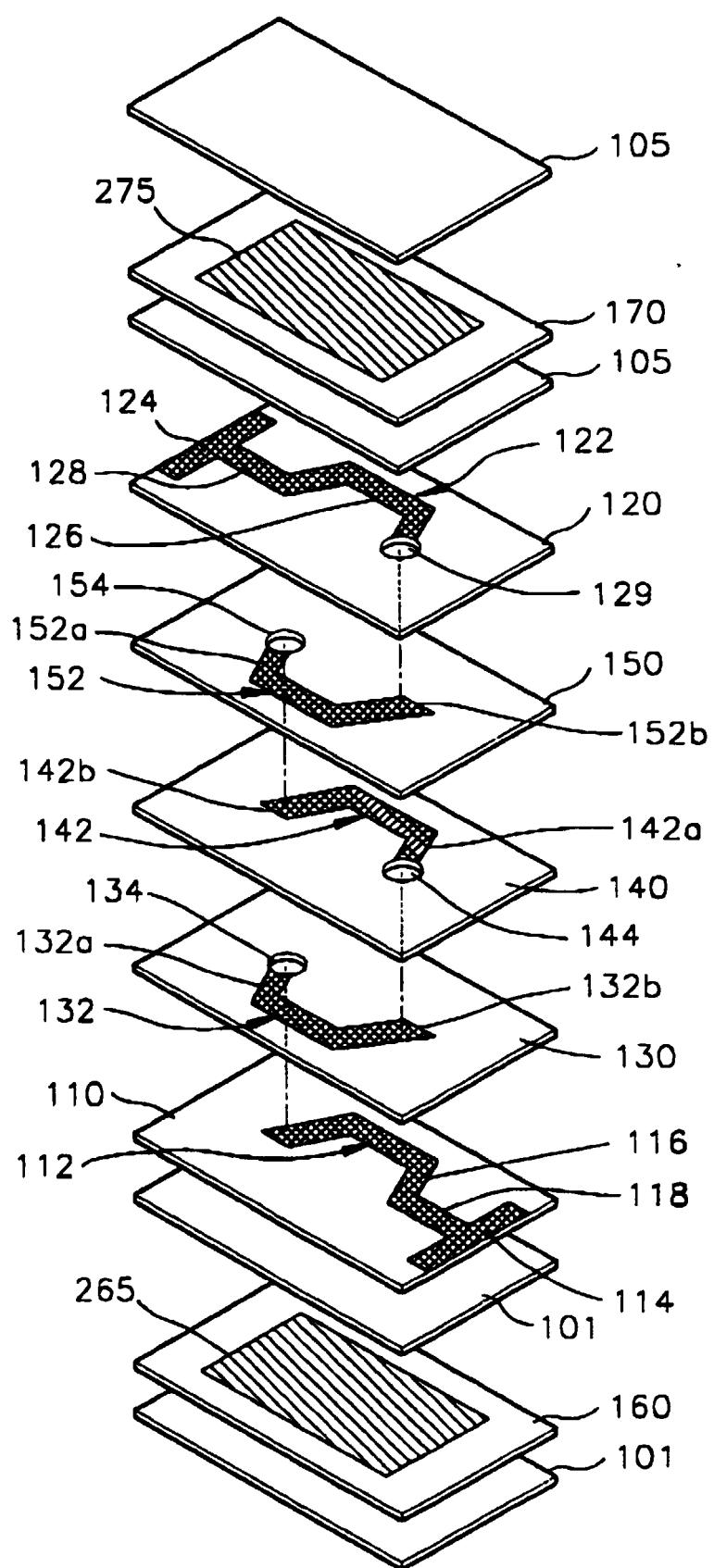
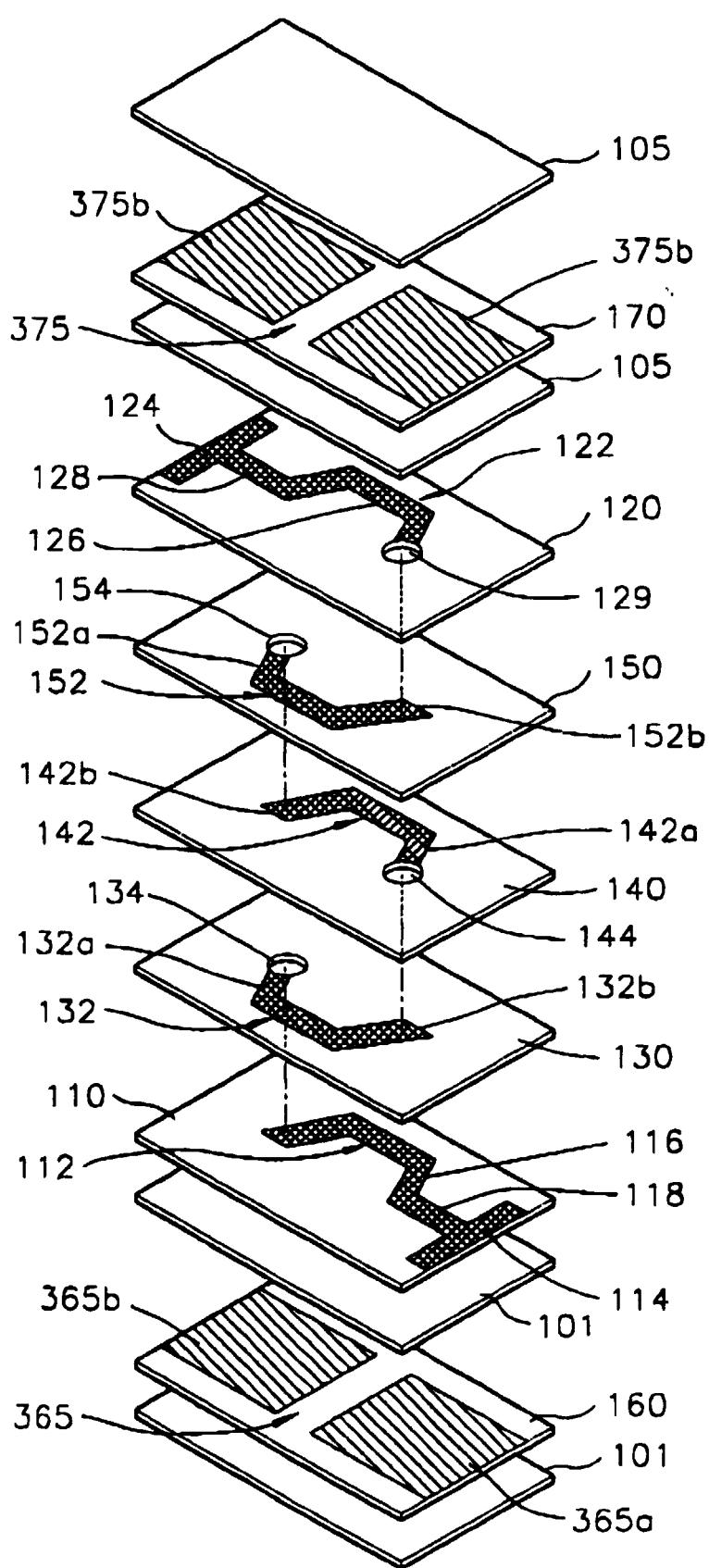


FIG.4





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 11 9524

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	US 4 916 582 A (OKAMURA HISATAKE ET AL) 10 April 1990 (1990-04-10) * column 4, line 1 - line 28 * * column 5, line 24 - line 50; figures 5-9B * ---	1-3,6,7	H01F17/00 H01F27/36
A	US 5 250 923 A (OSHIMA HISATO ET AL) 5 October 1993 (1993-10-05) * column 3, line 15 - column 5, line 14; figures 2-4 * ---	1,2,5	
A	US 5 392 019 A (OHKUBO AKIRA) 21 February 1995 (1995-02-21) * abstract * -----	4	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			H01F
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	31 January 2000	Marti Almeda, R	
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone	T : theory or principle underlying the invention		
Y : particularly relevant if combined with another document of the same category	E : earlier patent document, but published on, or after the filing date		
A : technological background	D : document cited in the application		
O : non-written disclosure	L : document cited for other reasons		
P : intermediate document	& : member of the same patent family, corresponding document		

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 11 9524

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

31-01-2000

Patent document cited in search report	Publication date		Patent family member(s)	Publication date
US 4916582 A	10-04-1990	JP	1960976 C	10-08-1995
		JP	2007405 A	11-01-1990
		JP	6090978 B	14-11-1994
US 5250923 A	05-10-1993	JP	5190363 A	30-07-1993
US 5392019 A	21-02-1995	JP	5152132 A	18-06-1993