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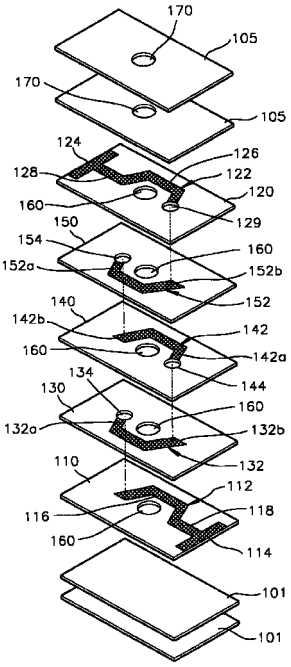
(54) Multilayer type chip inductor

(57) A multilayer type chip inductor includes a pair of outermost sheets each of which has a terminal pattern and a first via hole for an electrical connection with neighboring patterns and a plurality of intermediate sheets each of which has a conductor pattern, a second via hole for an electrical connection with neighboring patterns, and a first through hole for reducing a dielectric constant of the inductor. The intermediate sheets are stacked between the outermost sheets in such a way that the conductor patterns thereof are electrically connected with each other and simultaneously are electrically connected with the terminal patterns of the outermost sheets through the first and the second via holes.

FIG.3



EP 1 011 115 A1

Description

Field of the Invention

[0001] The present invention relates to a chip inductor; and, more particularly, to a multilayer type chip inductor having improved operating characteristics.

Background of the Invention

[0002] In general, a multilayer type chip inductor is comprised of a stack of the sheets made of a ferrite or a dielectric material, having respective coil patterned conductors formed thereon, and connected electrically by the via holes in series with each other in a substantially zigzag fashion. Such a multilayer type chip inductor is used, for example, for suppressing noise or making a LC resonance circuit.

[0003] There is shown in Fig. 1 an exploded view of the conventional multilayer type chip inductor.

[0004] As shown, the conventional multilayer type chip inductor includes a pair of first cover plates 1, a pair of second cover plates 5, a first and a second outermost sheets 10, 20 having a generally rectangular shape, and a first, a second, a third intermediate sheets 30, 40, 50 stacked one above the other and interposed between the outermost sheets 10, 20. The cover plates and the sheets 1, 5, 10, 20, 30, 40, 50 are made of the ferrite or the dielectric material.

[0005] The first outermost sheet 10 is formed with a first electric terminal pattern 12. The electric terminal pattern 12 has a lateral strip portion 14 extending along a shorter side of the first outermost sheet 10 for electric connection with an end cap or like terminal member (not shown), a coiled portion 16 at a general central portion of the first outermost sheet 10, and a connecting portion 18 for connecting the lateral strip portion 14 with the coiled portion 16.

[0006] Similar to the first outermost sheet 10, the second outermost sheet 20 is formed with a second electric terminal pattern 22 having a lateral strip portion 24, a coiled portion 26 and a connecting portion 28. However, dissimilar to the first outermost sheet 10, the second outermost sheet 20 has a first via hole 29 at a free end of the coiled portion 26 thereof. The first via hole 29 is formed by perforating the second outermost sheet 20 and filled with a conductive material for establishing an electrical connection with neighboring pattern, as will be described later.

[0007] The first, the second, the third intermediate sheets 30, 40, 50 are, respectively, formed with a first, a second, a third coiled electric conductor patterns 32, 42, 52. The first conductor pattern 32 has a perforated ends 32a and a non-perforated end 32b. Similarly, the second and the third conductor patterns 42, 52 have a perforated and a non-perforated ends 42a, 42b and a perforated and a non-perforated ends 52a, 52b, respectively. The perforated ends 32a, 42a, 52a are, respectively, formed with a second, a third, a fourth via holes 34, 44, 54. Each of the via holes 34, 44, 54 is formed by perforating the respective intermediate sheets 30, 40, 50 and filled with a conductive material for establishing an electrical connection with neighboring patterns, as will be described later.

[0008] When the above-mentioned sheets 1, 5, 10, 20, 30, 40, 50 are assembled together, the first outermost sheet 10 is positioned in a lowermost location.

[0009] The first intermediate sheet 30 is disposed above the first outermost sheet 10 in such a way that the perforated end 32a thereof is aligned with a free end of the first electric terminal pattern 12 of the first outermost sheet 10 and the first coiled electric conductor pattern 32 thereof is electrically connected with the first electric terminal pattern 12 of the first outermost sheet 10 through the second via hole 34 thereof.

[0010] Next, the second intermediate sheet 40 is installed above the first intermediate sheet 30 in such a way that the perforated end 42a and the non-perforated ends 42b thereof are, respectively, aligned with the non-perforated end 32b and perforated end 32a of the first intermediate sheet 30 and the second electric conductor pattern 42 thereof is electrically connected with the first electric conductor pattern 32 of the first intermediate sheet 30 through the third via hole 44 thereof.

[0011] Similarly, the third intermediate sheet 50 is installed above the second intermediate sheet 40 in such a way that the perforated end 52a and the non-perforated ends 52b thereof are, respectively, aligned with the non-perforated end 42b and perforated end 42a of the second intermediate sheet 40 and the third electric conductor pattern 52 thereof is electrically connected with the second electric conductor pattern 42 of the second intermediate sheet 40 through the fourth via hole 54 thereof.

[0012] Subsequently, the second outermost sheet 20 is disposed on the third intermediate sheet 50 in such a way that the free end of the second electric terminal pattern 22 thereof is aligned with the non-perforated end 52b of the third electric conductor pattern 52 of the third intermediate sheet 50 and the second electric terminal pattern 22 thereof is electrically connected with the third coiled electric conductor pattern 52 of the third intermediate sheet 50 through the first via hole 29 thereof.

[0013] The forgoing arrangement allows the sheets 10, 20, 30, 40, 50 to be electrically connected with each other.

[0014] Finally, in order to protect the assembled multilayer chip inductor from the external influences, the first and the second cover plates 1, 5 are, respectively, installed below the first outermost sheet 10 and above the second outermost sheet 20.

[0015] However, there are a number of major shortcomings associated with the above described chip inductor: for instance, at a relatively high frequency, e.g., order of 3GHz, it becomes impossible for it to func-

tion as an inductor.

Summary of the Invention

[0016] It is, therefore, a primary object of the present invention to provide a multilayer type chip inductor capable of operating at a relatively high frequency.

[0017] In accordance with one aspect of the present invention, there is provided a multilayer type chip inductor comprising: a pair of outermost sheets each of which has a terminal pattern and a first via hole for an electrical connection with neighboring patterns and a plurality of intermediate sheets each of which has a conductor pattern, a second via hole for an electrical connection with neighboring patterns, and a first through hole for reducing a dielectric constant of the inductor, the intermediate sheets being stacked between the outermost sheets in such a way that the conductor patterns thereof are electrically connected with each other and simultaneously are electrically connected with the terminal patterns of the outermost sheets through the first and the second via holes.

Brief Description of the Drawings

[0018] The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, wherein:

Fig. 1 shows an exploded perspective view of the conventional multilayer type chip inductor;
Fig. 2 illustrates an exploded perspective view of the multilayer type chip inductor in accordance with a first preferred embodiment of the present invention;
Fig. 3 describes an exploded perspective view of the multilayer type chip inductor in accordance with a second preferred embodiment of the present invention;
Fig. 4 discloses an exploded perspective view of the multilayer type chip inductor in accordance with a third preferred embodiment of the present invention; and
Fig. 5 displays an exploded perspective view of the multilayer type chip inductor in accordance with a fourth preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0019] A multilayer type chip inductor in accordance with the present invention will be described using Figs. 2 to 5. It should be noted that like parts appearing in Figs. 2 to 5 are represented by like reference numerals.

[0020] Referring to Fig. 2, a first preferred embodiment of the present invention includes a pair of first cover plates 101, a pair of second cover plates 105, a first and a second outermost sheets 110, 120 having a generally rectangular shape, and a first, a second, a third intermediate sheets 130, 140, 150 stacked one above the other and interposed between the outermost sheets 110, 120. The cover plates and the sheets 101, 105, 110, 120, 130, 140, 150 are made of a ferrite or a dielectric material.

[0021] The first outermost sheet 110 is formed with a first electric terminal pattern 112. The electric terminal pattern 112 has a lateral strip portion 114 extending along a shorter side of the first outermost sheet 110 for electric connection with an end cap or like terminal member (not shown), a coiled portion 116 at a general central portion of the first outermost sheet 110, and a connecting portion 118 for connecting the lateral strip portion 114 with the coiled portion 116.

[0022] Similar to the first outermost sheet 110, the second outermost sheet 120 is formed with a second electric terminal pattern 122 having a lateral strip portion 124, a coiled portion 126 and a connecting portion 128. However, in contrast to the first outermost sheet 110, the second outermost sheet 120 has a first via hole 129 at a free end of the coiled portion 126 thereof. The first via hole 129 is formed by perforating the second outermost sheet 120 and filled with a conductive material for establishing an electrical connection with neighboring patterns, as will be described later.

[0023] The first, the second, the third intermediate sheets 130, 140, 150 are, respectively, formed with a first, a second, a third coiled electric conductor patterns 132, 142, 152. The first conductor pattern 132 has a perforated ends 132a and a non-perforated end 132b. Similarly, the second and the third conductor patterns 142, 152 have a perforated and a non-perforated ends 142a, 142b and a perforated and a non-perforated ends 152a, 152b, respectively. The perforated ends 132a, 142a, 152a are, respectively, formed with a second, a third, a fourth via holes 134, 144, 154. Each of the via holes 134, 144, 154 is formed by perforating the respective intermediate sheets 130, 140, 150 and filled with a conductive material for establishing an electrical connection with neighboring patterns, as will be described later.

[0024] The sheets 110, 120, 130, 140, 150 described above are, respectively, provided with a first through hole 160 at their substantially central portion in such a way that the first through holes 160 are coaxially aligned.

[0025] When the above-mentioned sheets 101, 105, 110, 120, 130, 140, 150 are assembled together, the first outermost sheet 110 is positioned immediately above the first cover plates 101.

[0026] The first intermediate sheet 130 is disposed above the first outermost sheet 110 in such a way that the perforated end 132a thereof is aligned with a free end of the first electric terminal pattern 112 of the first outermost sheet 110 and the first coiled electric conduc-

tor pattern 132 thereof is electrically connected with the first electric terminal pattern 112 of the first outermost sheet 110 through the second via hole 134 thereof.

[0027] Next, the second intermediate sheet 140 is installed above the first intermediate sheet 130 in such a way that the perforated end 142a and the non-perforated ends 142b thereof are, respectively, aligned with the non-perforated end 132b and perforated end 132a of the first intermediate sheet 130 and the second electric conductor pattern 142 thereof is electrically connected with the first electric conductor pattern 132 of the first intermediate sheet 130 through the third via hole 144 thereof.

[0028] Similarly, the third intermediate sheet 150 is installed above the second intermediate sheet 140 in such a way that the perforated end 152a and the non-perforated end 152b thereof are, respectively, aligned with the non-perforated end 142b and perforated end 142a of the second intermediate sheet 140 and the third electric conductor pattern 152 thereof is electrically connected with the second electric conductor pattern 142 of the second intermediate sheet 140 through the fourth via hole 154 thereof.

[0029] Subsequently, the second outermost sheet 120 is disposed on the third intermediate sheet 150 in such a way that the free end of the second electric terminal pattern 122 thereof is aligned with the non-perforated end 152b of the third electric conductor pattern 152 of the third intermediate sheet 150 and the second electric terminal pattern 122 thereof is electrically connected with the third coiled electric conductor pattern 152 of the third intermediate sheet 150 through the first via hole 129 thereof.

[0030] The forgoing arrangement allows the sheets 110, 120, 130, 140, 150 to be electrically connected with each other through the via holes 129, 134, 144, 154 and the through holes 160 to be coaxially aligned. The coaxial first through holes 160 allow the dielectric constant of the chip inductor to be reduced. To be more specific, the dielectric constant of the ferrite or the dielectric material constituting the sheets is about 4 to 10 but that of air within a space formed by the through holes is about 1. Accordingly, the chip inductor with through holes 160 becomes capable of operating at a relatively high frequency, e.g., order of 3GHz.

[0031] On the other hand, the first cover plates 101 and the second cover plates 105 are, respectively, installed below the first outermost sheet 110 and above the second outermost sheet 120. This protects the inductor from the external influences.

[0032] An inventive multilayer type chip inductor in accordance with a second preferred embodiment of the present invention will now be described with reference to Fig. 3.

[0033] This embodiment is similar to the first one, except that the pair of second cover plates 105 are, respectively, formed with a second through hole 170 so as to be coaxially aligned with the through holes 160.

[0034] An inventive multilayer type chip inductor in accordance with a third preferred embodiment of the present invention will now be described with reference to Fig. 4.

[0035] This embodiment is similar to the second one, except that the pair of first cover plates 101 are, respectively, formed with a third through hole 180 so as to be coaxially aligned with the through holes 160.

[0036] Further, although the above discussions have been presented referring to a situation where the through holes 160, 170, 180 are located at a substantially central portion of its corresponding sheet, they may be positioned at the proper location of the sheets with the only requirement that they are not to be overlapped with its corresponding via holes and the patterns, as shown in Fig. 5.

[0037] Such a multilayer type chip inductor is capable of operating at a relatively high frequency.

[0038] While the present invention has been described with respect to certain preferred embodiments only, other modifications and variations may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A multilayer type chip inductor comprising :

a pair of outermost sheets each of which has a terminal pattern and a first via hole for an electrical connection with neighboring patterns; and

a plurality of intermediate sheets each of which has a conductor pattern, a second via hole for an electrical connection with neighboring patterns, and a first through hole for reducing a dielectric constant of the inductor, the intermediate sheets being stacked between the outermost sheets in such a way that the conductor patterns thereof are electrically connected with each other and simultaneously are electrically connected with the terminal patterns of the outermost sheets through the first and the second via holes.

2. The multilayer type chip inductor of claim 1, further comprising a first cover plate disposed below one of the outermost sheet and a second cover plate disposed above the other outermost sheet, for protecting the inductor from the external influences.

3. The multilayer type chip inductor of claim 2, wherein the first cover plate is formed with a second through hole so as to be coaxially aligned with the first through hole.

4. The multilayer type chip inductor of claim 3, wherein the second cover plate is formed with a third

through hole so as to be coaxially aligned with the first and the second through hole.

FIG. 1
(PRIOR ART)

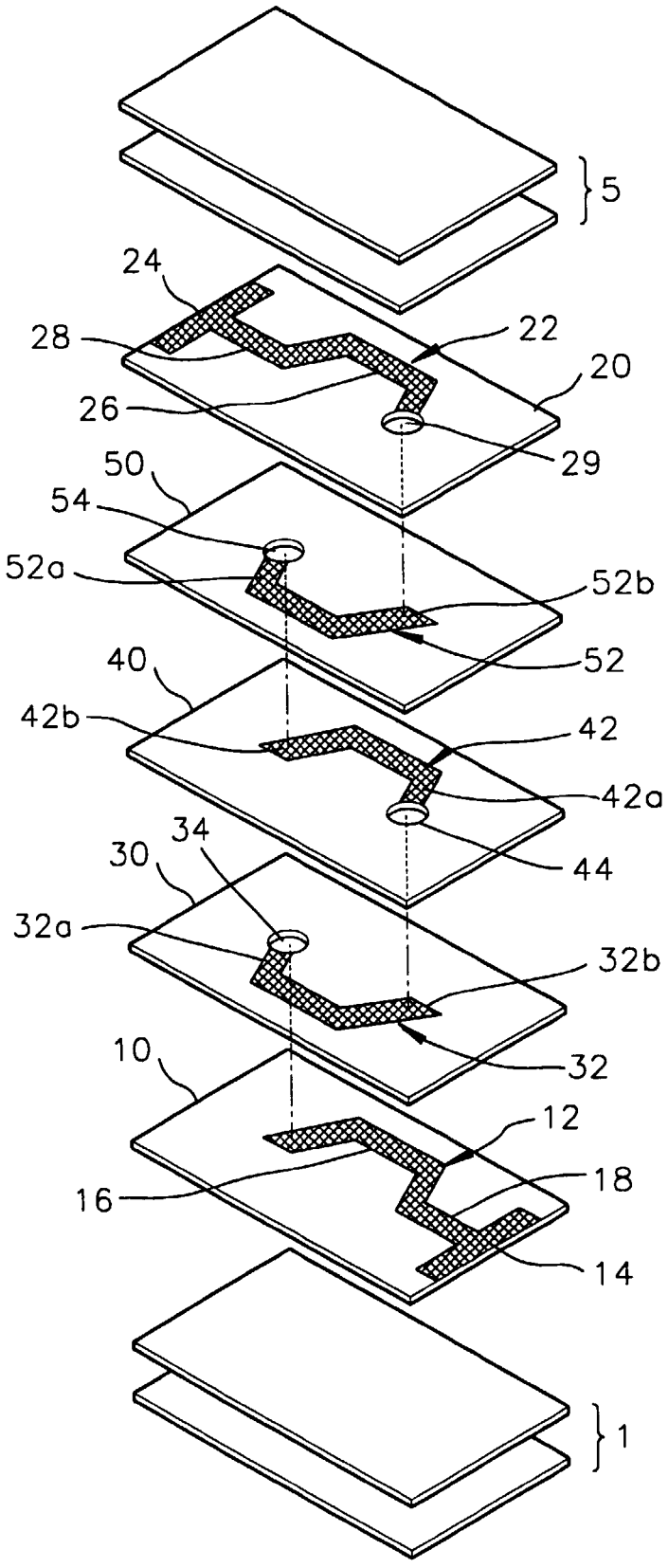


FIG.2

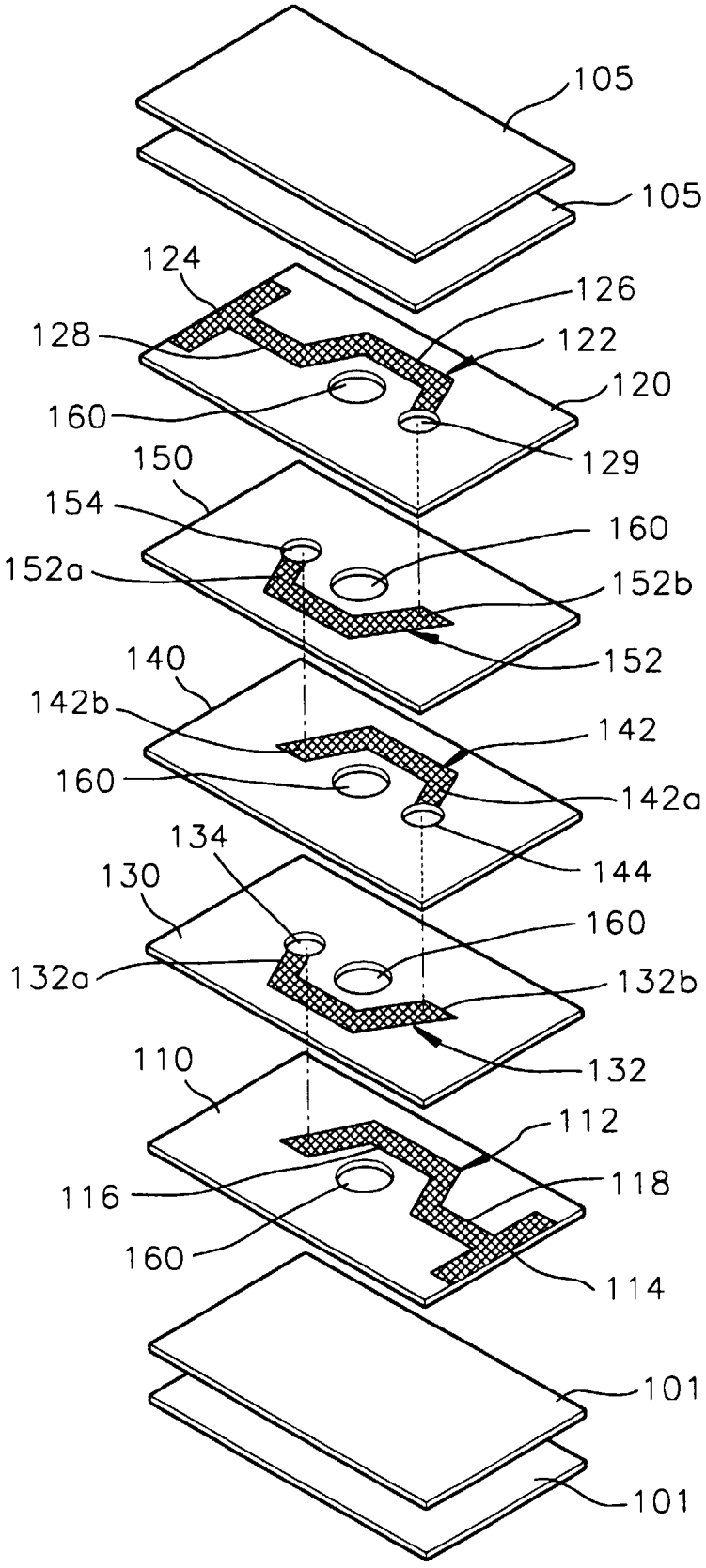

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FIG.3

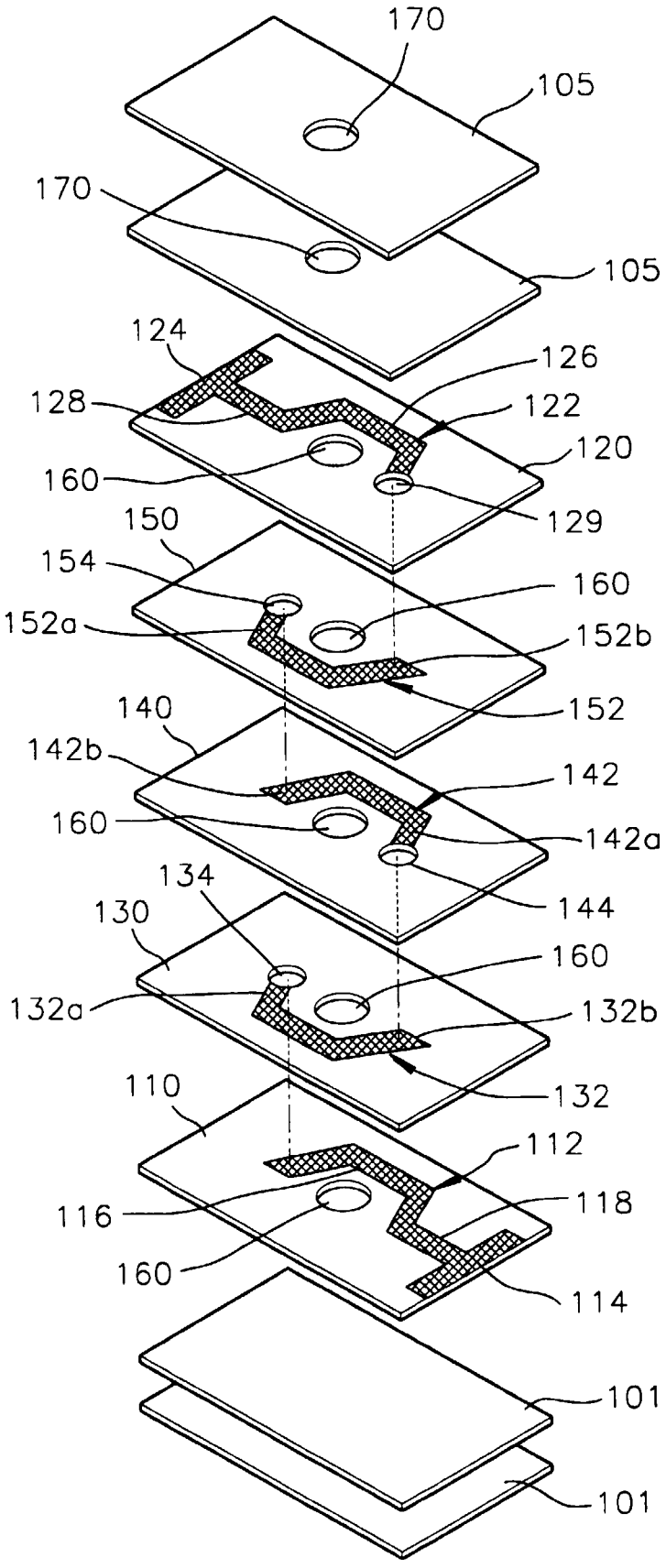
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FIG.4

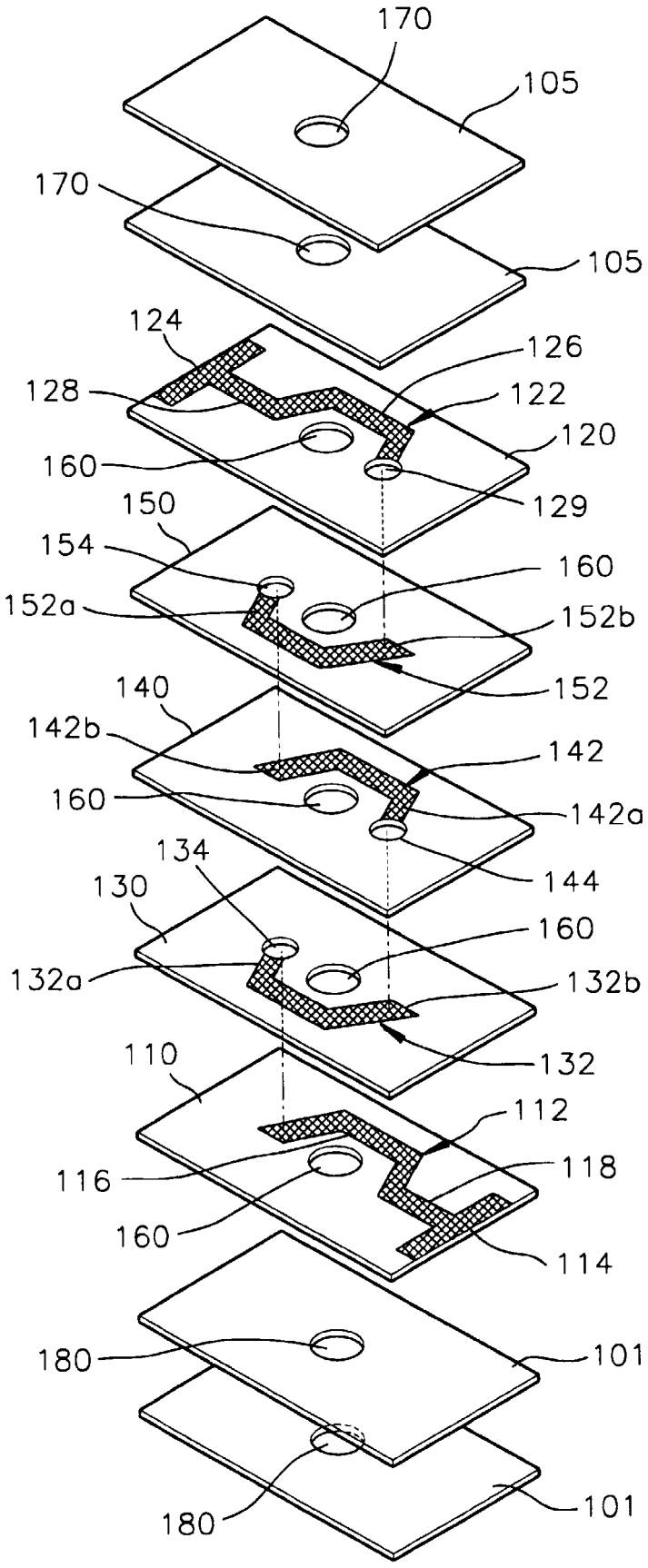
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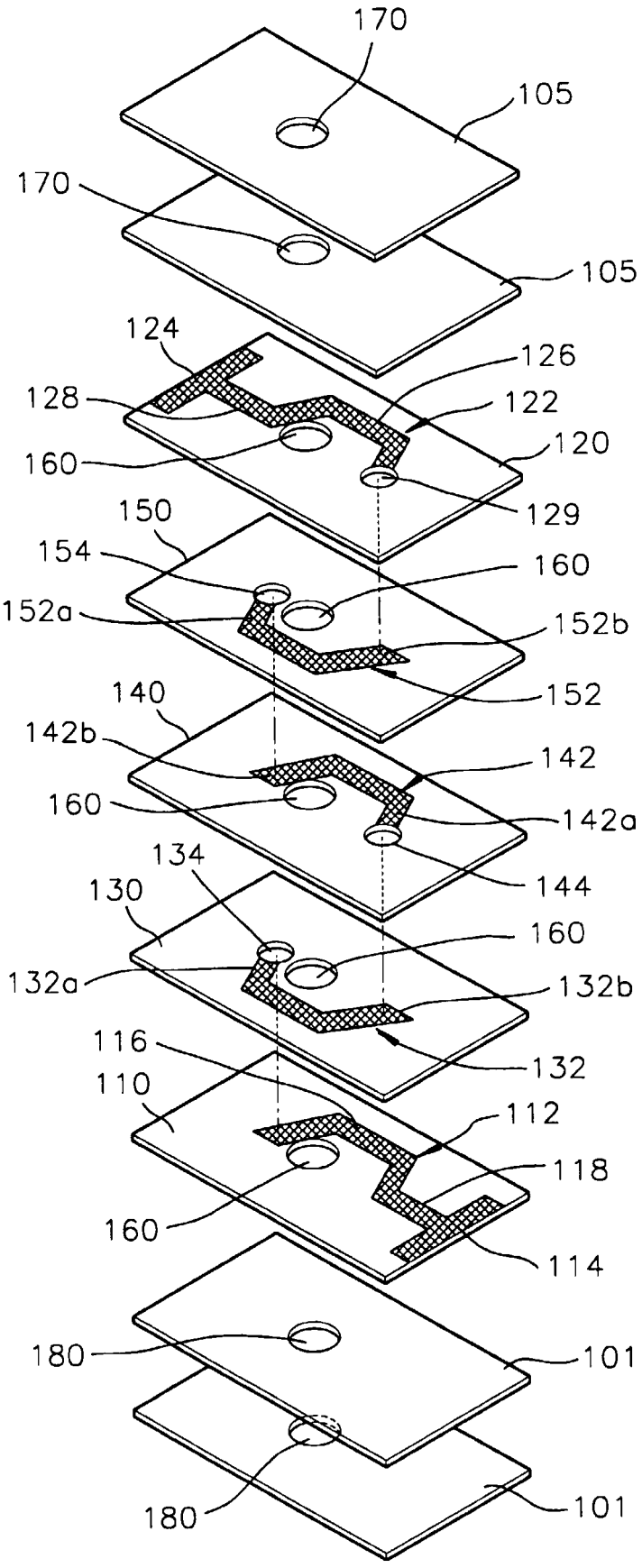
FIG.5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EUROPEAN SEARCH REPORT

Application Number
EP 99 12 1874

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	DE 195 22 043 A (BOSCH GMBH ROBERT) 19 December 1996 (1996-12-19) * column 4, line 4 - line 17; figure 4 *	1	H01F17/00
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 10, 31 October 1996 (1996-10-31) & JP 08 148363 A (MURATA MFG CO LTD), 7 June 1996 (1996-06-07) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 March 2000	Marti Almeda, R

CATEGORY OF CITED DOCUMENTS

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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JP 08148363 A	07-06-1996	NONE	

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