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(72) Inventors:
• **Graham, Alistair**
Powick, Worcestershire WR2 4QR (GB)
• **Hughes, Jonathan Rennie**
St Johns, Worcestershire WR2 4JW (GB)

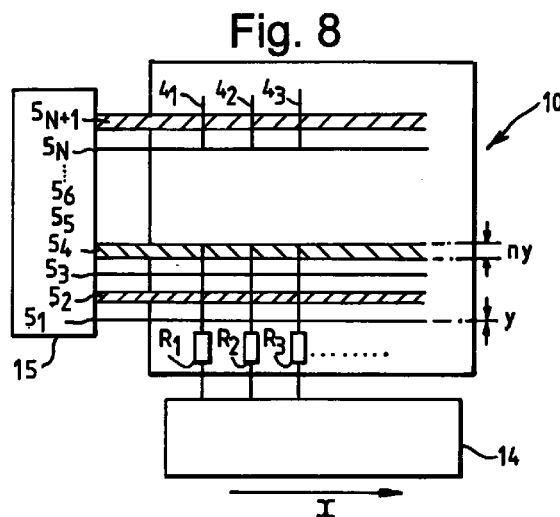
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(74) Representative:
Harding, Richard Patrick et al
Marks & Clerk,
4220 Nash Court,
Oxford Business Park South
Oxford OX4 2RU (GB)

(71) Applicants:
• **SHARP KABUSHIKI KAISHA**
Osaka 545-8522 (JP)
• **THE SECRETARY OF STATE FOR DEFENCE in**
Her Britannic Majesty's Gvmnt. of the United
Kingdom of Great Britain & Northern Ireland
Farnborough, Hampshire GU14 0LX (GB)

(54) **Addressable matrix arrays**

(57) A ferroelectric liquid crystal display panel 10 comprises a layer of ferroelectric liquid crystal material contained between two substrates and bearing first and second electrode structures on their inside surfaces. The first and second electrode structures comprise respectively a series of row and column electrode tracks 4 and 5 which cross one another to form a matrix array of switching elements. The addressing of the switching elements is controlled by a data signal generator 14 and a strobe signal generator 15 by applying data waveforms in parallel to the column electrode tracks $4_1, 4_2 \dots 4_n$ and by sequentially applying a strobe waveform to the row electrode tracks $5_1, 5_2 \dots 5_m$ so as to switch selected switching elements along each row from one state to another. In order to compensate for differential waveform distortion across the display due to the effects of the different electrode track resistances seen at each column driver input, the data signal generator 14 is coupled to the column electrode tracks by compensating resistances R_1, R_2, R_3 , etc. having resistance values which vary from the first to the last columns. It is therefore possible to substantially equalise the picture quality across the display, and to ensure that temperature variations across the display caused by the different power components of the different waveforms are substantially equalised.



Description

[0001] This invention relates to addressable matrix arrays, and is concerned more particularly, but not exclusively, with ferroelectric liquid crystal devices.

[0002] Liquid crystal devices incorporating a ferroelectric smectic liquid crystal material (FLCDs) are particularly suitable for use in displays and shutters in which their fast switching times and memory characteristics are of advantage. A conventional FLCD cell comprises a layer of ferroelectric smectic liquid crystal material between two parallel glass substrates, electrode structures being typically provided on the inside facing surfaces of the glass substrates in the form of row and column electrode tracks which cross one another to form a matrix array. As is well known, switching waveforms are applied to the row and column electrode tracks in order to produce electric fields which switch the molecules within the material between two polar states having different molecular orientations. In a display device in which the cell is disposed between two polarisers having polarising axes which are substantially perpendicular to one another, a display element or pixel at the intersection of two electrode tracks may appear dark or light depending on the state to which the molecules of the pixel have previously been switched, as a result of the different light transmitting properties of the two molecular orientations.

[0003] Various addressing schemes for controlling such a matrix array FLCD are known, and reference may be made in this regard to Surguy, Ayliffe, Birch, Bone, Coulson, Crossland, Hughes, Ross, Saunders and Towler, "The Joers/Alvey Ferroelectric Multiplexing Scheme", *Ferroelectrics*, 1991, Vol. 122, pp. 63-79 which refers to a number of such addressing schemes. Typically, in large display panels, the display panel is addressed on a line-by-line basis by applying data waveforms in parallel to the column electrode tracks, each data waveform being either a switching waveform or a non-switching waveform, and by sequentially applying a strobe waveform to the row electrode tracks so as to switch selected pixels along each row from one state to the other under the effect of the electric field produced by the voltage difference between the data waveform and the strobe waveform applied to the relevant electrode tracks. In certain addressing schemes a blanking pulse is applied sequentially to the row electrode tracks which is of such a voltage and duration as to set all the pixels along each row to one state, irrespective of the data waveforms applied to the column electrode tracks. Subsequent application of strobe and data waveforms may then be used to switch selected pixels to the other state whilst leaving the remaining pixels in the one state. It is also known to apply intermediate switching waveforms to impart different grey levels to the pixels of the display.

[0004] Because of the arrangement by which the display panel is addressed on a line-by-line basis by

applying data waveforms in parallel to the column electrode tracks, the switching waveforms will be distorted to different extents across the display panel due to the different resistances encountered by the applied data pulses with the waveforms being distorted to the greatest extent at those pixels along each row which are furthest from the drive circuit applying the strobe pulses. This can result in differences in picture quality across the display, and particularly in differences in grey level and contrast, and in a reduced operating window.

[0005] Furthermore, in large display panels, in which the addressing of the display panel leads to the application of high frequency alternating voltages to the row and column electrode tracks, the power loss, due to repeated charging and discharging of the liquid crystal capacitance through the electrode tracks, can lead to a large heating effect. Since the image quality and addressing properties of such displays are highly sensitive to temperature, such heating can lead to changes in the display performance. If the temperature increases uniformly over a display panel as a result of this heating effect, then the addressing parameters can be modified, for example by modifying the switching waveforms in dependence on the sensed temperature of the panel, in order to ensure satisfactory display performance. However, if there is non-uniform temperature variation over the display panel as a result of the heating effect, it becomes difficult to compensate for such temperature variation by modification of the addressing parameters. Such temperature variations over a display panel can lead to variations in contrast ratio, greyscale, operating window, viewing angle and other display properties, and as a result it is difficult to obtain uniform display performance over a large display panel.

[0006] Japanese Patent Publication No. 2-67521A discloses a ferroelectric liquid crystal display in which the resistance of the electrodes increases further from the driving source, for example by making each electrode progressively smaller in cross-section, in order to attempt to provide a uniform temperature distribution within the display.

[0007] European Patent Publication No. 0807845A discloses a ferroelectric liquid crystal display in which the resistance in an intermediate section of each electrode track is greater than the resistance in two end sections of the electrode tracks, so as to provide increased temperature uniformity over the display during switching by the switching waveforms applied to the electrode tracks. However such arrangements do not serve to equalise the switching waveforms across the display in order to obtain more uniform picture quality.

[0008] It is an object of the invention to provide an improved addressable matrix array in which variation in the switching waveforms across the display is decreased.

[0009] According to the present invention there is provided an addressable matrix array comprising an addressable matrix of switching elements and address-

ing means for addressing each of the switching elements to control the states of the switching elements relative to one another, the addressing means comprising column electrode tracks receiving data signals from data drive means coupled to the column electrode tracks and row electrode tracks, which cross the column electrode tracks at the locations of the switching elements, receiving scanning signals from scanning drive means coupled to the row electrode tracks whereby the states of the switching elements along each row electrode track are controlled by the resultants of the scanning signal and the data signals applied to the corresponding column electrode tracks, wherein at least some of the electrode tracks are coupled to the corresponding drive means by respective impedance means, the impedance means coupling at least one of said electrode tracks to said drive means having an impedance value which is greater than that of the impedance means coupling at least one other of said electrode tracks to said drive means in order to compensate for the different effects of electrode track impedance on the resultants for controlling the states of the corresponding switching elements.

[0010] By applying suitable resistance and/or capacitance and/or inductance values to the impedance means coupling the drive means to the different electrode tracks, it is possible to compensate for the different electrode track resistances and/or capacitances and/or inductances encountered by the switching waveforms, and thereby to substantially equalise the switching waveforms across the array. In the case of a display device, such as a ferroelectric liquid crystal display, it is therefore possible to substantially equalise the picture quality across the display, for example to ensure that the contrast, the grey level or the operating window does not change significantly with position over the display panel. In addition, temperature variations across the display which would otherwise be caused by the different power components of the different waveforms may be substantially equalised.

[0011] In a preferred embodiment the row electrode tracks are coupled to the scanning drive means at one edge of the display, and the column electrode tracks are coupled to the data drive means by respective impedance means, the impedance means connected to column electrode tracks closer to said one edge of the array having impedance values which are greater than the impedance values of the impedance means connected to other column electrode tracks further away from said one edge of the array. In this case the impedance means connected to the intervening column electrode tracks between the column electrode tracks close to the opposite edges of the array have intermediate impedance values which vary substantially uniformly with the position of the corresponding electrode track relative to the column electrode tracks close to the edges of the array. In this way it can be ensured that the current drawn from each column driver is substantially

the same across the array, thus ensuring that the waveform shape is substantially the same across the array.

[0012] In a possible alternative embodiment the row electrode tracks are coupled alternately to respective scanning drive means at opposite edge of the array and the column electrode tracks are coupled to the data drive means by respective impedance means, the impedance means connected to one column electrode track in a portion of the array substantially midway between said opposite edges having an impedance value which is less than that of the impedance means connected to the column electrode tracks close to said opposite edges of the array. In this case the array may be driven on alternate rows from left and right and both ends of the array have substantially the same impedance back to ground. Preferably the middle of the array has a different impedance to ground, and current balancing is achieved by applying additional impedance to the column electrode tracks at the ends of the array.

[0013] Additionally or alternatively the row electrode tracks may be coupled to the scanning drive means by respective impedance means, the impedance means connected to row electrode tracks closer to one edge of the array having impedance values which are greater than the impedance values of the impedance means connected to other row electrode tracks further away from said one edge of the array. In this case the effect of the different impedances encountered by the scanning signals supplied to the row electrode tracks will not be so significant when the array is a display device. However the impedance values may again be chosen so as to substantially equalise the waveform distortion from row to row. Again it is preferable that intermediate impedance values are applied to the intervening row electrode tracks which vary substantially uniformly with the position of the corresponding row electrode track relative to the row electrode tracks close to the edges of the array.

[0014] The impedance means may comprise conductive tracks of different widths, the resistance value of each such impedance means being related to the width of the corresponding conductive track. Alternatively the impedance means may comprise conductive tracks having reduced width portions of different lengths, the resistance value of each such impedance means being related to the length of the reduced width portion of the corresponding conductive track. Furthermore these conductive tracks may form input portions of the column and/or row electrode tracks.

[0015] In order that the invention may be more fully understood a FLCD incorporating an addressable matrix array in accordance with the invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic cross-section through a portion of the FLCD;

Figure 2 is a block diagram of the FLCD addressing

arrangement;

Figure 3 is a graph showing the first and last column voltage waveforms and the first and last column drive currents predicted by SPICE modelling of an addressable matrix array without current balancing;

Figure 4 is a graph showing the distorted voltage waveforms at the four corners of an addressable matrix array using SPICE modelling without current balancing, both for the resultant of the data and strobe waveforms and for the data waveform alone;

Figure 5 is a graph showing the distorted voltage waveforms at the four corners of an addressable matrix array using SPICE modelling with current balancing, both for the resultant of the data and strobe waveforms and for the data waveform alone;

Figure 6 is a block diagram of a modified FLCD addressing arrangement;

Figure 7 is a graph showing the distorted voltage waveforms of an array utilising such an addressing arrangement, both for the resultant of the data and strobe waveforms and for the data waveform alone;

Figure 8 is a block diagram of an FLCD addressing arrangement utilising current balancing; and

Figures 9 and 10 are graphs showing the values of added resistances added to the columns in such an addressing arrangement.

[0016] The FLCD panel 10 shown diagrammatically in Figure 1 comprises a layer 63 of ferroelectric smectic liquid crystal material contained between two parallel glass substrates 61 and 62 bearing first and second electrode structures on their inside surfaces. The first and second electrode structures comprise respectively a series of row and column electrode tracks 4 and 5 which cross one another to form a matrix array of switching elements or pixels. Furthermore alignment layers 66 and 67 are provided on baffle layers 64 and 65 on top of the row and column electrode tracks 4 and 5, so that the alignment layers 66 and 67 contact opposite sides of the ferroelectric liquid crystal layer 63 which is contained at its edges by a sealing member 68.

[0017] The panel 10 is disposed between polarisers 69 and 70 having polarising axes which are substantially perpendicular to one another. It will be understood that such a FLCD constitutes only one type of addressable matrix array to which the invention is applicable, and the following description of such a display is therefore to be considered as being given only by way of non-limiting example.

[0018] The addressing of the pixels of the display is controlled by a data signal generator 14 having respective signal outputs $D_1, D_2 \dots D_n$ coupled to the column electrode tracks $4_1, 4_2 \dots 4_n$, and a strobe signal generator 15 having signal outputs $S_1, S_2 \dots S_m$ coupled to the row electrode tracks $5_1, 5_2 \dots 5_m$. As is well known, the display panel is addressed on a line-by-line basis by applying data waveforms in parallel to the column elec-

trode tracks $4_1, 4_2 \dots 4_n$, and by sequentially applying a strobe waveform to the row electrode tracks $5_1, 5_2 \dots 5_m$ so as to switch selected pixels along each row from one state to another under the effect of the electric field produced by the voltage difference between the data and strobe waveforms applied to the relevant electrode tracks. The pixels may be switched between different switching states corresponding to different grey levels depending on the form of the data waveforms. Furthermore the data signal generator 14 and strobe signal generator 15 are controlled by a logic control unit 16 to which an input is supplied by an analogue or digital video input circuit 17.

[0019] When a display panel is driven from two edges of the panel as shown in Figure 2, that is from one edge to which the data signal generator 14 is connected and another edge to which the strobe signal generator 15 is connected, the currents drawn from the different column drivers of the data signal generator 14 are unequal due to the different resistances of the signal outputs $D_1, D_2 \dots D_n$ relative to 0 volts. This leads to differences in the shapes of the signal waveforms applied from the first column electrode track 4_1 to the last column electrode track 4_n which can change the optical properties of the display in an undesirable manner. In addition the different waveforms will have different power components giving rise to uneven temperature rises across the display in operation.

[0020] Such variation in waveform shape across the display is illustrated by the graph of Figure 3 in which the lines A and B denote the currents drawn from the first and last column drivers and the lines C and D denote the voltage waveforms applied to the pixels addressed by the first and last column electrode tracks on the first row of the panel. As shown in this graph the waveform applied to the pixel (Out, In) addressed by the last column electrode track along the first row is distorted to a greater extent than the waveform applied to the pixel (In, In) addressed by the first column electrode track along the row. This is due to the different resistance in the ground return from each column driver due to the different length of the row electrode track incorporated in the return path. Thus, in the case of the last column driver, the return path includes virtually the complete length of the first row electrode track 5_1 and the resistance will therefore correspond to substantially the complete resistance of the track (that is the product of the resistance per unit length and the length of the track), whereas the resistance associated with the first column driver will be considerably smaller since it will correspond only to the resistance of the short portion of the row electrode track 5_1 between the corresponding pixel and the output S_1 of the strobe signal generator 15. It will be seen that the current A drawn by the first column driver peaks much higher and drops off sharply, and this ready supply of current results in a voltage waveform C which is not distorted much. By contrast the current B drawn by the last column driver has a much

lower peak and is drawn for much longer, with the result that the corresponding voltage waveform D is more distorted.

[0021] In accordance with the preferred embodiment of the invention, the data signal generator 14 is coupled to the column electrode track 4_1 $4_2 \dots 4_n$ by compensating resistances R_1 , R_2 , R_3 , etc., as shown in Figure 8, having resistance values which vary from the first to the last columns, for example which vary from a value R for the first column electrode track 4_1 to zero for the last column electrode track 4_n (with intermediate values being substantially evenly spaced between these two extreme values) where R is also the output impedance of the column drivers. In this case R corresponds to the resistance along the row electrode track 5_1 so that the addition of these resistance values substantially equalises the overall resistances of the current paths associated with the different column drivers. It should be appreciated that, in this case, the row electrode track resistance corresponds to the column driver impedance R , but that the row electrode track resistance may have a different value X in which case the resistance value X (rather than R) may be added to the first column with no additional resistance being added to the last column.

[0022] Figure 9 is a graph showing the values of the resistances R_1 , R_2 , R_3 , etc. as a function of the distance x of the associated column electrode tracks 4_1 , 4_2 , 4_3 , etc. from the strobe signal generator 15 in the panel 10. It will be appreciated from this graph that the values of the resistances R_1 , R_2 , R_3 , etc. decrease linearly as a function of the distance x , that is the values are evenly spaced apart along a straight line of a particular slope in this graph.

[0023] Figure 10 shows a corresponding graph for a variant addressing arrangement utilising spatial dither for obtaining different grey levels. In this case the column electrode tracks incorporate thin tracks and thick tracks which can be addressed by means of a spatial dither addressing arrangement in order to control the states of different sized pixels to obtain different grey levels in known manner. The thin and thick tracks have different values of resistance per unit length, and accordingly it is necessary to apply different current balancing arrangements for the thin tracks and for the thick tracks. Thus, as shown in the figure, resistances R_1 , R_2 , R_3 , etc., which are linearly spaced apart, are applied to the thick tracks, whereas different resistances r_1 , r_2 , r_3 , etc., which are also linearly spaced apart relative to one another, are applied to the thin tracks. It will be appreciated that the two sets of resistances R_1 , R_2 , R_3 , etc. and r_1 , r_2 , r_3 , etc. lie on two parallel lines 30 and 31 in the graph. Alternatively or additionally, the row electrode tracks may comprise thin and thick tracks for the purposes of spatial dither, and Figure 8 illustrates such thin and thick tracks having widths of y and y_n respectively.

[0024] In a further variant, it would be possible for the strobe signal generator to be connected to the row electrode tracks in a mid portion of the display in which

case the resistance values added to the column electrode tracks may have values which decrease linearly symmetrically on either side of the mid portion. Considering, for example, the spatial dither addressing arrangement of Figure 10, this would then result in similar sets of resistances R_1 , R_2 , R_3 , etc. and r_1 , r_2 , r_3 , etc. being applied symmetrically on either side of the mid portion such that the resistances of each set decrease proportionately in either direction as a function of the distance from the mid portion.

[0025] Figure 4 is a graph showing the distorted voltage waveforms at the four corners of the display, both for the resultant 24 of the strobe and data waveforms and for the data waveform 25 alone, utilising SPICE modelling of such an addressable matrix array in which no current balancing is applied and in which the matrix consists of 12 rows and 38 columns with a row resistance of $0.1 \Omega/\text{sqr}$, a column resistance of $0.15 \Omega/\text{sqr}$, a column driver impedance of 300Ω and a row driver impedance of 50Ω . In this case no current balancing is applied by the addition of resistance values to the electrode tracks. The four voltage waveforms at the four pixels at the corners of the array, having the coordinates (In,In), (In,Out), (Out,Out) and (Out,In), are shown superimposed on one another so as to illustrate the relative distortions of the waveforms. It will be seen that the greatest waveform distortion is obtained at the bottom right hand corner of the array, that is at the pixel (Out,Out).

[0026] By contrast Figure 5 shows the corresponding distorted voltage waveforms 24 and 25 for a similar model of a matrix array in which current balancing is applied by the application of varying resistance values to the coupling between the data signal generator 14 and the column electrode tracks 4_1 , $4_2 \dots 4_n$ varying from 700Ω to 300Ω from the first column driver to the last column driver with the intermediate resistance values being evenly spread within the intervening range. In this case there is a notable reduction in the spread of waveform distortion as between the resultant waveforms applied to the pixels (In,In), (In,Out), (Out,Out) and (Out,In), both as regards the voltage waveform 24 and the voltage waveform 25. In the case of a FLCD this results in more uniform optical properties across the display, as well as in more even temperature rises across the display.

[0027] Such current balancing can be extended to the row electrode tracks so as to compensate for some of the waveform distortion introduced by the row electrode resistance. In this case a resistance value of about 50Ω (equivalent to the track length resistance) may be provided between the strobe signal generator 15 and the first row electrode track 5_1 whereas no additional resistance is applied between the generator 15 and the last row electrode track 5_m (with intermediate resistance values being applied to the intervening row electrode tracks $S_2 \dots S_{m-1}$). However it should be noted that the general effect of current balancing is to match

the best quality waveforms to the worst quality waveforms so that, although it reduces the spread of distortion, the current balancing may have the effect of moving the display operating point away from the ideal display operating point which would be obtained by use of undistorted switching waveforms.

[0028] In a development of the invention, as shown diagrammatically in Figure 6, alternate row electrode tracks are driven from left and right strobe signal generators 20 and 21 with the result that both end column drivers have substantially the same resistance back to ground. Figure 7 is a graph showing the voltage waveforms 24 and 25 at the four corner pixels (In,In), (In,Out), (Out,Out) and (Out, In) for such a matrix array in which alternate rows are driven from opposite ends, but in which no other current balancing measures are taken. It will be appreciated that, as compared with the graph of Figure 4, the spread of waveform distortion is reduced in a broadly similar manner to the current balancing arrangement previously described producing a reduction in the waveform distortion shown in Figure 5. However the middle column drivers in Figure 6 will still have a greater resistance back to ground than the end column drivers, and accordingly it is believed that a further reduction in the spread of waveform distortion may be obtained in accordance with the invention by the addition of resistance values to at least the end column drivers so as to substantially equalise the resistance with respect to ground of all the column drivers. However this has not been experimentally verified.

[0029] It will be appreciated that the above description of embodiments of the invention is given only by way of example, and that the invention is applicable to other types of addressable matrix array in which waveform distortion can be equalised over the array or over a portion of the array by compensating for such distortion caused by any combination of capacitance, resistance and inductance along the column and row electrode tracks. In this case the appropriate compensation is effected by the addition of appropriate impedance values (consisting of combinations of capacitance and/or resistance and/or inductance values) to the appropriate column and/or row electrode tracks.

[0030] Furthermore the applied resistances of varying resistance values may be constituted by end portions of the column or row electrode tracks, or by further metalisation tracks electrically coupled to the end portions of the column or row electrode tracks. These additional resistance portions may be made to have different resistance values by being narrower than the rest of the track and by ensuring that each narrowed portion of different resistance value has a different width. Alternatively or additionally each narrowed portion may be made to have a different resistance value by being of a different length. In this case the narrowed portions of all the tracks may have the same width, and their resistance values may be varied simply by varying the length of the narrowed portion. The narrower the width the

greater is the resistance value of the portion, and the greater the length of the narrowed portion the greater is its resistance value. However the additional resistances may also simply be formed by conventional resistors having different resistance values.

Claims

1. An addressable matrix array comprising an addressable matrix of switching elements (7) and addressing means for addressing each of the switching elements to control the states of the switching elements (7) relative to one another, the addressing means comprising column electrode tracks (4) receiving data signals from data drive means (14) coupled to the column electrode tracks and row electrode tracks (5), which cross the column electrode tracks (4) at the locations of the switching elements (7), receiving scanning signals from scanning drive means (15) coupled to the row electrode tracks (5) whereby the states of the switching elements (7) along each row electrode track (5) are controlled by the resultants of the scanning signal and the data signals applied to the corresponding column electrode tracks (4), wherein at least some of the electrode tracks (4, 5) are coupled to the corresponding drive means (14, 15) by respective impedance means ($R_1, R_2, R_3 \dots$), the impedance means coupling at least one of said electrode tracks (4, 5) to said drive means (14, 15) having an impedance value which is greater than that of the impedance means coupling at least one other of said electrode tracks (4, 5) to said drive means (14, 15) in order to compensate for the different effects of electrode track impedance on the resultants for controlling the states of the corresponding switching elements (7).
2. An array according to claim 1, wherein the row electrode tracks (5) are coupled to the scanning drive means (15) at one edge of the array (10), and the column electrode tracks (4) are coupled to the data drive means (14) by respective impedance means ($R_1, R_2, R_3 \dots$), the impedance means connected to column electrode tracks (4) closer to said one edge of the array (10) having impedance values which are greater than the impedance values of the impedance means connected to other column electrode tracks (4) further away from said one edge of the array (10).
3. An array according to claim 2, wherein the impedance means ($R_1, R_2, R_3 \dots$) connected to the column electrode tracks (4) between one column electrode track (4) close to said one edge of the array (10) and another column electrode track (4) close to an opposite edge of the array (10) have impedance values which are between the imped-

ance values of the impedance means connected to said one column electrode track (4) and said other column electrode track (4) and which vary substantially uniformly with the position of the corresponding column electrode track (4) relative to said one column electrode track (4) and said other column electrode track (4).

4. An array according to claim 2 or 3, wherein the impedance means ($R_1, R_2, R_3 \dots$) connected to one column electrode track (4) close to said one edge of the array (10) has an impedance value which is approximately twice that of the impedance means connected to another column electrode track (4) close to an opposite edge of the array (10).
5. An array according to claim 1, wherein the row electrode tracks (15) are coupled alternately to respective scanning drive means (20, 21) at opposite edges of the array (10), and the column electrode tracks (4) are coupled to the data drive (14) means by respective impedance means ($R_1, R_2, R_3 \dots$), the impedance means connected to one column electrode track (4) in a portion of the array (10) substantially midway between said opposite edges having an impedance value which is less than that of the impedance means connected to the column electrode tracks (4) close to said opposite edges of the array (10).
6. An array according to any preceding claim, wherein the row electrode tracks (5) are coupled to the scanning drive means (15, 20, 21) by respective impedance means ($R_1, R_2, R_3 \dots$), the impedance means connected to row electrode tracks (5) closer to one edge of the array (10) having impedance values which are greater than the impedance values of the impedance means connected to other row electrode tracks (5) further away from said one edge of the array (10).
7. An array according to claim 6, wherein the impedance means ($R_1, R_2, R_3 \dots$) connected to the row electrode tracks (5) between one row electrode track (5) close to said one edge of the array (10) and another row electrode track (5) close to an opposite edge of the array (10) have impedance values which are between the impedance values of the impedance means connected to said one row electrode track (5) and said other row electrode track (5) and which vary substantially uniformly with the position of the corresponding row electrode track relative to said one row electrode track and said other row electrode track.
8. An array according to any preceding claim, wherein the impedance means ($R_1, R_2, R_3 \dots$) have impedance values which are chosen so as to substantially

equalise waveform distortion across the array (10) due to the different impedances with respect to ground encountered by the signals applied by the drive means (14, 15) to different electrode tracks (4, 5).

9. An array according to any preceding claim, wherein the impedance means ($R_1, R_2, R_3 \dots$) comprise conductive tracks of different widths, the resistance value of each such impedance means being related to the width of the corresponding conductive track.
10. An array according to any preceding claim, wherein the impedance means ($R_1, R_2, R_3 \dots$) comprise conductive tracks having reduced width portions of different lengths, the resistance value of each such impedance means being related to the length of the reduced width portion of the corresponding conductive track.
11. A ferroelectric liquid crystal device incorporating an addressable matrix array according to any preceding claim.

Fig. 1

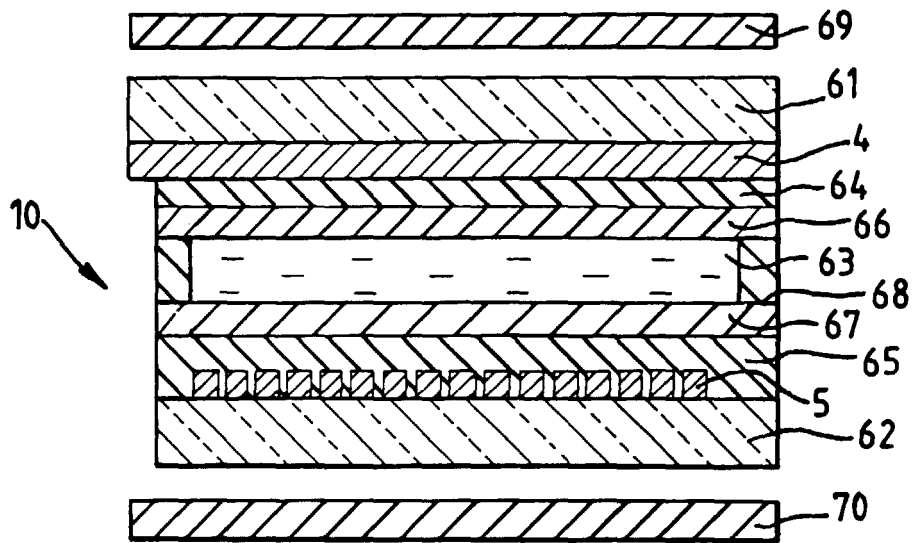


Fig. 2

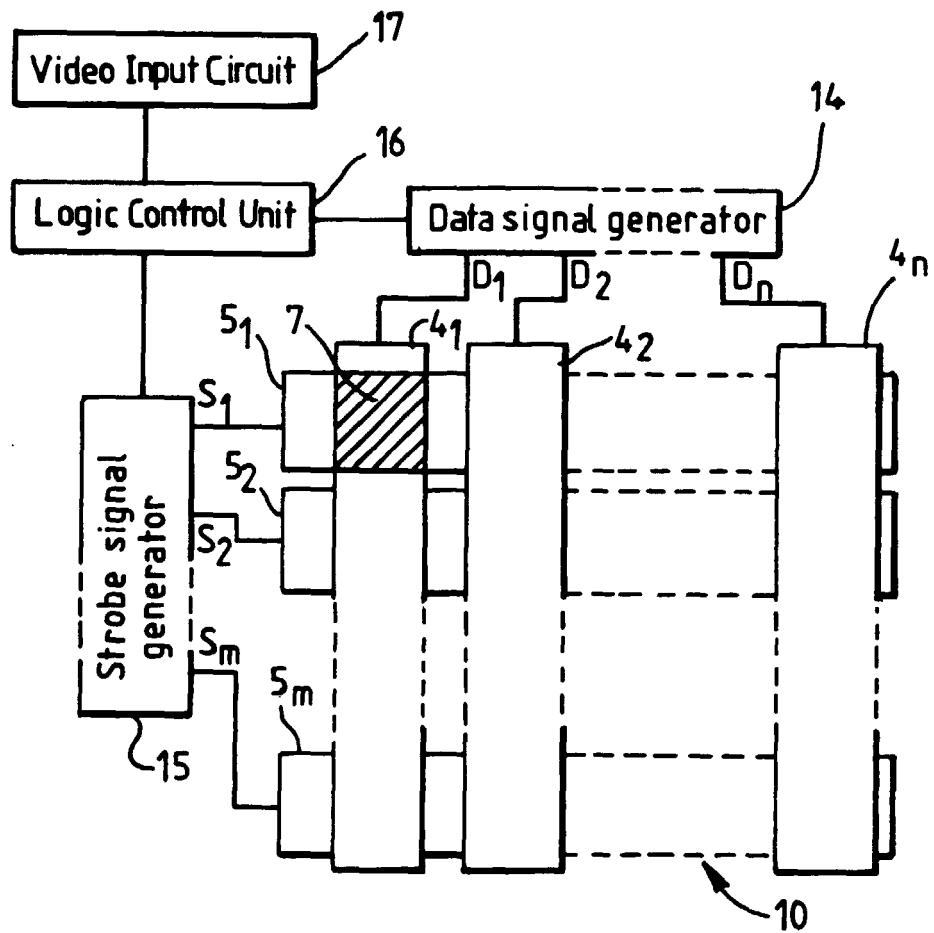


Fig. 3

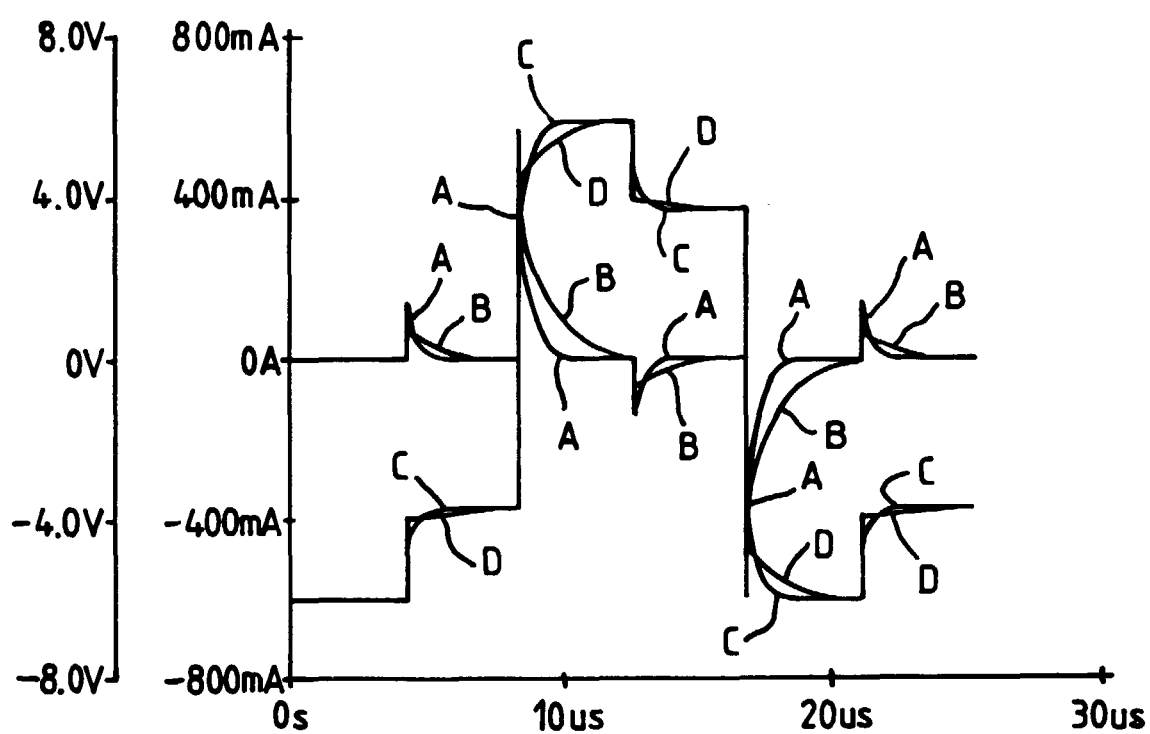


Fig. 4

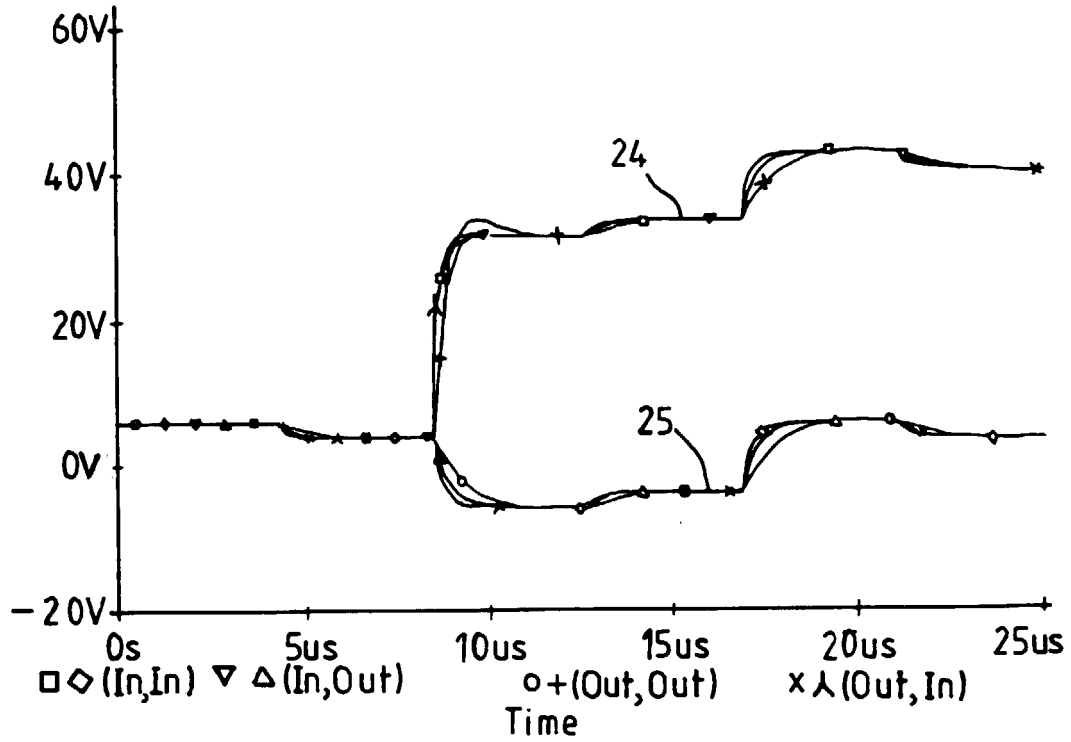


Fig. 5

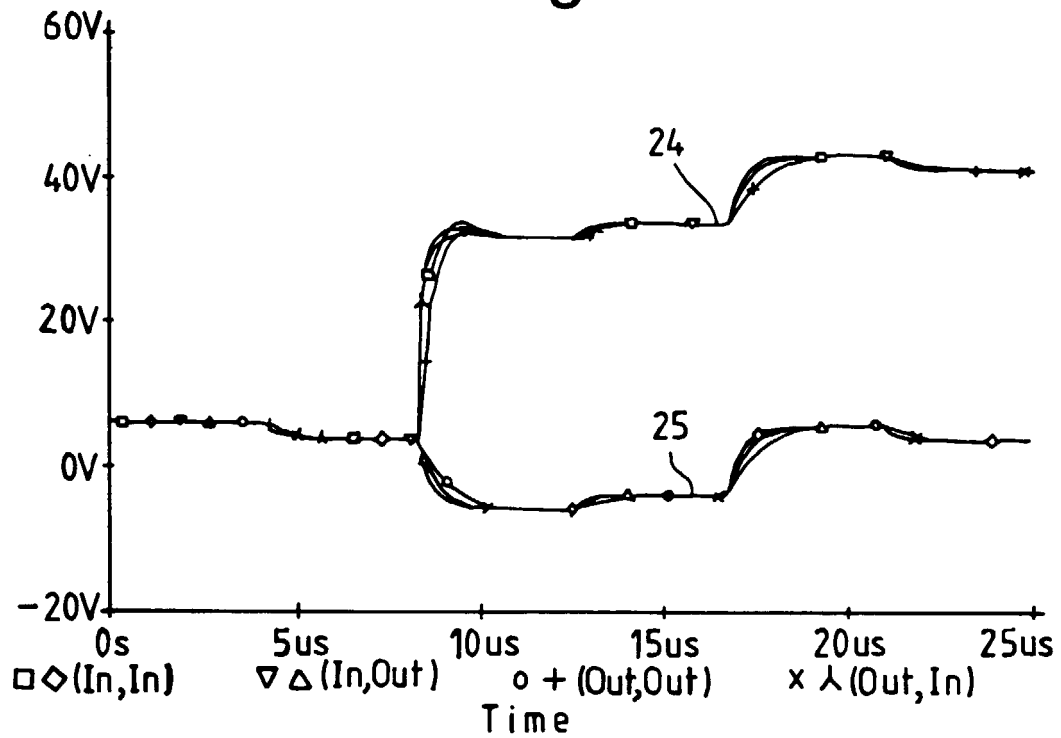


Fig. 6

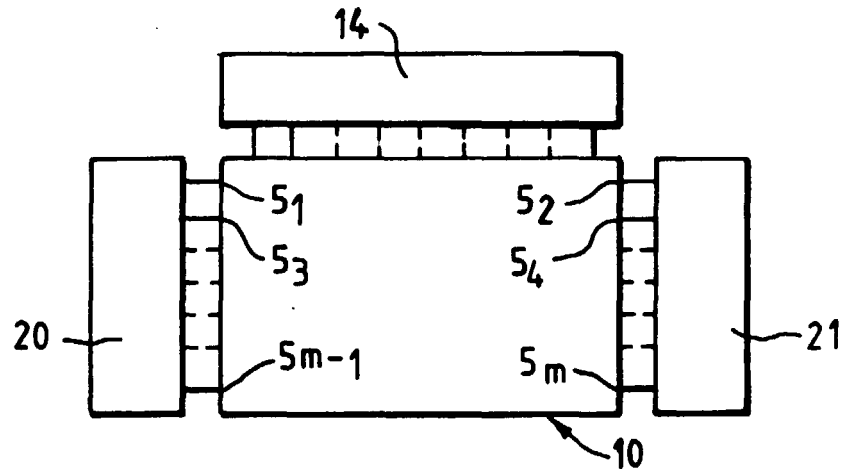


Fig. 7

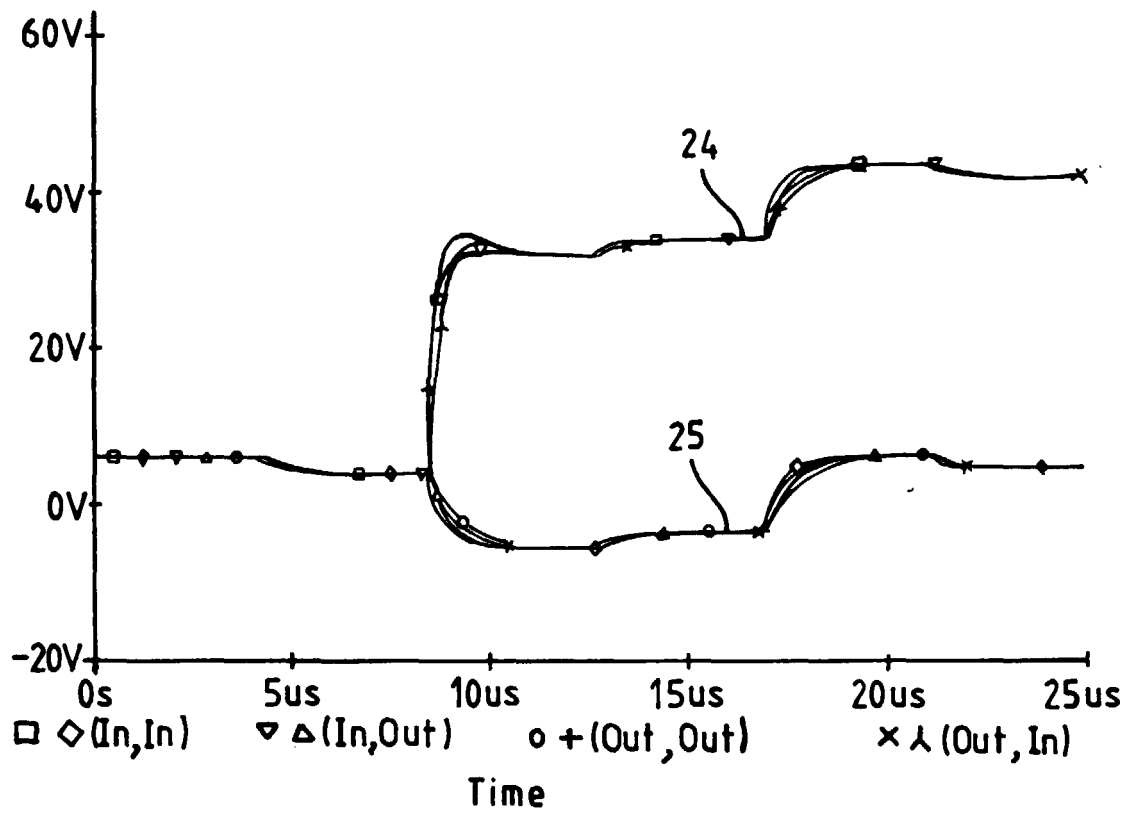


Fig. 8

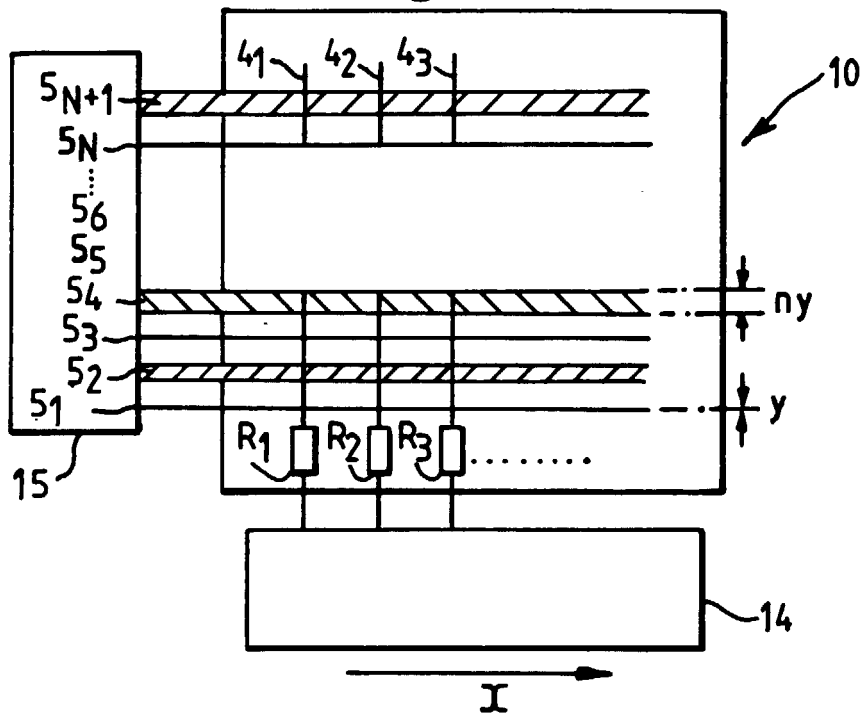


Fig. 9

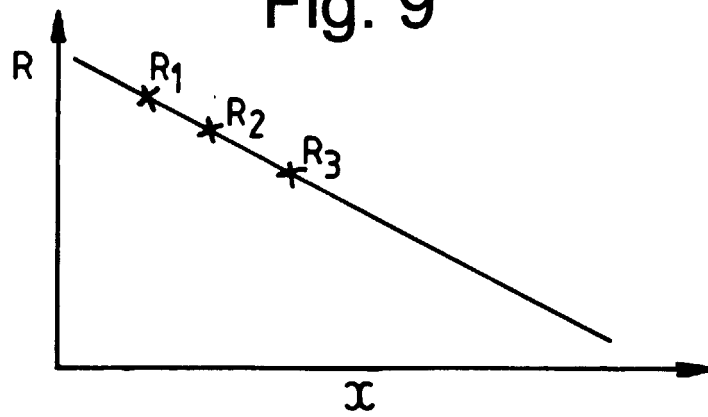


Fig. 10

