(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 032 047 B9

(12) # CORRECTED EUROPEAN PATENT SPECIFICATION

(15) Correction information:
Corrected version no 1 (W1 B1)
Corrections, see
Claims EN 1

(48) Corrigendum issued on:
09.02.2011 Bulletin 2011/06

(45) Date of publication and mention of the grant of the patent:
22.09.2010 Bulletin 2010/38

(21) Application number: **00301097.2**

(22) Date of filing: **11.02.2000**

(51) Int Cl.:
H01L 29/739 (2006.01) *H01L 29/06* (2006.01)
H01L 23/528 (2006.01) *H02M 7/527* (2006.01)

(54) **Semiconductor device and power converter using the same**

Halbleiterbauelement und dieses verwendender Leistungswandler

Dispositif semiconducteur et convertisseur de puissance l'utilisant

(84) Designated Contracting States:
DE FR GB

(30) Priority: **17.02.1999 JP 3816699**

(43) Date of publication of application:
30.08.2000 Bulletin 2000/35

(60) Divisional application:
07009037.8 / 1 811 572
10007172.9 / 2 237 319

(73) Proprietor: **Hitachi, Ltd.**
Chiyoda-ku,
Tokyo (JP)

(72) Inventors:
- **Oyama, Kazuhiro**
  Hitachi-shi,
  Ibaraki 316-0036 (JP)
- **Sakano, Jyunichi**
  Hitachi-shi,
  Ibaraki 310-1225 (JP)
- **Mori, Mutsuhiro**
  Mito-shi,
  Ibaraki 310-0842 (JP)

(74) Representative: **Calderbank, Thomas Roger et al**
Mewburn Ellis LLP
33 Gutter Lane
London
EC2V 8AS (GB)

(56) References cited:
EP-A- 0 746 030 EP-A- 0 889 531

- **PATENT ABSTRACTS OF JAPAN vol. 1996, no. 09, 30 September 1996 (1996-09-30) & JP 08 116056 A (HITACHI LTD), 7 May 1996 (1996-05-07)**

EP 1 032 047 B9

Description

[0001] The present invention relates to a semiconductor device and particularly to an insulating gate type bipolar transistor having a trench insulating gate structure and a power converter using it.

[0002] An insulating gate type bipolar transistor (hereinafter abbreviated to IGBT) is conventionally known as a power semiconductor element. During the ON operation, the pnp transistor operates and the conductivity is modulated, so that the IGBT has an advantage that the ON voltage can be lowered. However, it is a transistor operation, so that the conductivity modulation is not sufficient compared with the thyristor operation and the ON voltage is high compared with the GTO thyristor.

[0003] Recently, the trench insulating gate type IGBT is begun to be noticed as a power semiconductor element. The trench type IGBT has a structure that the insulating gate is embedded in the semiconductor. As a basic constitution, on one surface of the n-type base layer of high resistance, the p-type collector layer is formed across the n-type buffer layer. On the other surface of the n-type base layer, the p-type base layer is formed. On the p-type base layer, trench gate electrodes having a plurality of same shapes that the plane shape is changed to a stripe shape are formed. The trench electrodes are in a shape that the electrodes and their surroundings are covered with an insulating film. Therefore, the trench gate electrodes are structured so that their side walls are MOS channels.

[0004] In the trench insulating gate type IGBT, the insulating gates can be formed densely compared with the planar IGBT, so that the channel width is wider and the channel resistance is low. As a result, compared with the conventional planar IGBT, a low ON voltage (ON voltage: saturation voltage between the collector and the emitter) is obtained.

[0005] In the trench insulating gate type IGBT, as the channel width increases, the saturation current increases and the short-circuit withstand amount reduces.

[0006] The structure using trench insulating gates is described in Japanese Patent Application Laid-Open 5-243561. This is a structure that the injection effect of holes into the n-type base layer is increased. Concretely, in the trench insulating gate type IGBT having trench insulating gates formed at equal intervals or widely, the number of channels formed on the side walls of the trench insulating gates are reduced and the channel width is narrowed. Furthermore, the p-type base layer which is positioned on the other surface on the side where no channels are formed is covered with an insulating film and isolated from the main electrode. It is said that this structure increases the injection effect and provides a conductivity modulation close to that of the thyristor. As a result, although the channel resistance increases, the resistance when the n-type base layer is used reduces and a low ON voltage is obtained. However, since the gate input capacity is large and hence the switching is slow, a problem arises that the switching loss is large particularly in high frequency waves. A problem also arises that the drive power is large.

[0007] A structure for solving such problems is described in Japanese Patent Application Laid-Open 10-178176. The characteristic of this structure is that the interval of the gates forming no channels is wider than the interval of the gates forming channels and such a status is repeated.

[0008] By doing this, the gate input capacity, switching loss, and drive power can be reduced. However, to reduce the loss sufficiently, it is necessary to widen the interval of the gates forming no channels and a problem arises that the withstand voltage of the element reduces.

[0009] EP 0 746 030 describes a trench-gated power MOSFET device defining a plurality of MOSFET cells. A protective diffusion in the form of a diode is constructed, the diode being connected in parallel with the channel region in each of the MOSFET cells.

[0010] The present invention has been developed in consideration of the aforementioned problems and provides a semiconductor device of the trench insulating gate type for improving electric characteristics.

[0011] In a first aspect, there is provided an insulated gate bipolar transistor comprising: a first semiconductor layer of a first conductive type, a second semiconductor layer of a second conductive type neighbouring to said first semiconductor layer, a third semiconductor layer of said first conductive type neighbouring to said second semiconductor layer, a plurality of insulated gates passing through said third semiconductor layer and reaching said second semiconductor layer, a first area and a second area which are areas between said neigh boring insulated gates and neighbouring to each other, a fourth semiconductor layer of said second conductive type in contact with said insulated gates in said third semiconductor layer in said first area, a first main electrode electrically connected to said third semiconductor layer and said fourth semiconductor layer in said first area, and a second main electrode electrically connected to said first semiconductor layer, wherein: assuming an interval between said neighbouring insulated gates in said first area as La and an interval between said neighbouring insulated gates in said second area as Lb, $La \leqq 5\ \mu m$ and $Lb/La > 1$; and a fifth semiconductor layer of said first conductive type either

(i) deeper than said third semiconductor layer or
(ii) deeper than the bottom of said insulated gates is installed in said second area, and said first main electrode is insulated from said fifth semiconductor layer by an insulating film.

[0012] Since $Lb/La > 1$, a low ON voltage is ensured and the saturation current density is reduced in addition. To ensure a low ON voltage, $6 > Lb/La > 2$ is desirable. $La \leqq 5\ \mu m$ is also desirable.

[0013] Preferably, in the second area, a fifth semiconductor layer of the first conductive type which is deeper than the third semiconductor layer is provided. By use of the fifth semiconductor layer, even if the interval between neighboring insulating gates in the second area is made larger than the interval between neighboring insulating gates in the first area, the withstand voltage does not reduce so much. The aforementioned semiconductor device of the present invention, by making the interval between neighboring insulating gates in the second area larger than the interval between neighboring insulating gates in the first area, can produce an effect of reducing the saturation current density and improving the short-circuit withstand amount or an effect of reducing the ON voltage or power loss. However, to obtain a sufficient short-circuit withstand amount, it is desirable that the saturation current density is less than 1000 A/cm^2. To reduce the ON voltage or power loss, it is desirable that the third semiconductor layer and the fifth semiconductor layer in the second area and the first main electrode are insulated by an insulating film and furthermore, the third semiconductor layer in the first area and the third semiconductor layer in the second area are separated from each other. It is also valid to reduction in the ON voltage or power loss that in the first area, the second semiconductor layer has a first portion of the first semiconductor layer and a second portion of the third semiconductor layer that the impurity density is higher than that of the first portion. On the other hand, to improve the turn-off performance such as reduction in the turn-off loss and shortening of the turn-off time, it is desirable that a Zener diode is connected between the fifth semiconductor layer and the first main electrode. By doing this, when a high voltage is applied during turn-off, the Zener diode breaks over, and a current flows, and the accumulation carrier is pulled out from the fifth deep semiconductor layer. Therefore, the turn-off performance is improved.

[0014] In the aforementioned semiconductor device of the present invention, the first conductive type and second conductive type are the p type or n type and reverse conductive types respectively. As an insulating gate, a trench insulating gate formed in a so-called trench groove such that a groove passing through the third semiconductor layer and reaching the second semiconductor layer is formed and a gate electrode insulated by an insulating film covering the inner side wall and bottom of the groove is formed in the groove can be applied. The second semiconductor layer may have a first portion in contact with the first semiconductor layer and a second portion of the third semiconductor layer that the impurity density is lower than that of the first portion. The first portion is equivalent to a so-called buffer layer.

[0015] Among the aforementioned constitution, the following constitutions a, b, and c independently produce their effects respectively regardless of the existence of the fifth semiconductor layer.

a. The third semiconductor layer in the second area and the first main electrode are insulated by an insulating film and the third semiconductor in the first area and the third semiconductor layer in the second area are separated.

b. In the first area, the second semiconductor layer has a first portion of the first semiconductor layer and a second portion of the third semiconductor layer that the impurity density is higher than that of the first portion.

c. A Zener diode is connected between the third semiconductor layer in the second area and the first main electrode and preferably further, the third semiconductor layer in the second area and the first main electrode are insulated by an insulating film.

[0016] Namely, these constitutions are the first semiconductor layer of the first conductive type, the second semiconductor layer of the second conductive type neighboring to the first semiconductor layer, the third semiconductor layer of the first conductive type neighboring to the second semiconductor layer, a plurality of insulating gates passing through the third semiconductor layer and reaching the second semiconductor layer, and areas between neighboring insulating gates, and they are applied to a semiconductor device having the first area and second area which are neighboring to each other, the fourth semiconductor layer of the second conductive type in contact with insulating gates in the third semiconductor layer in the first area, and the first main electrode in contact with the third semiconductor layer and fourth semiconductor layer in the first area and the second main electrode in contact with the first semiconductor layer, wherein the interval between neighboring insulating gates in the second area is larger than the interval between neighboring insulating gates in the first area, and they independently produce effects respectively.

[0017] The semiconductor device of the present invention can be used for a power converter for converting the power by turning the semiconductor switching element on or off. The power converter has a pair of DC terminals, a plurality of series connection circuits connected between the DC terminals in which a plurality of semiconductor switching elements are connected in series, and a plurality of AC terminals connected to each DC series connection point of a plurality of DC connection circuits. These plurality of semiconductor switching elements are the semiconductor device of the present invention. According to this power converter, the reliability and efficiency of a power converter can be improved. As a power converter, there are an invertor for converting the DC power to an AC power and a converter for converting the AC power to a DC power.

[0018] In the drawings:

Fig. 1 is a cross sectional view for explaining the constitution of the first embodiment relating to the present invention.

Fig. 2 is a graph for explaining the effect of the embodiment.

Fig. 3 is a cross sectional view for explaining the constitution of the second embodiment relating to the present invention.

Fig. 4 is a cross sectional view for explaining the constitution of the third embodiment relating to the present invention.

Fig. 5 is a plan view for explaining the terminal constitution of the first embodiment relating to the present invention.

Fig. 6 is a cross sectional view of A-A' shown in Figs. 5, 8, and 9.

Fig. 7 is a cross sectional view of B-B' shown in Figs. 5, 8, and 9.

Fig. 8 is a plan view for explaining the trench gate structure relating to the present invention.

Fig. 9 is a plan view for explaining the trench gate structure relating to the present invention.

Fig. 10 is a cross sectional view for explaining an embodiment of a crimp type element relating to the present invention.

Fig. 11 is a cross sectional view for explaining an embodiment of another crimp type element relating to the present invention.

Fig. 12 is a circulation diagram for explaining an embodiment of a 3-phase invertor using an insulating gate type trench type IGBT relating to the present invention.

Fig. 13 is a plan view of the eighth embodiment relating to the present invention.

Fig. 14 is a cross sectional view of A-A' shown in Fig. 13.

Fig. 15 is a cross section view of the ninth embodiment relating to the present invention.

Fig. 16 is a solid perspective view of the tenth embodiment relating to the present invention.

[0019] Fig. 1 shows the first embodiment of the present invention and a cross sectional view of a cell of a trench insulating gate type IGBT.

[0020] On the trench insulating gate type IGBT, on one surface of the n-type base layer 1 (second semiconductor layer) of high resistance, the p-type collector layer 2 (first conductor layer) is formed across the n-type buffer layer 3 whose impurity density is higher than that of the n-type base layer 1. On the other surface of the n-type base layer 1, the p-type base layer (third semiconductor layer) is formed.

[0021] On the p-type base layer 4, a plurality of trench insulating gate electrodes 7 (insulating gates) having the same shape that the plane shape is striped are formed so deep that they reach the n-type base layer 1. The trench insulating gate electrodes 7 are shapes so that the gate electrodes are embedded in the groove reaching the n-type base layer 1 from the surface of the p-type base layer 4 and the periphery of the gate electrodes is covered with an insulating film. These trench insulating gate electrodes 7 are structured so that as to the mutual intervals of neighboring trench insulating gates, the narrow La and wide Lb appear alternately. According to this embodiment, the mutual intervals are indicated with the side wall of the trench groove as the starting point. However, the center in the direction of the width of the trench insulating gates may be used as the starting point.

[0022] In the area La, the n-type source layer 5 (fourth semiconductor layer) whose impurity density is higher than that of the p-type base layer 4 is formed by impurity diffusion so that the plane shape is striped in contact with trench insulating gates. By doing this, the n-type MOSFET portion which is a channel area where the side of the p-type base layer 4 is controlled by the trench gate electrodes 7 is structured. In the area La, the p+ layer 6 whose impurity density is higher than that of the p-type base layer 4 is formed across the n-type source layer 5 deeper than the n-type source layer 5.

[0023] In the area Lb, the p-type base layer 4 is formed in the same depth as the area La so as to be separated from the p-type base layer in the area La and also at the center of the p-type base layer 4, the p-type well layer 9 (fifth semiconductor layer) is formed deeper than the p-type base layer 4 and equally deep to or deeper ($Lc \geqq 0$) than the trench insulating gate electrodes 7. The distance Le between the trench gate electrodes 7 at the bottom of the trench gate electrodes 7 and the p-type well layer 9 is set sufficiently wide so that the withstand voltage of the element is not lowered.

[0024] The main electrode 10 (emitter electrode, first main electrode), in the area La, touches the n-type source layer 5 and the p+ layer 6 at the same time. The other main electrodes 11 (collector electrodes, second main electrodes) touch the p-type collector layer 2. In the area Lb, the main electrode 10 is insulated from the p-type base layer 4 and the p-type well layer 9 by an insulating film.

[0025] The operation of this embodiment is described below. The voltage is applied so that the potential of the main electrodes 11 is set higher than the potential of the main electrode 10 and the potential of the trench insulating gate electrodes 7 is set higher than the potential of the main electrode 10. When the voltage of the trench insulating gate electrodes 7 is more than the threshold voltage, an n-type channel is formed on the surface in contact with the gate insulating film of the p-type base layer 4 and electrons flow into the n-type base layer 1 via the channel from the n-type source layer 5 and the n-type base layer 1 is turned on. In this case, holes are injected into the n-type base layer 1 from the p-type collector layer 2 and a conductivity modulation is generated in the n-type base layer 1. In this embodiment, no channel is formed in the area Lb, so that a deep conductivity modulation is generated. Therefore, the element of this embodiment has characteristics of low ON voltage. Furthermore, when $La < Lb$ is set, the area occupied by the gates is reduced, so that the gate input capacity can be made smaller. In this embodiment, although the main continuity area is the area La, since the p-type collector layer 2 extends from the area La to the area Lb, holes are injected also from the p-type collector layer 2 in the area Lb into the n-type base layer 1. The holes also contribute to conductivity modulation. The main electrodes 11 are in ohmic contact with the p-type collector layer 2 also in the area Lb, so that more holes are injected from the p-type collector layer 2 in the area Lb.

[0026] The channel resistance is almost inversely proportional to the channel width. In this embodiment, the channel width is smaller than that of a conventional trench IGBT and the channel resistance is increased. However, by use of the structure of this embodiment, the ON voltage of the n-type base layer 1 is reduced and the incremented part of the channel resistance is canceled out. As a result, although the input capacity of gates is low, a low ON voltage can be obtained.

[0027] In the OFF state, the withstand voltage is held by junction of the n-type base layer 1 and the p-type base layer 4. Since the trench insulating gates 7 are projected into the n-type base layer 1, the electric field intensity is high at the corner of the trench insulating gates 7. When Lb > La, the electric field intensity is high in the area Lb. When the withstand voltage of the element is higher, to ensure sufficient loss reduction and short-circuit withstand amount, it is valid to widen the area Lb. When the area Lb is widened so that the withstand voltage of the element is decided by the electric field intensity in the area Lb, the withstand voltage of the element is lowered. When the depth Lc from the bottom of the trench insulating gates 7 of the p-type well layer 9 is set like Lc $\geqq$ 0 and the distance Le between the trench insulating gates 7 and the p-type well layer 9 is adjusted, the electric field intensity in the area Lb can be lowered, so that the withstand voltage of the element will not be lowered.

[0028] In the load short-circuit state, the n-type channel MOSFET positioned in the area La is pinched off and a saturation current flows in the main electrode 10 and the main electrodes 11. The saturation current is almost proportional to the channel width. Since the channel width is smaller than that of a conventional trench IGBT, the saturation current is lower than that of a conventional trench insulating gate type IGBT.

[0029] According to this embodiment, the input capacity of gates can be reduced. Since the total area of the element of gate insulating film is small, the embodiment also has an advantage at the same time that the manufacturing yield of element is improved.

[0030] Here, for comparison of this embodiment with a conventional trench insulating gate type IGBT, the dependency on the characteristic interval ratio (Lb/La) is shown in Fig. 2. The values are indicated under the condition that the conventional trench insulating gate IGBT is standardized to 1. In the drawing, the dependency of the ON voltage (Von), gate input capacity (Cin), saturation current (Icsat), and element withstand voltage (VBCEO, VBCEO2) on the interval ratio of this embodiment is shown. The element withstand voltage VBCEO2 is, as shown in Fig. 1, the one when the p-type well layer 9 is formed in the area Lb and the element withstand voltage VBCEO is the one when the p-type well layer 9 is not formed and the p-type base layer is formed continuously. The examination of the inventors of the present invention shows that the ON voltage, gate input capacity, and saturation current have the dependency on the interval ratio (Lb/La) as shown in Fig. 2 regardless of the existence of the p-type well layer.

[0031] The examination of the inventors of the present invention shows that when La $\leqq$ 5 μm is satisfied, the trend characteristic shown in Fig. 2 is obtained. When Lb/La > 1, as Lb/La increases, the input capacity Cin and the saturation current Icsat decrease and when Lb/La = 12, they are almost minimized. Namely, when Lb/La> 1, the high-speed switching performance of the trench insulating gate type IGBT and the short-circuit withstand amount are improved. Furthermore, when 12 > Lb/La > 1, the original property of the trench insulating gate type which is the low ON resistance is not impaired but rather improved, so that the input capacity Cin and the saturation current Icsat decrease. Furthermore, when 6 $\geqq$ Lb/La $\geqq$ 2 is set, the ON voltage is minimized.

[0032] As shown in Fig. 2, when the p-type well layer 9 is not formed in the IGBT shown in Fig. 1 and Lb/La is increased, the element withstand voltage VBCEO is lowered. However, if such reduction in the element withstand voltage VBCEO produces no practical effect, even if the p-type well layer 9 is not formed, the aforementioned effect of increasing Lb/La can be produced. On the other hand, as shown by VBCEO2 in the drawing, when the p-type well layer 9 is formed, even if Lb/La is increased, the element withstand voltage changes little. Therefore, the aforementioned reduction in the ON voltage by Lb/La is more valid.

[0033] Generally, in a power converter such as an invertor, for a power short-circuit when an accident occurs, by interrupting the current by the IGBT, excessive destruction of the invertor is prevented. To realize it, it is desired that the IGBT withstands for more than 10 microseconds in the short-circuit state independently of the capacity of the invertor, power source, and voltage. The examination of the inventors of the present invention shows that in the IGBT of this embodiment, to realize more than 10 microseconds, it is desirable to control the saturation current density to 1000 A/cm^2 or less. For example, in an element having a withstand voltage of 600 V, when La = 3.2 μm and Lb = 23.2 μm, the ON voltage is lower than that of a conventional trench insulating gate IGBT, and the gate input capacity is reduced such as 1/3 times, and the saturation current is set to 1000 A/cm^2.

[0034] In an element having a withstand voltage of 1200 V, Lb is made wider such as 31.8 μm. The saturation current is set to 750 A/cm^2. Therefore, to ensure the short-circuit withstand amount for the two elements, it is not necessary to integrate an IC for limiting the maximum current in the IGBT chip and add it to the outside. As a result, there is an advantage that compared with a conventional trench insulating gate IGBT, the manufacturing cost can be reduced.

[0035] As mentioned above, by use of the structure of this embodiment that trench insulating gates are arranged at different intervals, and channels are formed in the wider trench mutual intervals, and the p-type well layer is formed in the wider trench mutual intervals, an insulating gate type bipolar transistor that the reduction in the element withstand voltage is not accompanied, and the gate input capacity is reduced compared with that of a conventional IGBT that trench insulating gates are arranged at equal intervals, and the switching loss is reduced, and the saturation current is lower than that of a conventional trench insulating gate type IGBT at the low ON voltage equivalent to that of the trench insulating gate type IGBT can be realized. Namely, an element having the structure of this embodiment is not accompanied by a reduction in the element withstand voltage and has a small loss even in the high frequency area.

[0036] Fig. 3 shows the second embodiment of the present invention and the basic constitution thereof is the same as that of the first embodiment. According to this embodiment, between the p-type base layer 4 and the n-type base layer 1 positioned in the area La, the n-type semiconductor layer 8 whose impurity density is higher than that of the n-type base layer 1 is installed. To form the uniform n-type semiconductor layer 8 under the p-type base layer 4, a part of the n-type semiconductor layer 8 may be extended into the area Lb or extended under the bottom of the trench insulating gates 7.

[0037] Holes injected into the n-type base layer 1 from the p-type collector layer 2 are ejected from the n-type source layer 5 in the area La. By the n-type semiconductor layer 8 in the hole movement path, the holes are limited to movement to the p-type base layer 4 and accumulated in the n-type base layer 1 in the neighborhood of the n-type semiconductor layer 8 and hence the conductivity modulation is promoted. As a result, the reduction in the ON voltage is realized. In the turn OFF state, a high voltage is applied to the main electrodes 11 and the n-type semiconductor layer 8 is depleted, so that it causes no obstacles to passing of holes and the turn-off loss is not increased.

[0038] The element withstand voltage depends on the impurity density in the n-type semiconductor layer 8. The reason is that the electric field intensity in the neighborhood of the junction of the p-type base layer 4 and the n-type semiconductor layer 8 depends on the impurity density in the n-type semiconductor layer 8. The examination of the inventors of the present invention shows that as the impurity density in the n-type semiconductor layer 8 increases, the ON voltage lowers. However, when it exceeds $1 \times 10^{12}/cm^2$, the element withstand voltage reduces greatly. Therefore, it is desirable to control the carrier density in the n-type semiconductor layer 8 to $1 \times 10^{12}/cm^2$ or less.

[0039] Fig. 4 shows the third embodiment of the present invention and the basic constitution thereof is the same as that of the first embodiment. According to this embodiment, a Zener diode D1 is connected between the p-type well layer 9 and the main electrode 10.

[0040] According to this embodiment, by installing a Zener diode D1 between the p-type base layer 4 and the main electrode 10, the upper limit of the potential between the trench insulating gates 7 and the p-type base layer 4 positioned in the area Lb can be set and generation of an electrostatic concentration exceeding the withstand voltage of the insulating film 71 can be prevented. During turn-off, holes in the n-type base layer 4 pass the p-type well layer 9 and flow into the main electrode 10. Therefore, holes in the n-type base layer 4 can be reduced and the turn-off loss can be reduced. Furthermore, since holes ejected from the n-type source layer 4 in the area La can be reduced, latch-up can be prevented.

[0041] Fig. 5 shows the fourth embodiment of the present invention and is a plan view of the cell and cell end of the trench insulating gate type IGBT relating to the first embodiment of the present invention. Figs. 6 and 7 are cross sectional views of A-A' and B-B' shown in Fig. 5 respectively.

[0042] In the direction of the channel width (see Fig. 7) of the trench insulating gates 7, the p-type well layer 91 is formed at a distance of Lp from the p-type base layer 4 so as to touch the end of the trench insulating gates 7 and be separated from the p-type base layer 4. The distance Lp is preset to a distance which the p-type base layer 4 and the p-type well layer 91 punch through in the voltage inhibition state of the IGBT. In the direction of the channel length (see Fig. 6) of the trench insulating gates 7, the p-type well layer 91 is formed at a distance of Lp from the p-type base layer 9 so as to be separated from the p-type well layer 9 in contact with the p-type base layer 4 in the outermost periphery. The distance Lp is preset to a distance which the p-type well layer 9 and the p-type well layer 91 punch through in the voltage inhibition state of the IGBT. The p-type well layer 91 is electrically connected to the main electrode 10 via the electrode 66. To pull out holes during turn-off, the p-type well layer 9 in the outermost periphery may come in contact with the electrode 10 like the contact 67.

[0043] In this embodiment, in the state that a positive voltage is applied to the main electrodes 11 and a negative voltage is applied to the main electrode 10, the p-type base layer 4, the p-type well layer 9, and the p-type well layer 91 punch through and at the end of the p-type base layer 4, the electrostatic concentration is prevented and the withstand voltage reduction is prevented. According to this embodiment, the p-type base layer 4 positioned in the area Lb can be electrically insulated from the p-type well layer 91 without reducing the main withstand voltage, and holes accumulated in the p-type base layer 4 are not ejected outside the element, and the ON voltage is lowered.

[0044] Fig. 8 is a plan view of the fourth embodiment of the present invention and the basic constitution is the same as that of the first embodiment. The cross sectional views of A-A' and B-B' shown in Fig. 8 are those shown in Figs. 6 and 7 respectively.

[0045] The trench insulating gates 7 formed so as to be repeated alternately like the area La and the area Lb are arranged to intersect the trench insulating gates 7 indicated in the second embodiment. 100 to 20000 trench insulating gates in total or so are formed in an actual element. The p-type well layer 9 may not be formed in the area Lb.

[0046] According to this embodiment, the gate wire resistance can be reduced.

[0047] Therefore, the difference in the delay between a gate signal of the IGBT near to the gate electrode pad or gate input terminal and a gate signal of the IGBT far from it is made smaller, so that the uniformity of the switching operation in the element is improved. Therefore, the element destruction due to current concentration caused by an ununiform operation can be prevented.

[0048] As a deformation example of this embodiment, as shown in Fig. 9, trench insulating gate electrodes can be structured in the area 101 where the two narrow areas La intersect each other and furthermore, the gate resistance can be reduced.

[0049] Fig. 10 shows the sixth embodiment of the present invention and is a cross sectional view of an IGBT chip. The basic constitution is the same as that of the first embodiment. The plane shape of the trench insulating gates is formed in a mesh-shape as shown in Fig. 8. Numerals 231 and 232 indicate an emitter electrode member and a collector electrode member respectively. The emitter electrode member 231 and the collector electrode member 232 are in contact with the main electrodes 10 and 11 by pressure respectively. These electrode members, in this embodiment, use molybdenum Mo whose coefficient of heat expansion is close to that of a semiconductor layer as a material. Numeral 61 indicates gate wires, which are separated from the pressure portion and attached with the conductive metal wires 65 so as to form a resistor. Under the main electrode 10, the insulating film 161 is formed thicker or higher than the gate wires 61 and the insulating film around them. As a result, the top of the main electrode 10 is formed higher than the metal wires 65 on the gate wires 61 and the emitter electrode member 231 is not in contact with the metal wires 65 on the gate wires. Since the metal wires 65 for reducing the gate wire resistance are provided, the delay of a gate signal to be transferred to the IGBT can be suppressed. Therefore, the switching delay between the IGBT unit near to the gate pad and the IGBT far from the gate pad is reduced and the current concentration to the IGBT units and heat destruction by it can be prevented. In this embodiment, the trench insulating gates 7 are arranged so as to intersect each other. As indicated by this embodiment 1, the gate input capacity in this structure can be reduced and also the delay of a gate signal can be suppressed and by pressurizing the main electrodes 10 and 11, the emitter electrode and collector electrode can come into contact with each other.

[0050] Fig. 11 shows the seventh embodiment of the present invention and is a cross sectional view of an IGBT chip. The basic constitution is the same as that of the sixth embodiment. Under the insulating film 161, the p-type base layer 4 and the p-type well layer 9 are in contact with the trench insulating gate electrodes so as to be separated by an insulating film and the electrodes 171 connecting the insulating gates are formed in the area Lb. The electrodes 171 hold the main electrode 10 high and make the resistance of the gates lower. Although the gate input capacity increases, the difference between the gate input capacity and the feedback capacity does not increase, so that by use of this structure, the delay of a gate signal can be suppressed more. Therefore, by pressurizing the main electrodes 10 and 11, the emitter electrode and collector electrode can come into contact with each other.

[0051] Fig. 12 shows an example of a power converter using the trench insulating gate type IGBT of the present invention which is a circuit diagram showing an embodiment of a 3-phase invertor for driving an induction motor. Between the collector and the emitter of the IGBT, a diode having a reverse polarity for feeding back the load current is connected in parallel and between the gates and the emitter, a gate driver is connected. The two IGBTs connected in series are connected in parallel for three phases respectively. By using the IGBTs of the present invention, the input capacity is reduced, so that the output capacity of the gate driver can be lowered and the gate driver can be miniaturized and lightened. Since the saturation current is equivalent to that of a conventional planar IGBT, there is no need to add a current limit circuit and an invertor circuit which is simple and reliable and causes little loss can be realized.

[0052] Fig. 13 shows the eighth embodiment of the present invention and is a plan view of the cell and cell end of a trench insulating gate type IGBT. Fig. 14 is a cross sectional view of A-A' shown in Fig. 13.

[0053] The basic constitution is the same as that of the fourth embodiment. However, though the p-type well layer 9 positioned in the outermost periphery is not provided in the direction of the channel width of the trench insulating gates 7, the p-type base layer 4 and the p-type well layer 91 are overlaid and in contact with each other. The p-type base layer 4 and the p-type well layer 91 are in contact with the main electrode 10 like the contact 67.

[0054] It is desirable to form the p-type well layer 9 and the p-type well layer 91 as a same layer in the same process. The reason is that the production cost can be reduced.

[0055] Fig. 15 shows the ninth embodiment of the present invention and the basic constitution is the same as that of the first embodiment. In this embodiment, an M1 source electrode which is a p-type MOS is electrically connected to the p-type well layer 9 and a drain electrode is electrically connected to the main electrode 10. An M1 gate electrode is electrically connected to the trench insulating gates 7.

[0056] When the IGBT is turned off, a negative or 0 potential is applied to the trench insulating gates 7.

[0057] When the trench insulating gates 7 of the IGBT are turned off by applying a negative potential, M1 may be any one of the enhancement type and the depression type, though when they are turned off by applying a 0 potential, it is necessary to use M1 of the depression type. In either case, when the IGBT is turned on, M1 is turned off and when the IGBT is turned off, M1 is turned on.

[0058] When the IGBT is turned off, holes accumulated in the p-type well layer 9 and the p-type base layer 4 pass M1. As a result, holes can be quickly ejected from the element, so that the turn-off loss is reduced. As a result, the potential of the p-type base layer 4 is not increased and the insulation destruction of the gate oxidized film of the trench insulating gates 7 can be prevented. When the IGBT is turned on, M1 is turned off, so that holes do not flow out of the element from M1.

[0059] Fig. 16 shows the ninth embodiment of the present invention and is a solid perspective view. Although the basic constitution is the same as that shown in Fig. 1, the p-type well layer 9 is not formed in the area Lb and the p-type base layer 4 is formed continuously. Along the longitudinal direction of the trench insulating gates 7, that is, the longitudinal direction of the area La, the n-type source layer 5 is divided into a plurality of areas. Between neighboring areas, a part of the p-type base layer 4 is positioned. Namely, the n-type source layer 5 is formed intermittently. Almost at the center in the width direction of the area La, a groove which is a contact hole 201 is formed in the longitudinal direction so deep as to pass the n-type source layer 5. The area La is divided into two areas by this groove. In these two areas, the n-type source layer 5 is formed respectively in the same way. Although not shown in the drawing, the main electrode 10 (source electrode) is electrically connected to the n-type source layer 5 and the p-type base layer 4 in the same way as with Fig. 1. Furthermore, in this embodiment, even in the contact hole 201, the main electrode 10 (source electrode) is electrically connected to the n-type source layer 5 and the p-type base layer 4. At the bottom of the contact hole 201, the p+ layer 6 whose impurity density is higher than that of the p-type base layer 4 is formed and the p-type base layer 4 is electrically connected to the main electrode via the p+ layer 6.

[0060] In this embodiment, Lb/La is set in the same way as with the embodiment shown in Fig. 1 and the operation and effect previously described by referring to Fig. 2 are produced. Furthermore, in the area La, the n-type source layer 5 is formed intermittently, so that the saturation current Icsat is reduced. Namely, the short-circuit withstand amount is improved. Therefore, as shown in Fig. 2, within the range of 6 > Lb/La > 2 when the ON voltage Von is minimized, Icsat is reduced in the same way as with a case that Lb/La is increased (for example, Lb/La = 12). Therefore the trench insulating gate type IGBT of this embodiment, within the range that the effect of Lb/La on the element withstand voltage is comparatively small, has both low ON voltage and high short-circuit withstand amount. In this embodiment, the p-type base layer 4 is electrically connected to the main electrode at the bottom of the contact hole 201, so that when the IGBT is turned off, the hole current is ejected to the main electrode 10 without almost passing in the neighborhood of the n-type source layer 5. Therefore, the latch-up phenomenon at the time of turn-off is hardly generated.

[0061] According to the present invention, a high performance trench insulating gate type IGBT can be realized.

Claims

1. An insulated gate bipolar transistor comprising:

a first semiconductor layer (2) of a first conductive type,
a second semiconductor layer (1) of a second conductive type neighbouring to said first semiconductor layer,
a third semiconductor layer (4) of said first conductive type neighbouring to said second semiconductor layer,
a plurality of insulated gates (7) passing through said third semiconductor layer and reaching said second semiconductor layer,
a first area and a second area which are areas between said neighbouring insulated gates (7) and neighbouring to each other,
a fourth semiconductor layer (5) of said second conductive type in contact with said insulated gates (7) in said third semiconductor layer (4) in said first area,
a first main electrode (10) electrically connected to said third semiconductor layer (4) and said fourth semiconductor layer (5) in said first area, and
a second main electrode (11) electrically connected to said first semiconductor layer (2) **characterized in that**:

assuming an interval between said neighbouring insulated gates (7) in said first area as La and an interval between said neighbouring insulated gates in said second area as Lb, La $\leqq$ 5 μm and Lb/La > 1; and
a fifth semiconductor layer (9) of said first conductive type either

(i) deeper than said third semiconductor layer (4) or
(ii) deeper than the bottom of said insulated gates (7)

is installed in said second area, and said first main electrode (10) is insulated from said fifth semiconductor layer (9) by an insulating film.

2. An insulated gate bipolar transistor according to claim 1, wherein 6 ≧ Lb/La ≧ 2.

3. An insulated gate bipolar transistor according to claim 1 or 2, wherein said third semiconductor layer in said second area and said first electrode are insulated by an insulating film.

4. An insulated gate bipolar transistor according to claim 3, wherein said third semiconductor layer in said first area and said third semiconductor layer in said second area are separated from each other.

5. An insulated gate bipolar transistor according to claim 1, wherein said third semiconductor layer and fifth semiconductor layer in said second area and said first electrode are insulated by an insulating film.

6. An insulated gate bipolar transistor according to claim 5, wherein said third semiconductor layer in said first area and said third semiconductor layer in said second area are separated from each other.

7. An insulated gate bipolar transistor according to claim 1, wherein a Zener diode is connected between said fifth semiconductor layer and said first main electrode.

8. An insulated gate bipolar transistor according to claim 1, wherein said second semiconductor layer in said first area has a first portion of said first semiconductor layer and a second portion of said third semiconductor layer whose impurity density is higher than that of said first portion.

9. An insulated gate bipolar transistor according to claim 1, wherein a Zener diode is connected between said third semiconductor layer in said second area and said first main electrode.

10. An insulated gate bipolar transistor according to claim 8 or claim 9, wherein said third semiconductor layer in said second area and said first electrode are insulated by an insulating film.

Patentansprüche

1. Bipolartransistor mit isoliertem Gate mit:

einer ersten Halbleiterschicht (2) eines ersten Leitfähigkeitstyps,
einer zweiten Halbleiterschicht (1) eines zweiten Leitfähigkeitstyps, die zur ersten Halbleiterschicht benachbart ist,
einer dritten Halbleiterschicht (4) des ersten Leitfähigkeitstyps, die zur zweiten Halbleiterschicht benachbart ist,
mehreren isolierten Gates (7), die durch die dritte Halbleiterschicht hindurch die zweite Halbleiterschicht erreichen,
einem ersten und einem zweiten Bereich, die Bereiche zwischen den benachbarten isolierten Gates (7) sind und die zueinander benachbart sind,
einer vierten Halbleiterschicht (5) des zweiten Leitfähigkeitstyps in Kontakt mit den isolierten Gates (7) in der dritten Halbleiterschicht (4) im ersten Bereich,
einer ersten Hauptelektrode (10), die elektrisch mit der dritten Halbleiterschicht (4) und der vierten Halbleiterschicht (5) im ersten Bereich verbunden ist, und
einer zweiten Hauptelektrode (11), die elektrisch mit der ersten Halbleiterschicht (2) verbunden ist,
dadurch gekennzeichnet, dass
unter der Annahme eines Abstands La zwischen den benachbarten isolierten Gates (7) im ersten Bereich und eines Abstands Lb zwischen den benachbarten isolierten Gates im zweiten Bereich, La ≦ 5μm und Lb/La > 1 gilt; und
eine fünfte Halbleiterschicht (9) des ersten Leitfähigkeitstyps entweder

(i) tiefer als die dritte Halbleiterschicht (4) oder
(ii) tiefer als die Unterseite der isolierten Gates (7)

im zweiten Bereich installiert ist und die erste Hauptelektrode (10) von der fünften Halbleiterschicht (9) durch einen Isolierfilm isoliert ist.

2. Bipolartransistor mit isoliertem Gate nach Anspruch 1, wobei 6 ≥ Lb/La ≥ 2 gilt.

3. Bipolartransistor mit isoliertem Gate nach Anspruch 1 oder 2, wobei die dritte Halbleiterschicht im zweiten Bereich und die erste Elektrode durch einen Isolierfilm isoliert sind.

4. Bipolartransistor mit isoliertem Gate nach Anspruch 3, wobei die dritte Halbleiterschicht im ersten Bereich und die dritte Halbleiterschicht im zweiten Bereich voneinander getrennt sind.

5. Bipolartransistor mit isoliertem Gate nach Anspruch 1, wobei die dritte Halbleiterschicht und die fünfte Halbleiterschicht im zweiten Bereich von der ersten Elektrode durch einen Isolierfilm isoliert sind.

6. Bipolartransistor mit isoliertem Gate nach Anspruch 5, wobei die dritte Halbleiterschicht im ersten Bereich und die dritte Halbleiterschicht im zweiten Bereich voneinander getrennt sind.

7. Bipolartransistor mit isoliertem Gate nach Anspruch 1, wobei eine Zenerdiode zwizchen der fünften Halbleiterschicht und der ersten Hauptelektrode angeschlossen ist.

8. Bipolartransistor mit isoliertem Gate nach Anspruch 1, wobei die zweite Halbleiterschicht im ersten Bereich einen ersten Abschnitt der ersten Halbleiterschicht und einen zweiten Abschnitt der dritten Halbleiterschicht hat, dessen Verunreinigungsdichte höher ist als die des ersten Abschnitts.

9. Bipolartransistor mit isoliertem Gate nach Anspruch 1, wobei eine Zenerdiode zwischen der dritten Halbleiterschicht im zweiten Bereich und der ersten Hauptelektrode angeschlossen ist.

10. Bipolartransistor mit isoliertem Gate nach Anspruch 8 oder 9, wobei die dritte Halbleiterschicht im zweiten Bereich und die erste Elektrode durch einen Isolierfilm isoliert sind.

Revendications

1. transistor bipolaire à porte isolée comportant :

une première couche semi-conductrice (2) d'un premier type de conductivité,
une deuxième couche semi-conductrice (1) d'un second type de conductivité proche de ladite première couche semi-conductrice,
une troisième couche serni-conduccrice (4) dudit premier type conducteur proche de ladite deuxième couche semi-conductrice,
une pluralité de portés isolées (7) traversant ladite troisième couche semi-conductrice et atteignant ladite deuxième couche semi-conductrice,
une première zone et une seconde zone qui sont des zones entre lesdites portes isolées voisines (7) et mutuellement proches,
une quatrième couche semi-conductrice (5) dudit second type de conductivité en contact avec lesdites portes isolées (7) dans ladite troisième couche semi-conductrice (4) de ladite première zone,
une première électrode principale (10) électriquement connectée à ladite troisième couche semi-conductrice (4) et à ladite quatrième couche semi- conductrice (5) dans ladite première zone, et
une seconde électrode principale (;lui) électriquement connectée à ladite première couche semi-conductrice (2), **caractérisé en ce que :**

en partant de l'hypothèse d'un intervalle entre lesdites portes isolées voisines (7) dans ladite première zone désigné en tant que La et d'un intervalle entre lesdites portes isolées voisines dans ladite seconde zone désigné en tant que Lb, La ≤ 5μm et Lb/La > 1, et
une cinquième couche semi-conductrice (9) dudit premier type de conductivité soit

(i) plus profonde que ladite troisième couche semi-conductrice (4) soit
(ii) plus profonde que la partie inférieure desdites partes isolées (7)

est installée dans ladite seconde zone, et ladite première électrode principale (10) est isolée de ladite cinquième couche semi-conductrice (9) par un film isolant.

2. Transistor bipolaire à porte isolée selon la revendication 1, dans lequel 6 ≥ Lb/La ≥ 2.

3. Transistor bipolaire à porte isolée selon la revendication 1 ou 2, dans lequel ladite troisième couche semi-conductrice dans ladite seconde zone et ladite première électrode sont isolées par un film isolant.

4. Transistor bipolaire à porte isolée selon la revendication 3, dans lequel ladite troisième couche semi-conductrice dans ladite première zone et ladite troisième couche semi-conductrice dans ladite seconde zone sont séparées l'une de l'autre.

5. Transistor dipolaire à porte isolée selon la revendication 1, dans lequel lesdites troisième couche semi-conductrice et cinquième couche semi-conductrice dans ladite seconde zone et ladite première électrode sont isolées par un film isolant.

6. Transistor bipolaire à, porte isolée selon la revendication 5, dans lequel ladite troisième couche semi-conductrice dans ladite première zone et ladite troisième couche semi-cosrduatrice dans ladite seconde zone sont séparées l'une de l'autre.

7. Transistor bipolaire à porte isolée selon la revendication 1, dans lequel une diode Zener est connectée entre ladite cinquième couche semi-conductrice et ladite première électrode principale.

8. Transistor bipolaire à porte isolée selon la revendication 1, dans lequel ladite deuxième couche semi-conductrice dans ladite première zone a une première partie de ladite première couche semi-conductrice

et une seconde partie de ladite troisième couche semi-conductrice dont la densité d'impuretés est supérieure à celle de ladite première partie.

9. Transistor bipolaire à porte isolée selon la revendication 1, dans lequel une diode Zener est connectée entre ladite troisième couche semi-conductrice dans ladite seconde zone et ladite première électrode principale.

10. Transistor bipolaire à porte isolée selon la revendication 8 ou la revendication 9, dans lequel ladite troisième couche semi-conductrice dans ladite seconde zone et ladite première électrode sont isolées par un film isolant.

FIG. 1

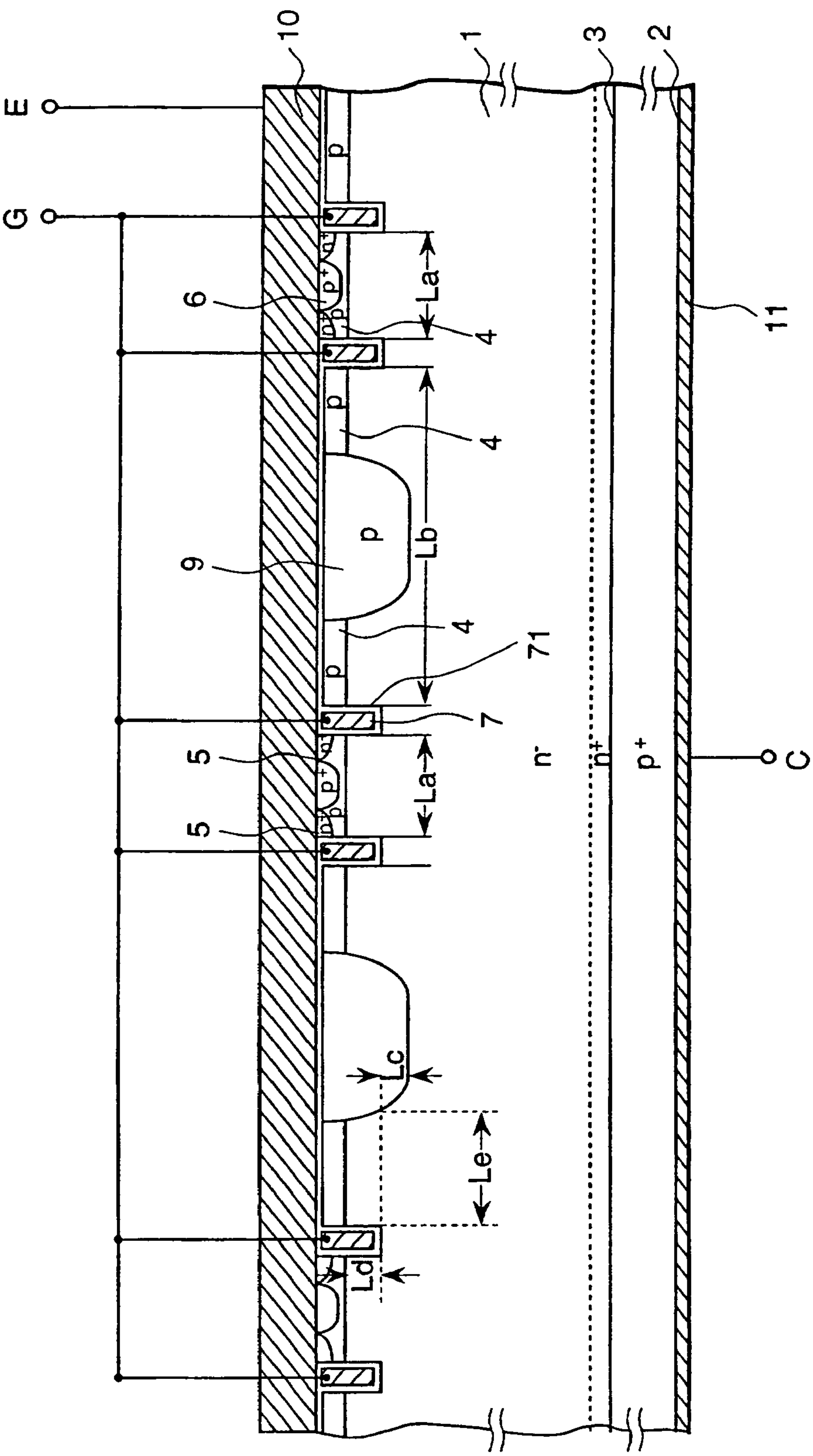


FIG. 2

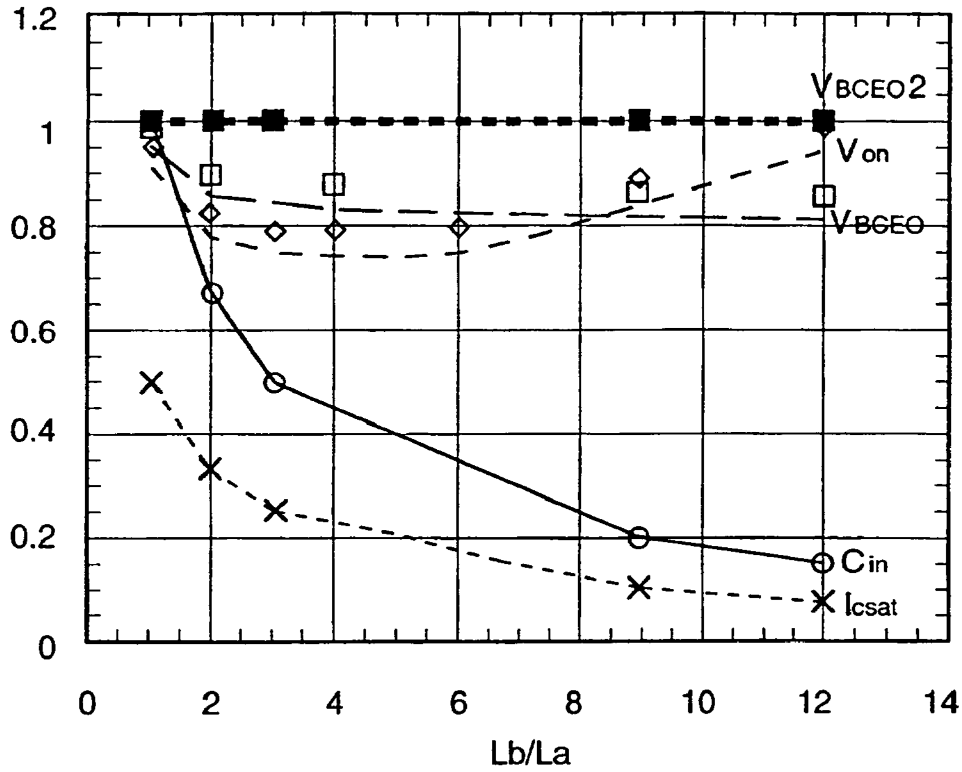


FIG. 3

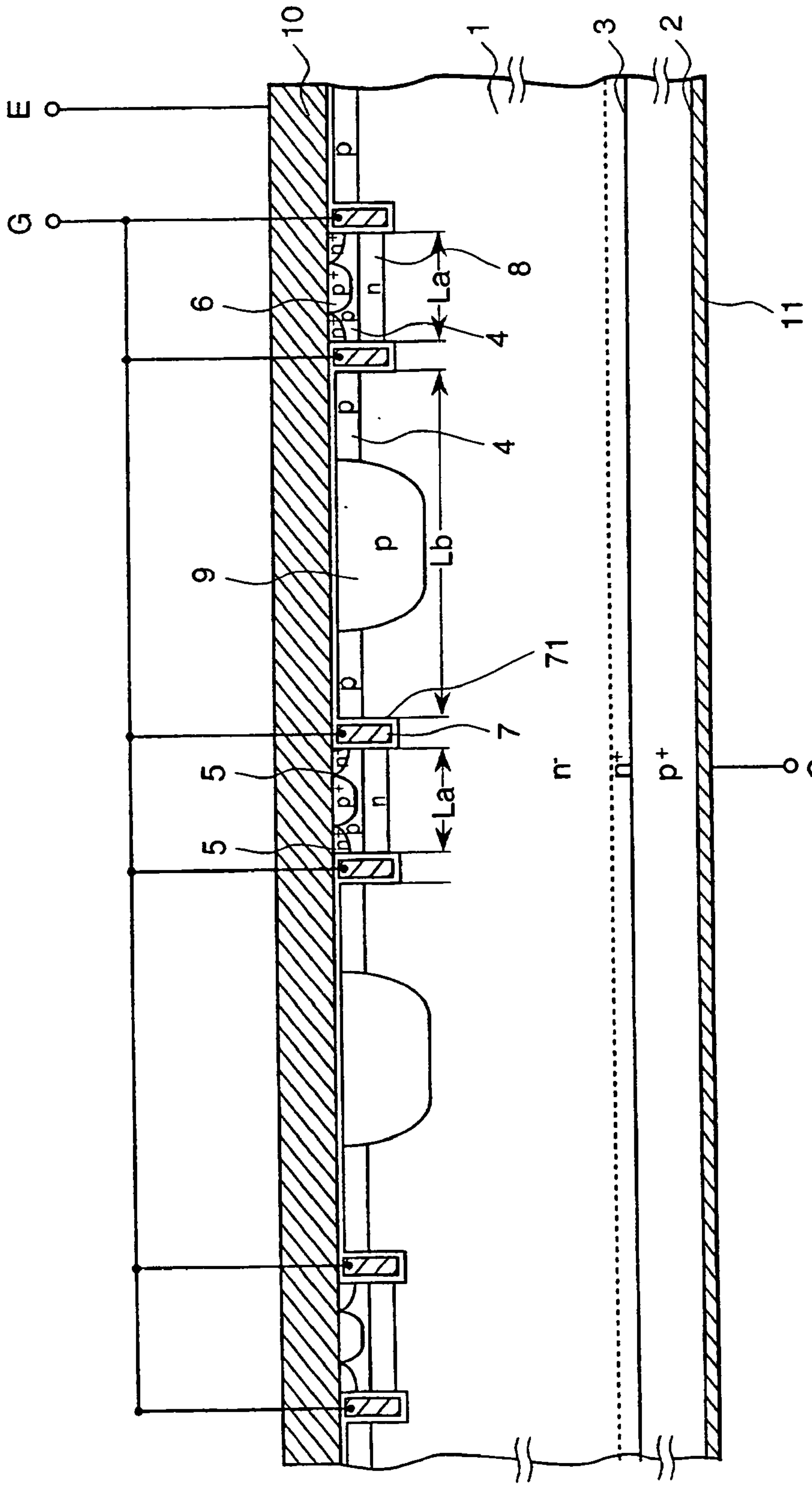


FIG. 4

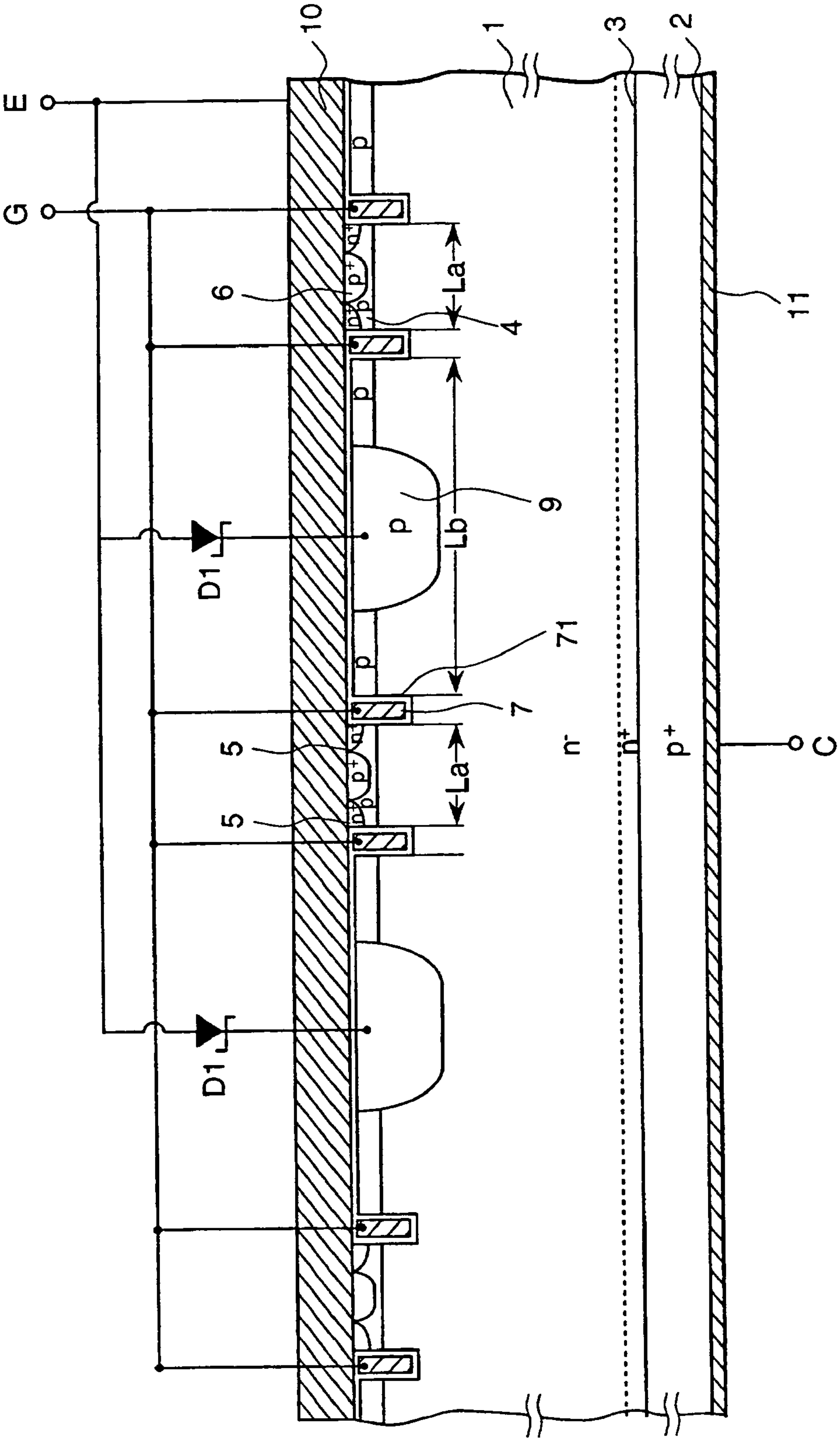


FIG. 5

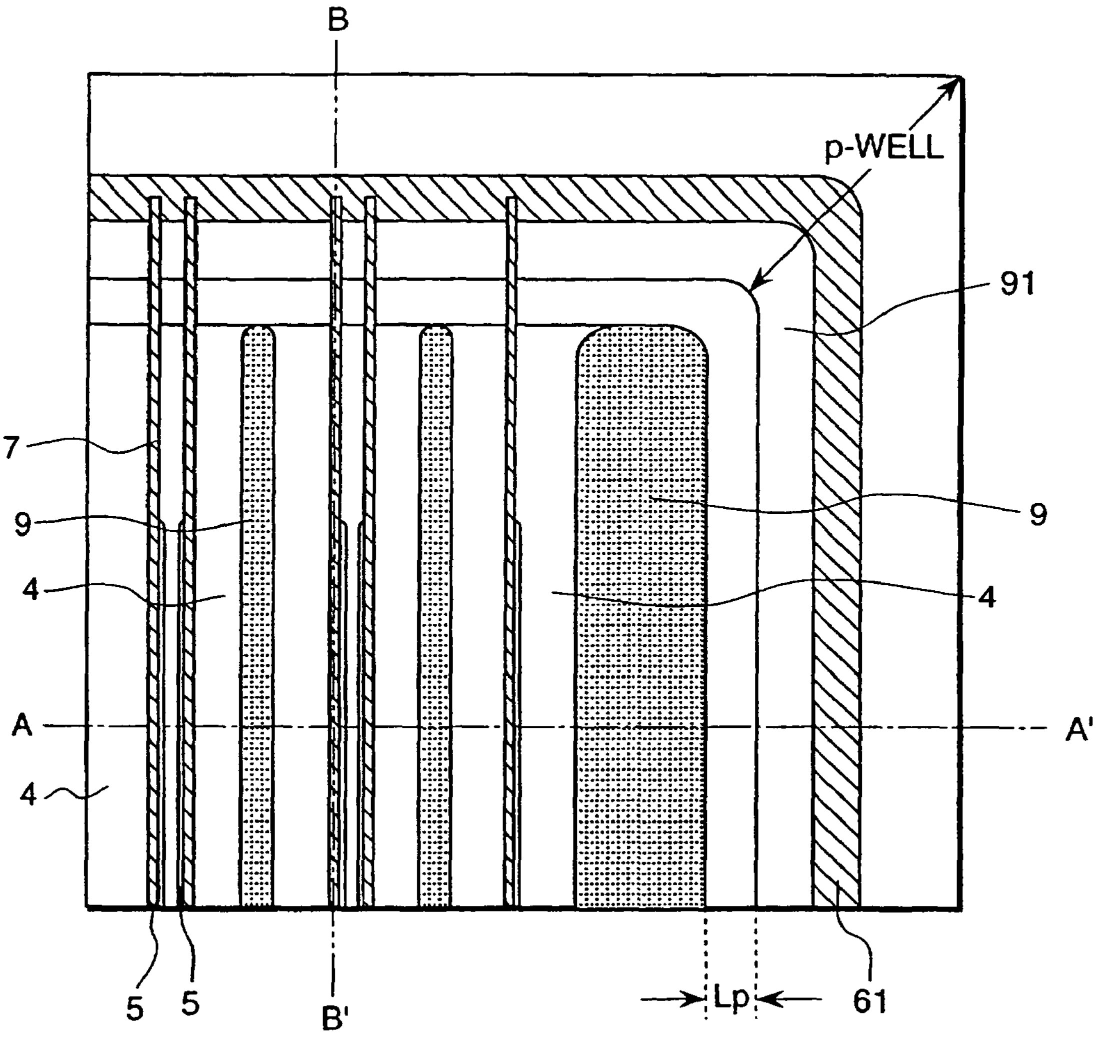


FIG. 6

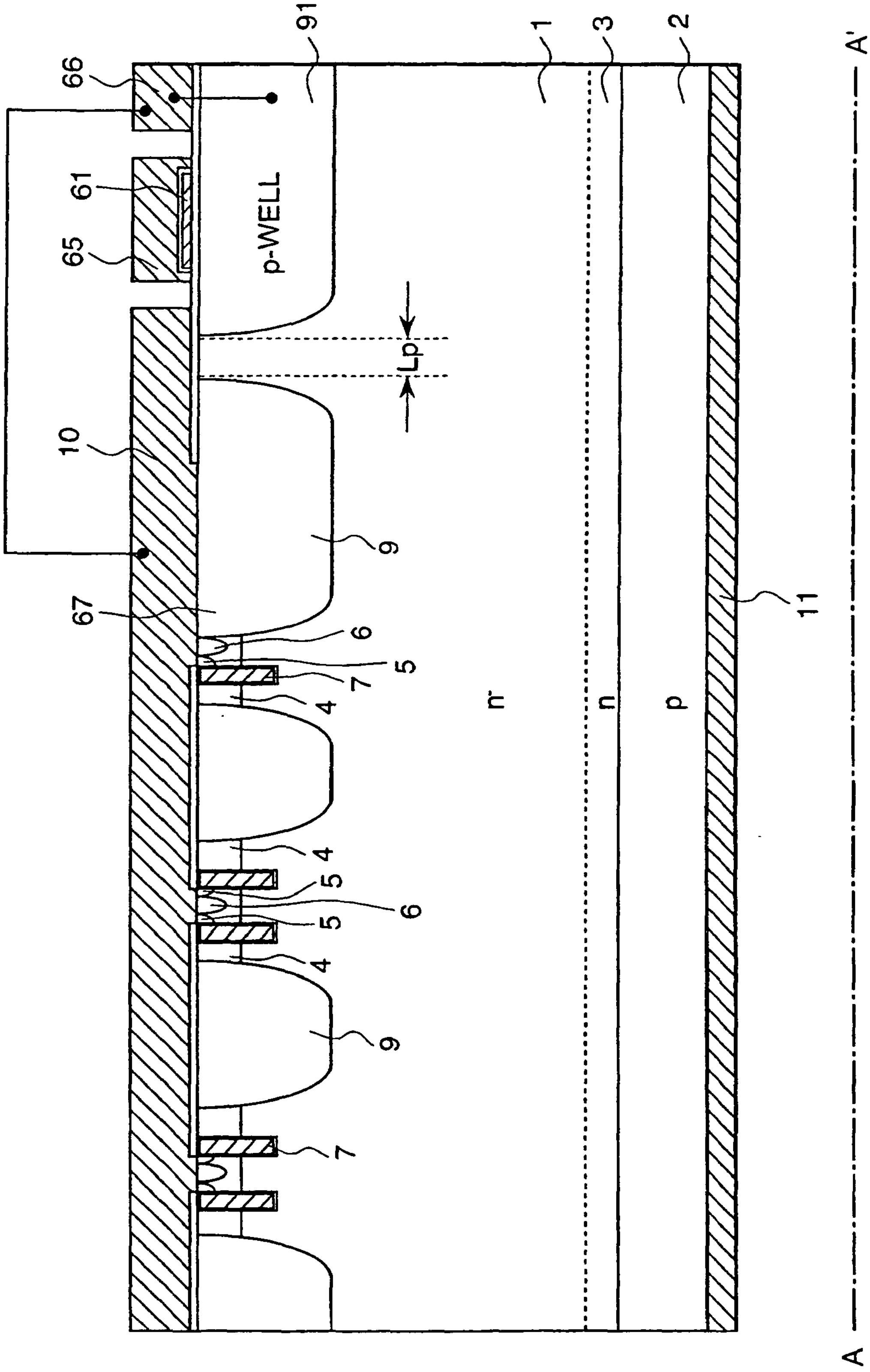


FIG. 7

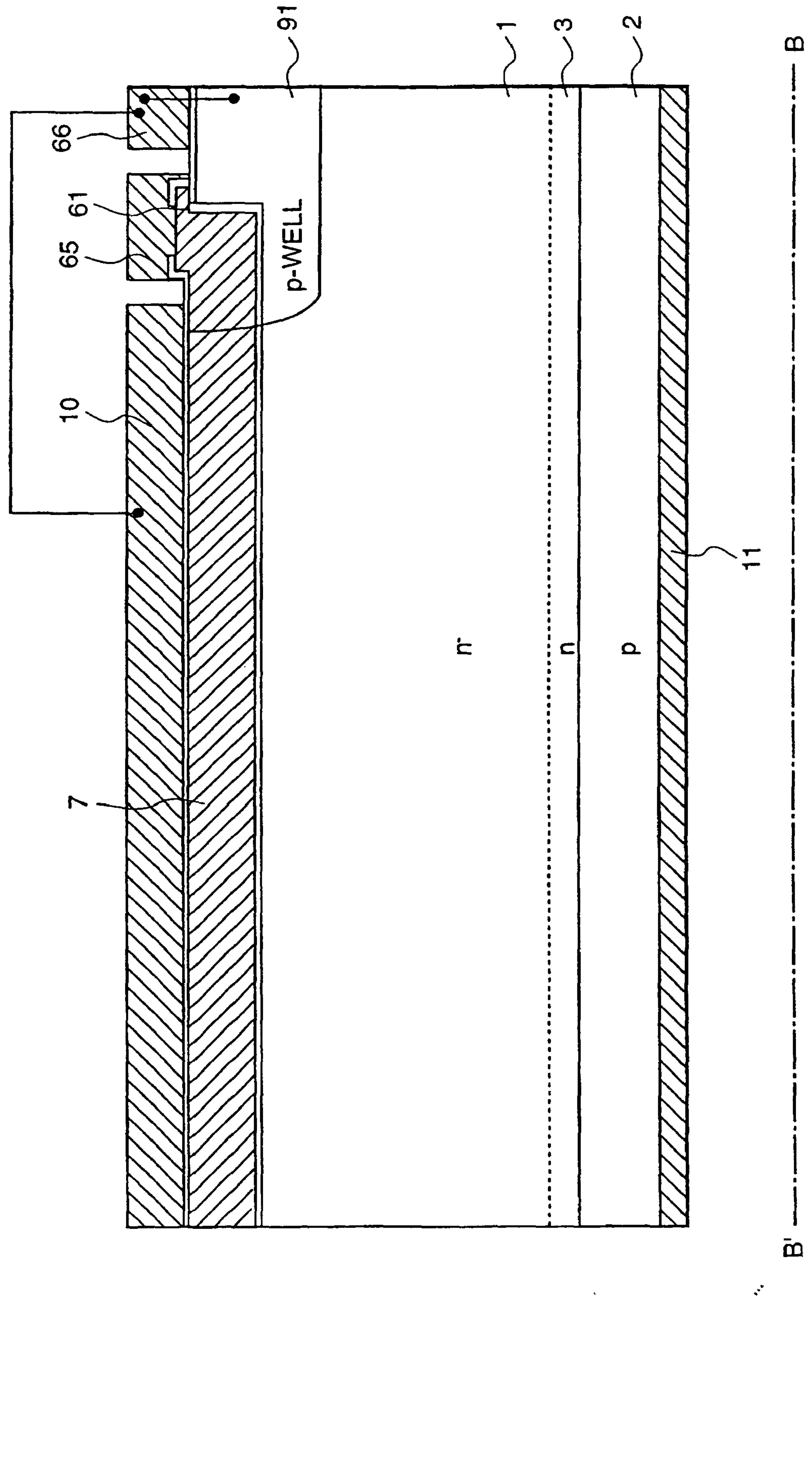


FIG. 8

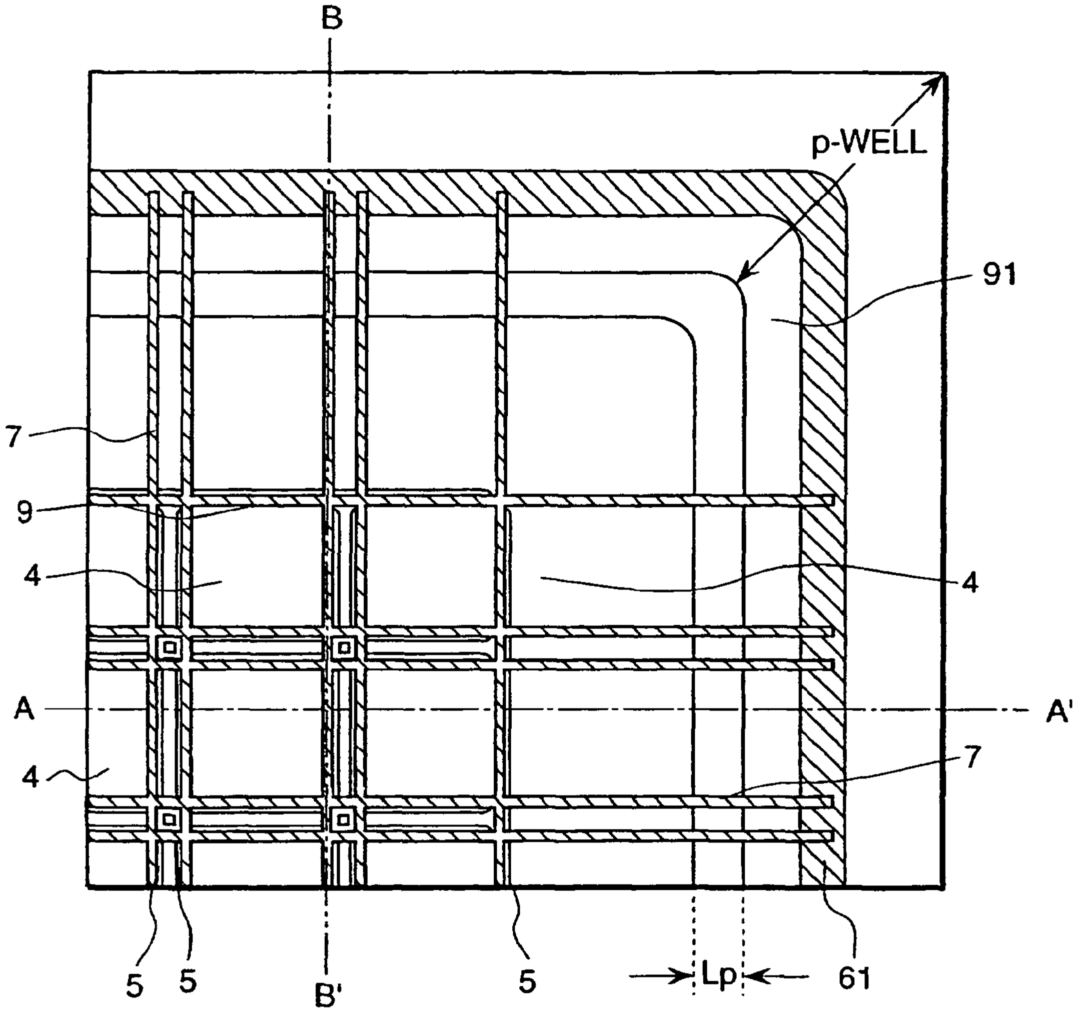


FIG. 9

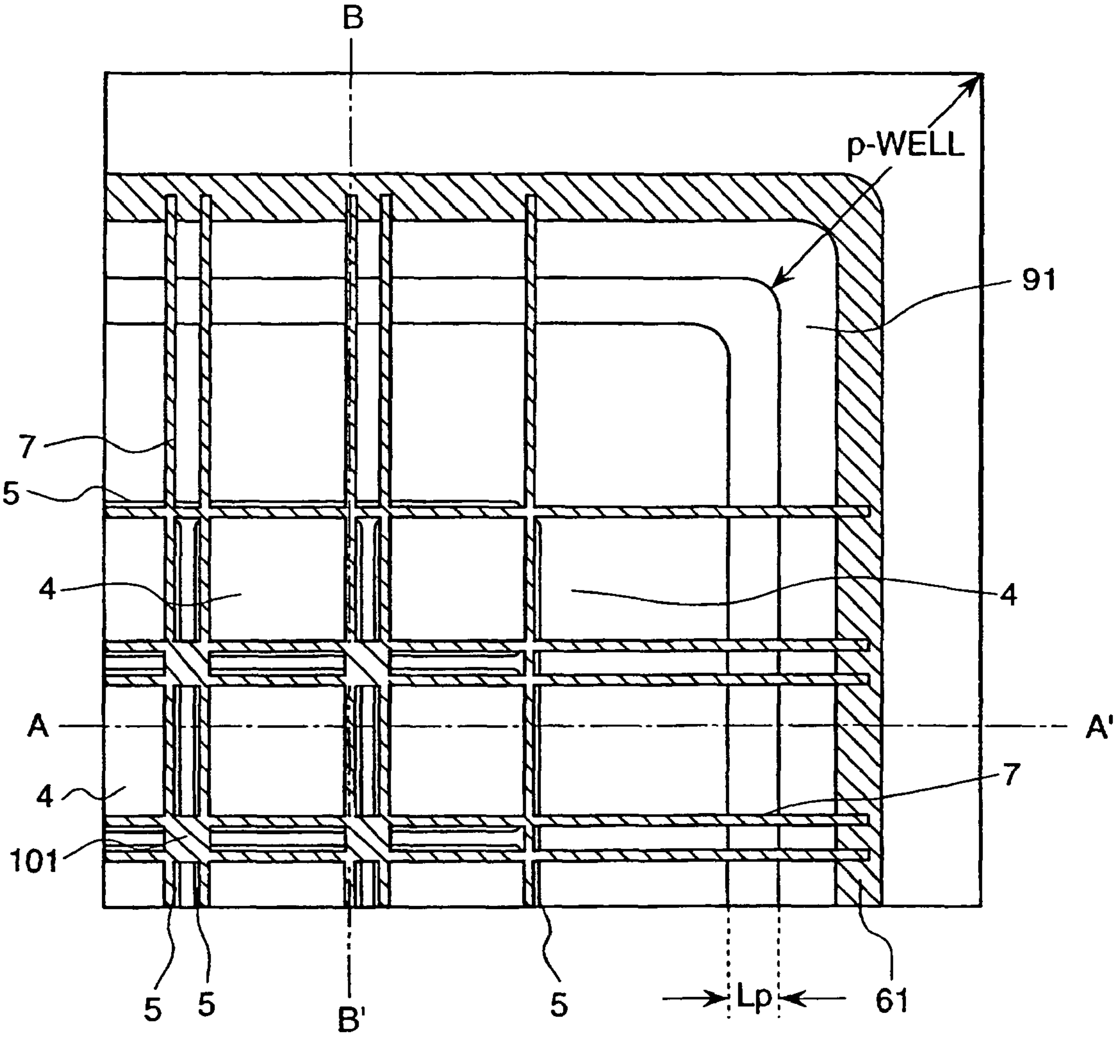


FIG. 10

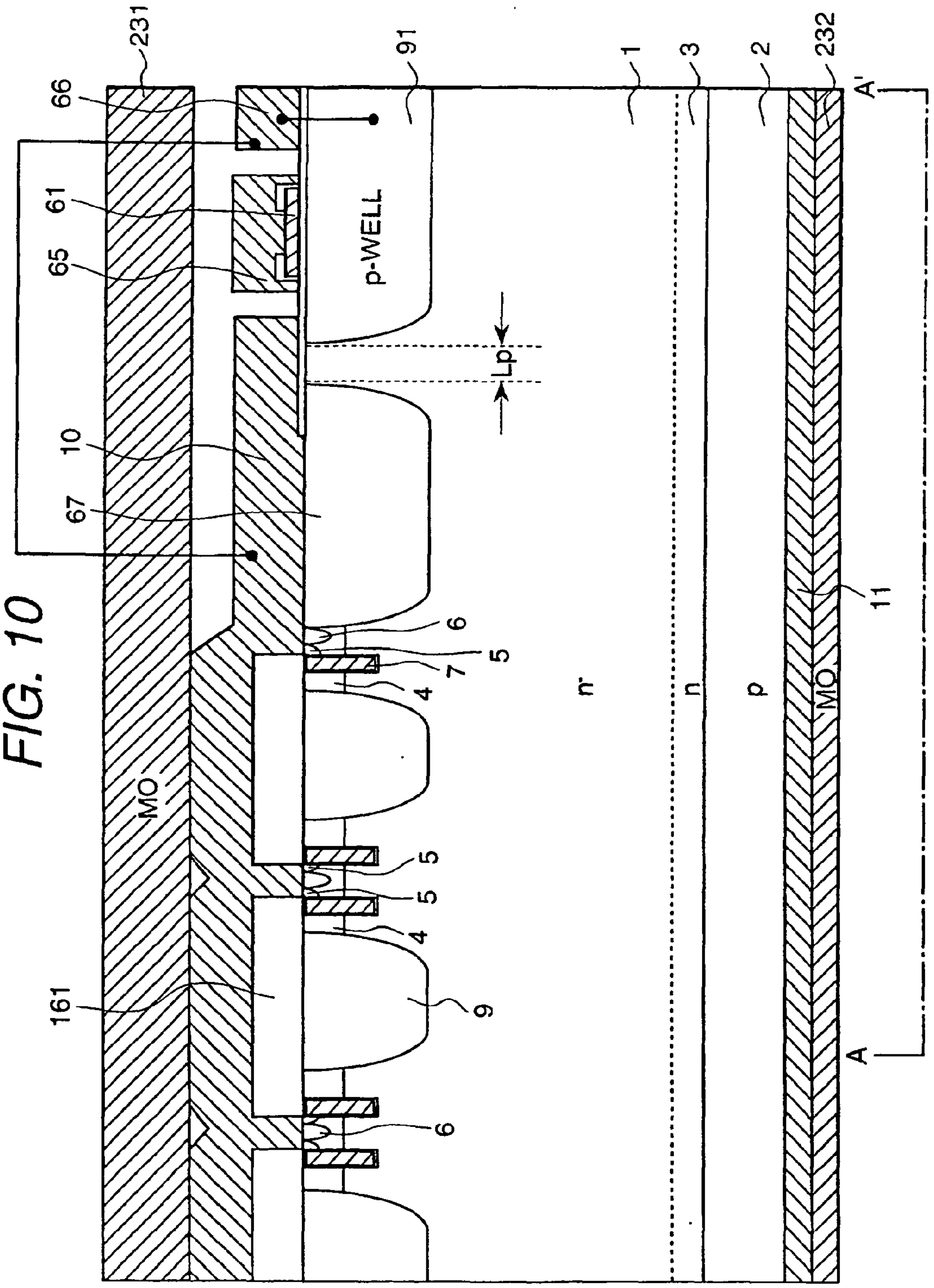


FIG. 11

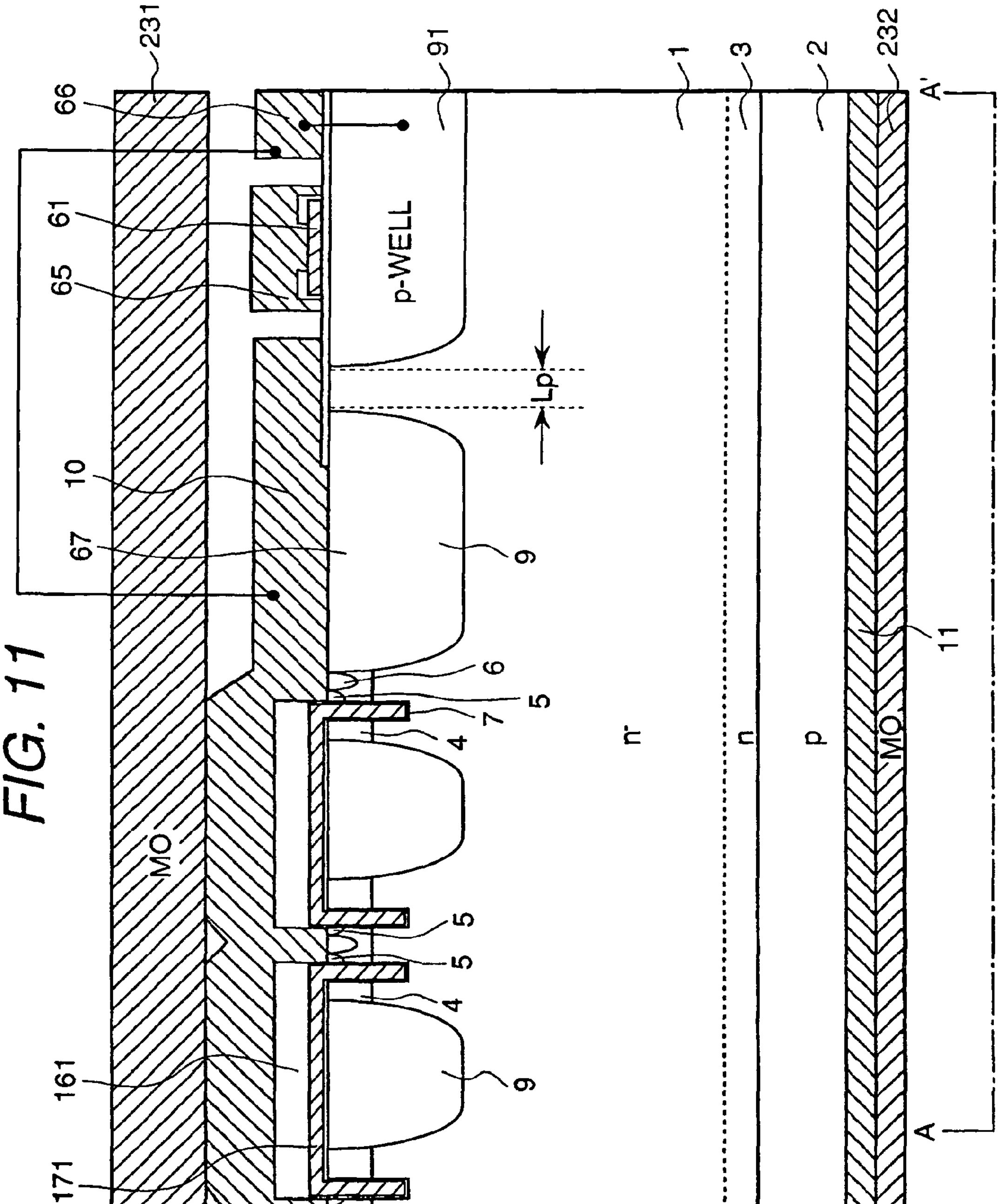


FIG. 12

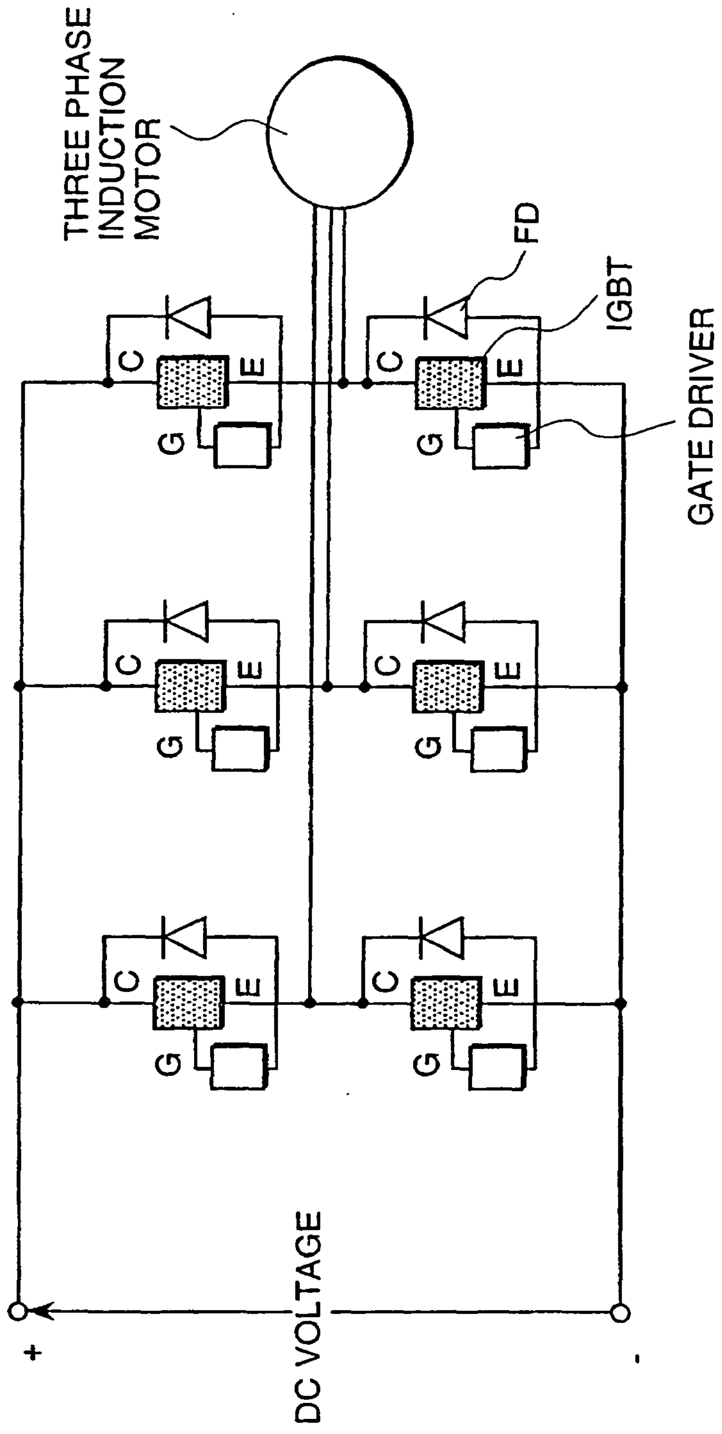

THREE PHASE
INDUCTION
MOTOR
FD
IGBT
GATE DRIVER
C
G
E
DC VOLTAGE
+
-

FIG. 13

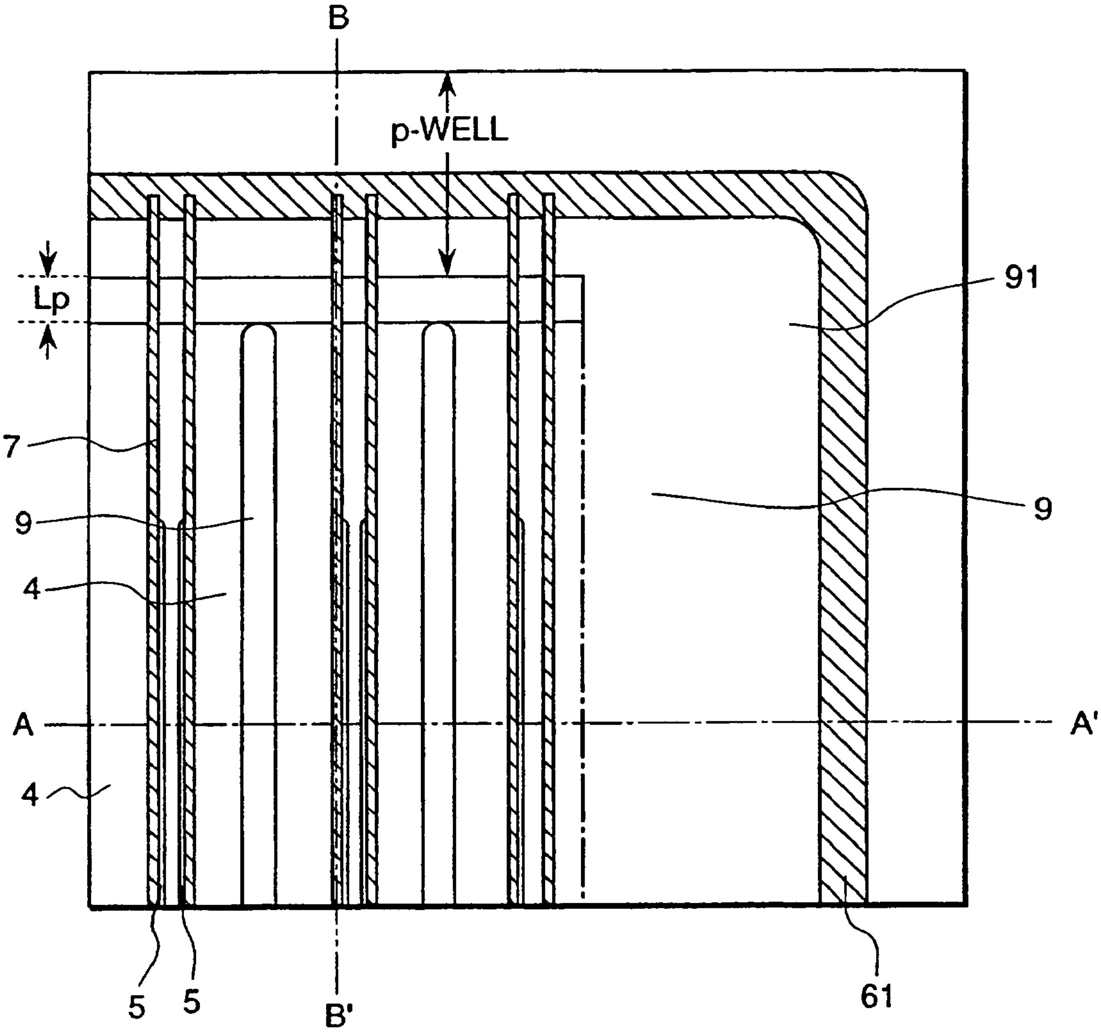
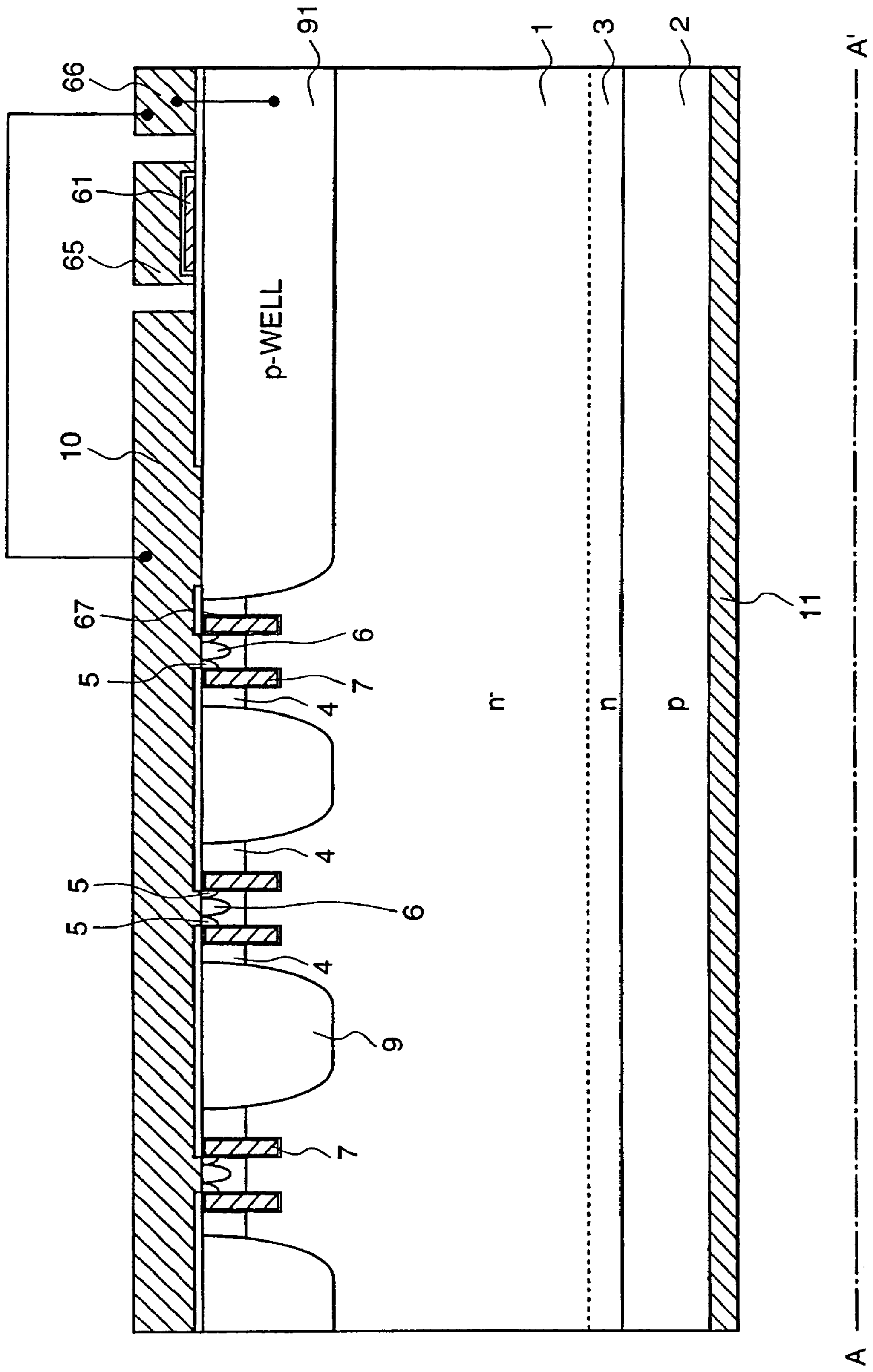


FIG. 14



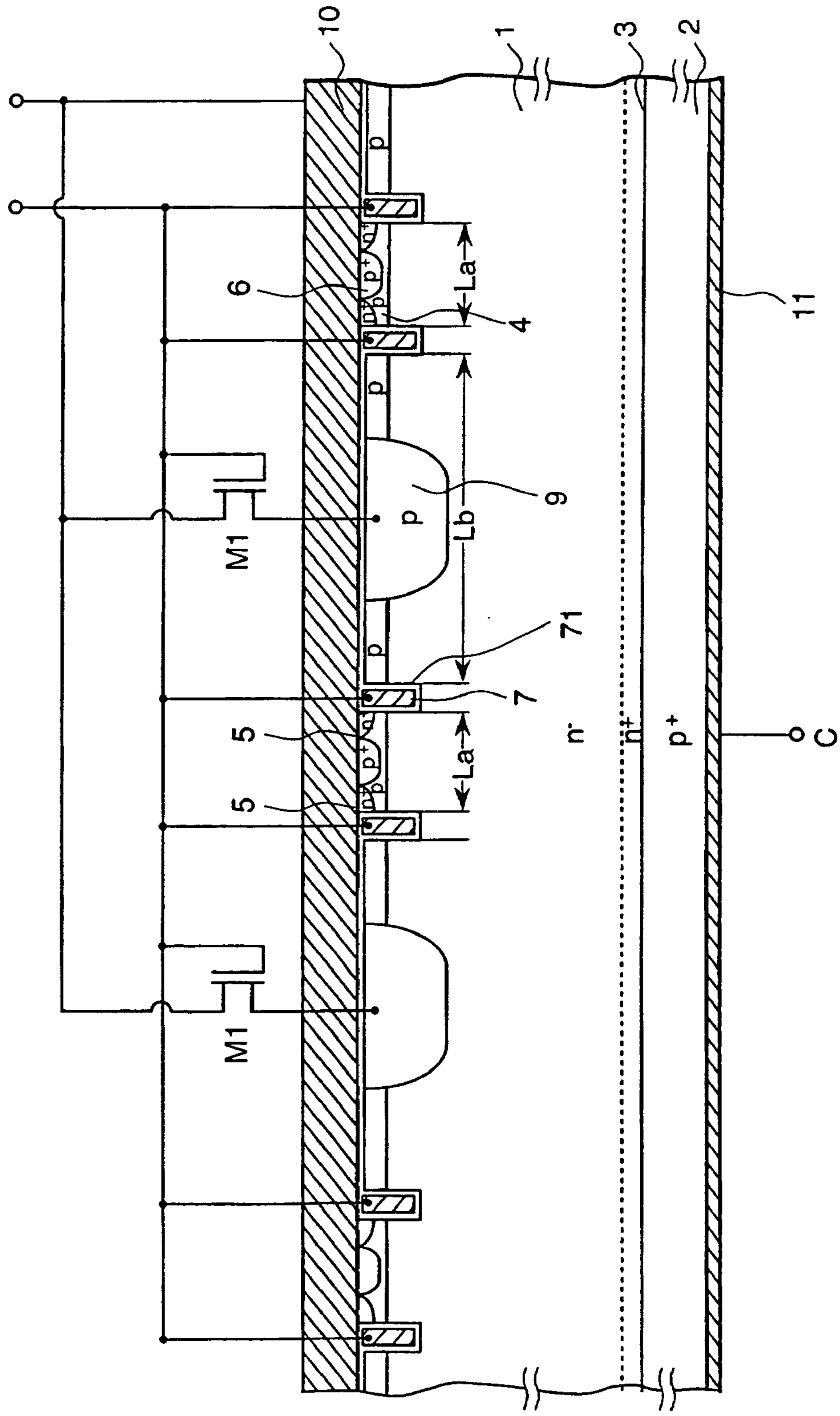
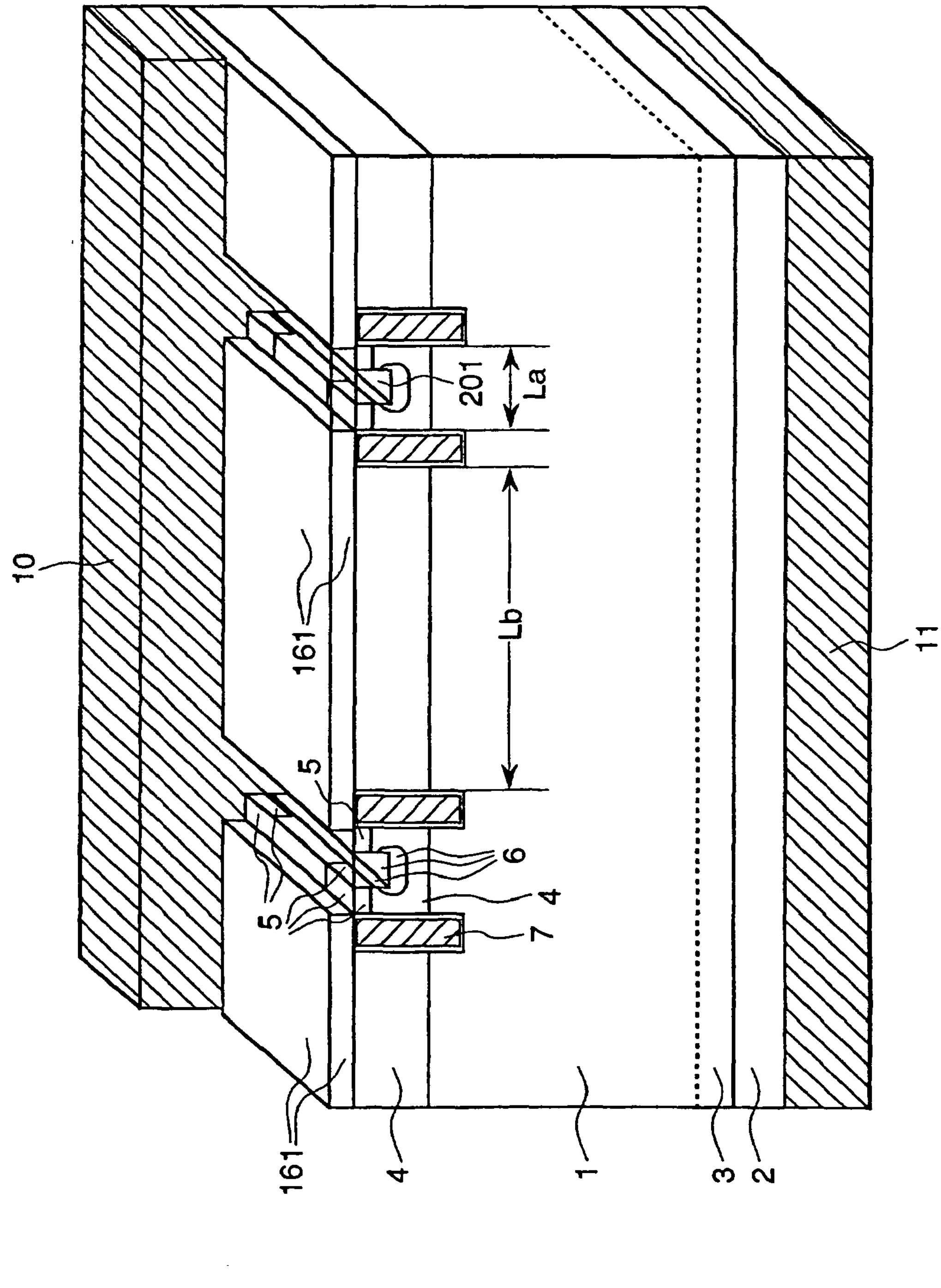


FIG. 15

FIG. 16



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 5243561 A **[0006]**
- JP 10178176 A **[0007]**
- EP 0746030 A **[0009]**