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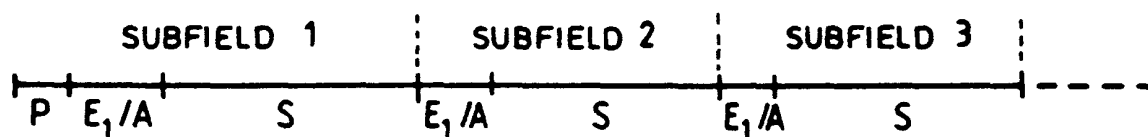
(54) **Method for controlling a plasma display panel and display apparatus using this method**

(57) The invention relates to a method for controlling a plasma display panel (PDP), wherein each field is divided into a plurality of subfields. Each subfield period comprises an addressing period during which charges are created in the cells of the PDP which must generate light during the corresponding subfield. This generation of light is obtained by a sustain voltage during the remaining of the subfield.

According to the invention, each cell generates light only in addressed successive subfields, starting from the first subfield, the erasing (E_1) during each subfield being limited to cells for which no light must be generated during the corresponding subfield and the remaining subfield(s) of the same field.

Preferably, during each subfield, addressing (A) and erasing (E_1) are simultaneous.

FIG.4



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Description

[0001] The invention relates to a method for controlling a plasma display panel and to a display apparatus using this method.

[0002] Plasma display panels (PDPs) used for image reproduction, such as for display of television images, are either of the AC type or of the DC type. For simplification purpose, AC type will be only described here. A PDP comprises a transparent front plate, to which is associated a first set of parallel electrodes, and a back substrate, associated with a second set of parallel electrodes, perpendicular to the first set. The interval between the front and back plates is separated in cells containing a gas, for instance a mixture of Xenon and Neon, which, when selectively and properly excited by voltages applied to electrodes, produce ultraviolet (UV) light and this UV light excites phosphors deposited on walls of the cell and generate visible light.

[0003] PDPs are good solutions for the display of images, because they are flat and can be realized with an area which is greater than the areas of current displays such as cathode-ray tubes (CRTs) and liquid crystal displays (LCDs). Although the quality of pictures is quite satisfactory, the contrast may be improved. Moreover, in certain circumstances, moving pictures present unpleasant blurred contours.

[0004] The low contrast comes from the undesirable emission of light during periods which do not correspond to the controlled excitation of the gas in each cell.

[0005] In fact, the control of a current PDP is realized in the following way:

[0006] At the beginning of each field is realized a priming of the cells, the goal of which is to generate charges on the walls of all the cells; in this case, the cells already presenting charges do not change of state and the cells which have no charges accumulate charges.

[0007] Afterwards, all the cells are erased in order to eliminate these wall charges. It is to be noted that the succession of priming and erasing is necessary in order to eliminate the wall charges. In fact, if the priming did not take place before the erasing, cells presenting no charges would accumulate wall charges during erasing.

[0008] After erasing, the cells which must emit light are addressed. The addressing is an operation similar to priming, i.e. charges are created on the walls of cells. However, this addressing has a shorter duration than priming and is, of course, selective. For instance, the duration of priming is about 15 μ s and the duration of addressing is generally less than 3 μ s.

[0009] For priming, erasing and addressing, voltages are created between the front and the back faces and the pulses are of the DC type.

[0010] After the addressing period, a sustain voltage is applied to the addressed cells. This sustain voltage is an alternative current (AC) at a high frequency, generally comprised between 100 and 500 kHz. This sustain voltage may be applied either between a front and a

back electrodes or between two parallel electrodes on one side of the panel.

[0011] It is only during this sustain period, that the cells emit useful light.

[0012] During the priming and the erasing periods, all the cells emit light. This light is undesirable for the cells which are not selected. This explains the relatively poor contrast obtained with plasma display panels.

[0013] Each field is divided into, for instance, subfields having lengths which decrease from the first to the last subfield. Each cell emits light during subfields which are selected in such a way that the luminance of a pixel corresponds to the addition of the times of active subfields.

[0014] As represented on figure 1, the length of the sustain period in each subfield is such that the first subfield corresponds to the least significant bit (LSB) and the last subfield corresponds to the most significant bit (MSB). Therefore, if the duration of the sustain period of this subfield is 1, the durations of the subsequent subfields are respectively 2, 4, 8, 16, 32, 64 and 128, corresponding, respectively to the second, third, fourth, fifth, sixth, seventh and eighth subfields. Therefore, it is possible to obtain 256 levels of luminance, each luminance being expressed by a number of 8 bits.

[0015] This distribution of light generation with time may, in certain circumstances, create defects as explained with figure 2.

[0016] On figure 2, four successive pixels a, b, c and d of the same line have been represented. These pixels are represented in abscissa and the time is in ordinate.

[0017] In this simplified example, each field (or frame) has four bits, i.e. four subfields for which the sustain period is, respectively, 1, 2, 4 and 8. During the first field (F_1), the luminance of pixels a and b is 8; this means that only the fourth subfield emits light and the first three subfields remain dark. The pixels c and d have the luminance 7 during this same field F_1 . Therefore, the first three subfields are active and the last subfield corresponds to no emission of light because $7 = 0111$. It is supposed that, during the second field F_2 , there is a movement such that pixels a and b keep the luminance 8 and pixel c has its luminance increased from 7 to 8 and the luminance of pixel d remains at value 7. In these circumstances, the eye e of the viewer follows the movement of the moving contour, when the luminance decreases from 8 to 7. This following movement is represented by the oblique lines 10, 12, 14 on figure 2. The oblique line 10 corresponds to a black line and the luminance increases from this line 10 to the parallel lines respectively 12 and 14. Of course, the eye does not see a black line, but a relatively dark or blurred contour which is quite unpleasant.

[0018] The invention eliminates the drawbacks mentioned herein above, i.e. it increases the contrast and it prevents blurring due to certain moving images as described with figure 2.

[0019] According to the invention, during each sub-

field, the erasing is limited to the cells for which no emission is necessary in the corresponding subfield and for the subsequent subfields in the same field. In other words, the invention provides a selective erasing and not an erasing for all the cells. Therefore, the emission of unnecessary light due to erasing is limited and the contrast is improved.

[0020] Moreover, when the luminance increases the distribution of the light according to the time increases regularly from the first subfield to the last subfield. In other words, when the luminance increases of one unit, the number of successive subfields which are active increases of one. Therefore, the blurring appearing with the embodiment described with figures 1 and 2 is prevented, because the generation of light is, in the invention, always beginning with the first subfield(s).

[0021] Advantageously, the addressing is simultaneous to the erasing. Therefore, the duration of the control part of each subfield is reduced.

[0022] In an embodiment, all the subfields have the same duration. Therefore, the control of the PDP is simplified.

[0023] Other features and advantages of the invention will appear with the description of certain of its embodiments, this description being made in relation with the herein-appended drawings, wherein:

figure 1, already described, corresponds to the control of a conventional plasma display panel, figure 2, also already described, is a diagram showing some properties of a conventional PDP, figure 3 is also a diagram explaining the operation of a conventional PDP,

figure 4 is a diagram similar to the diagram of figure 3 showing the operation of a PDP according to the invention,

figure 5 is a diagram similar to figure 1 explaining also the operation of the PDP according to the invention,

figure 6 and figure 7 are diagrams similar to the diagram of figure 5 but for two other embodiments of the invention,

figure 8 is a schematic drawing showing one cell of a PDP with its associated electrodes and also control means for the electrodes,

figure 9 and figure 10 are schematic drawings explaining the operation of the PDP according to the invention,

figure 11 is a drawing showing some elements of a cell for an embodiment of the invention,

figure 12 is a diagram showing some control signals for the embodiment of figure 11,

figure 13 is a diagram similar to figure 2, showing advantages of the invention with respect to prior art, and

figure 14 is a diagram used for explaining further aspect of the invention.

[0024] Figure 4 shows clearly the difference between the invention and the prior art as represented on figure 3.

[0025] As shown on the diagram of figure 3, at the beginning of the first subfield, i.e. at the beginning of subfield 1, all the cells, which constitute capacitors, are loaded with control signals such that all the cells have the same charges. This operation is called priming P. After the priming, in subfield 1, all the cells are discharged. This operation, which consists in applying control signals in the reverse direction of the control signal for priming P, is called erasing E. The erasing operation E is realized at the beginning of all the subsequent subfields: 2, 3, etc.

[0026] After erasing E, also during each subfield, the cells which must be lit (generate light) are loaded or addressed A. During the remaining time of the subfield, an AC voltage is applied in order that the addressed cells maintain their generation of light during this remaining time of the subfield, as described with reference to figure 1.

[0027] According to the invention, in order to create the required level of luminance for each cell, the cells are lit during successive subfield(s) starting from subfield 1 and, if they must not produce maximum luminance, they are extinguished during the last subfield(s). With this embodiment, erasing E_1 is necessary only for the cells which must not generate light during the current subfield and the subsequent subfield(s). It is therefore possible to perform simultaneously erasing E_1 for such selected cells, and addressing A for the other cells of the PDP.

[0028] This property is shown on figure 4 where E_1 and A are represented by the same time segment.

[0029] It must be noted here that, although the time spent for erasing and addressing may be reduced compared to prior art, the fact that it is possible for each pixel or cell to generate light only during successive subfields starting from subfield 1, may reduce (compared to prior art) the total number of luminance or grey levels which it is possible to generate. It is the reason why the design of the control of the PDP must be such that it maximizes the number of luminance levels. Herein below, several embodiments will be described which achieve this maximization. However, even if the number of grey levels is smaller than with the prior art, the PDP according to the invention has important advantages which compensate this drawback. One advantage is the improvement of contrast of the image because the total duration of erasing periods is much smaller in the PDP according to the invention than in the conventional PDP. Moreover, as will be explained hereinafter with reference to figure 13, the generation of light only from subfield 1 and successive subfield(s) provides the advantage that no blurring occurs, contrary to what happens with conventional PDPs as explained above with figure 2.

[0030] In the embodiment shown on the diagram of figure 5 which represents the control of one line, all the subfields have the same duration. In this example, P

means priming, E_1 means simultaneous erasing and addressing (for different cells) for subfield 1, and S_1 is the sustain period for this subfield 1. More generally, E_n means the simultaneous erasing and addressing for subfield n and S_n means sustaining for this subfield n .

[0031] Compared to conventional PDPs, where the duration of the sustain period increases (doubles) from one subfield to the subsequent subfield, the control is much simpler.

[0032] Figure 6 represents the control of the successive lines. In this example, the number of lines is 480 and the $E_1, E_2, \dots$ periods must be distributed in time in such a way that no interference may happen between the control of successive lines. In this example, the priming P is performed simultaneously for all the cells and the $E_1, E_2, E_3, \dots$ periods are contiguous from one line to the subsequent line, without any overlapping. In other words, each line begins with respect to the previous line, after a delay which equals the duration of an E_1 period.

[0033] This delay from one line to the other entails a "suspending" period $SP_1 \dots SP_{480}$ between the end of the priming P and the beginning of E_1 period. This suspending period SP_n is maximum for the last line 480. During this suspending period, no luminance signal is generated. It is also to be noted that corresponding suspending periods SP'_n are provided at the end of each line, i.e. between the end of the last erasing/addressing period and the beginning of priming P for the next field. This suspending period SP'_n is maximum for the first line and is equal to zero for the last line.

[0034] In the embodiment represented on figure 7, the suspending periods are suppressed. In order to achieve this goal, the priming periods for successive lines are staggered, i.e. the priming periods are not simultaneous. More precisely, the priming P_2 period for line 2 appears immediately after the end of priming period P_1 , with no delay between the end of P_1 and the beginning of P_2 . In this embodiment, the erasing/addressing period for subfield 1 appears immediately after priming, with no delay. As concerns the erasing/addressing periods for the other subfields: subfield 2, subfield 3, etc., they are staggered in such a way that for line n , this erasing/addressing period begins when the erasing/addressing period for line $n - 1$ finishes.

[0035] Figure 8 represents a cell of a PDP. Conventionally, a plasma display panel comprises a front substrate (not shown) which is transparent and a back substrate (not shown). The back substrate is provided with parallel ribs 13, 15 which constitute walls separating the space between the front and the back substrates. This space is filled with a mixture of gases such as Neon and Xenon. An addressing electrode 16 is associated with each space between two neighboring partition ribs 13, 15. In this example, the addressing, or line, electrode 16 is on the middle of the space separating ribs 13 and 15, on the front side.

[0036] To each cell is also associated a couple 18, 20 of electrodes on the backside. These electrodes are per-

pendicular to the ribs. The electrode 20 is used for addressing and both electrodes 18 and 20 are used for the application of the AC sustain voltage.

[0037] For priming, erasing and addressing, a DC voltage is created between electrodes 16 and 20.

[0038] As shown on the schematic diagrams of figures 9 and 10, the cells $C_{11}, C_{12}, \dots, C_{21}, C_{22}, \dots$ are disposed according to a matrix with lines $l_1, l_2, l_3, \dots$ and columns, $col_1, col_2, \dots$.

[0039] During the addressing/erasing period for line 1 and subfield n , an addressing pulse 30_1 is generated on line 1 and, simultaneously, on each column is generated either an erasing pulse 32_1 , if the corresponding cell C_{11} must be erased, or no pulse (zero pulse 32_2) is generated, if the corresponding cell C_{12} must generate light. The erasing pulses are generated simultaneously with the addressing pulses and have the same duration, i.e. 5 μs .

[0040] The erasing pulse 32_1 of column col_1 suppresses the wall charges only on cell C_{11} , because, during its appearance, only line 1 is addressed and not the other lines.

[0041] As described with reference to figure 8, each column electrode col_1, col_2 comprises two electrodes 18, 20. During the sustain period, an AC current is applied between these electrodes. The AC voltage is applied after the erasing/addressing pulse until the end of the corresponding subfield. Only the non-erased cells emit light. As shown on figure 10, cell C_{11} , which has been erased, remains black and cell C_{12} , which has been addressed, generates light.

[0042] It is to be noted that, with a duration of 5 μs for each addressing/erasing pulse, the total duration of addressing/erasing is, for one frame (480 lines), 2.4 ms for each subfield, i.e. 12 ms for each field if 5 subfields are provided for 1 field. As in the NTSC standard the duration of one field is 16.7 ms, the duration of the remaining sustain period is 4.7 ms for each field, i.e. 1 ms for each subfield.

[0043] In order to optimize the sustain time, it is preferable to use the embodiment represented on figure 7.

[0044] Moreover, the number of possible luminance levels being limited, it is preferable to increase this number. For this purpose, it is possible to use the conventional double scan method according to which the lines are divided in two sets. For instance, if there are 480 lines, the first set comprises lines 1-240 and the second set comprises lines 241-480.

[0045] With this double scan method, the lines of the two sets are addressed simultaneously. In other words, line 1 is addressed simultaneously with line 241, line 2 is addressed simultaneously with line 242, ... and line 240 is addressed simultaneously with line 480.

[0046] In order to further increase the duration of the sustain periods compared to the addressing/erasing periods, it is possible to address lines during overlapping periods. In this embodiment, it is necessary to provide several - for instance five - electrodes per column. As

shown on figure 11, five electrodes correspond to col₁ or col₂ of figure 9. The reference of these electrodes are A₁ to A₅.

[0047] For erasing the cell C₁₁, a pulse 38 (figure 12) of 5 μs is applied to line 1 and, simultaneously, a pulse 39 of the same duration is applied to electrode A₁.

[0048] In order to erase cell C₂₁ (the cell on the second line and first column), line 2 is addressed with a pulse 40 beginning 1 μs after the beginning of the pulse 38 applied on line 1 and having also a duration of 5 μs. Simultaneously, a pulse 42 of duration 5 μs is also applied on column electrode A₂ of column col₁. If cell C₂₁ must not be lit, no pulse 42 is applied on electrode A₂.

[0049] In spite of the simultaneous presence of pulse 40 on line 2 and pulse 39 on electrode A₁ during an overlapping time of 4 μs, cell C₂₁ is not erased because this duration of 4 μs is insufficient to erase a cell.

[0050] With this embodiment, the duration of addressing five lines is 9 μs. Therefore, it is possible to divide one field into nineteen subfields, because the total duration of addressing is $\frac{480 \times 9}{5} = 864 \mu s$ which is about 1/19 of the duration of 1 TV frame (1/60 s).

[0051] If simultaneously, double scan is used, one field may be divided into 38 subfields. In other words, it is possible to have 38 luminance levels for one color. For three colors, this may amount to 114 levels.

[0052] In general, this number of luminance levels would be sufficient. However, it is further possible to increase this number of levels with conventional technologies used for picture compression or for improving the quality of pictures transmitted by facsimile machines or computer displays. These techniques are called dithering and error diffusion methods; these methods are conventionally used for personal computers (PCs) and LCDs (Liquid Crystal Displays).

[0053] Figure 13 is a diagram similar to figure 2 wherein, during field F₁, the pixels a and b have the luminance level 8 and the pixels c and d have the level 7. During the field F₂, pixels a and b keep their luminance level 8, but pixel c has the luminance 8 and pixel d keeps the level 7.

[0054] It can be seen that no blurring occurs because with the eye following the movement of pixel b, the eye sees a smooth transition between luminance 8 and 7 as shown by the inclined lines α, β and γ. On line α, the eye sees a luminance of value 8, and on line β, where the eye sees the transition from 8 to 7 at each time, the luminance is 7. On line γ, the luminance remains 7.

[0055] In an embodiment, the duration of subfields is modulated in order to perform a γ correction. Fig. 14 shows an example of a PDP wherein the luminance L generated by the PDP varies, in function of the input signal I, according to curve 80 wherein, when the input signal grows linearly with the values: 1, 2, 3, 4, 5, 6, 7, the PDP luminance has the values 1, 1+1=2, 1+1+2=4, 1+1+2+3=7, 1+1+2+3+4=11, 1+1+2+3+4+5=16, 1+1+2+3+4+5+6= 22.

[0056] In that case in subfield 1, the sustain period will

have duration to, and the sustain periods of subfields 2 to 7 will be respectively to, 2to, 3to, 4to, 5to and 6to.

5 Claims

1. Method for controlling a plasma display panel, wherein each field is divided into a plurality of subfields, each subfield period comprising an addressing period during which charges are created in the cells of the PDP which must generate light during the corresponding subfield, this generation of light being obtained by a sustain voltage during the remaining of the subfield, characterized in that each cell generates light only in addressed successive subfields, starting from the first subfield, the erasing during each subfield being limited to cells for which no light must be generated during the corresponding subfield and the remaining subfield(s) of the same field.
2. Method according to claim 1, characterized in that, during each subfield, addressing (A) and erasing (E₁) are simultaneous.
3. Method according to claim 1 or 2, characterized in that the subfields have substantially the same duration.
4. Method according to any of the previous claims, characterized in that a priming (P₁, P₂, ...) is performed, during the first subfield of each field, and in that, for each field, the priming of one line begins at the end of the priming of the previous line.
5. Method according to any of claims 1-3, characterized in that a priming is performed during the first subfield of each subfield and in that, for each field, the primings of all lines are simultaneous.
6. Method according to any of the previous claims, characterized in that the lines are divided into sets, the first and the second sets being controlled simultaneously.
7. Method according to any of the previous claims, characterized in that each column being controlled by N electrodes (A₁-A₅), the addressing pulses (38,40) of two successive lines have a duration of T and the beginning of the pulse controlling the second of the two successive lines follows the beginning of the pulse controlling the previous line by a duration of T/N, one line being associated to one of the N column electrodes on which is applied simultaneously, if necessary, an erasing pulse simultaneous with the pulse on the corresponding line, the number N being chosen in such a way that the overlapping period of an addressing pulse on one line

and an erasing pulse on the column electrode corresponding to the previous line is insufficient to perform an erasing.

8. Method according to any of the previous claims, characterized in that the duration of subfields is modulated in order to perform a γ correction. 5
9. Method according to any of the previous claims, characterized in that the plasma display panel is of the AC type. 10

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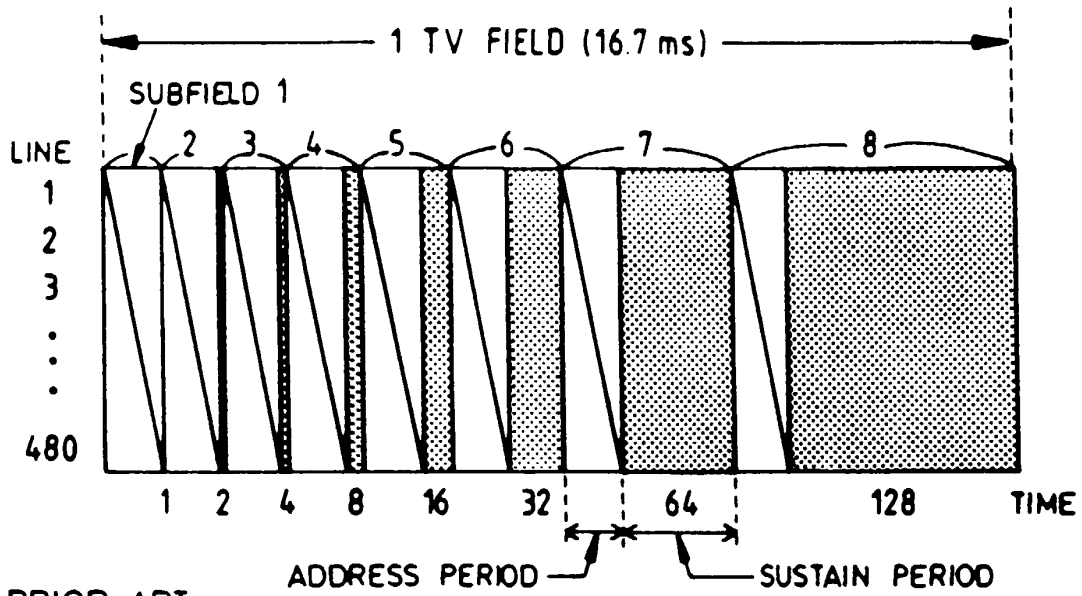
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PRIOR ART
FIG.1

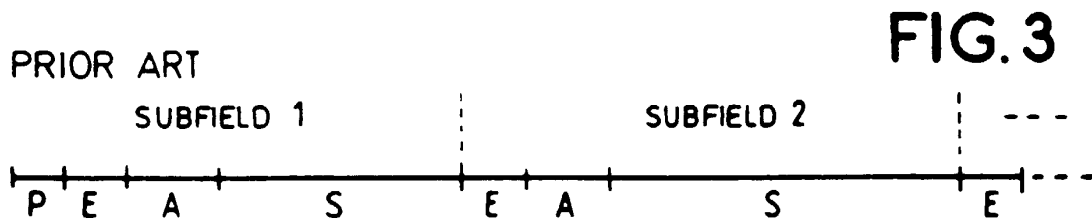


FIG.3

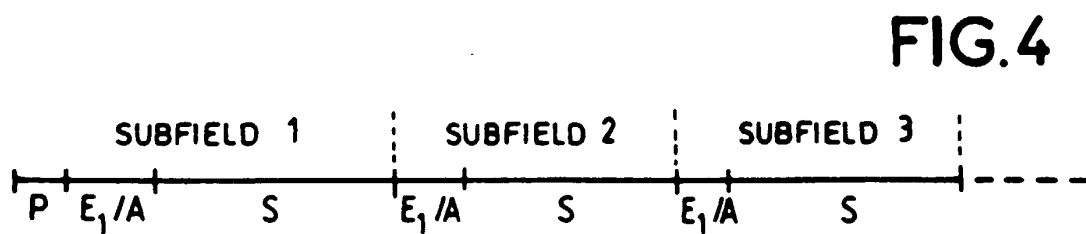


FIG.4

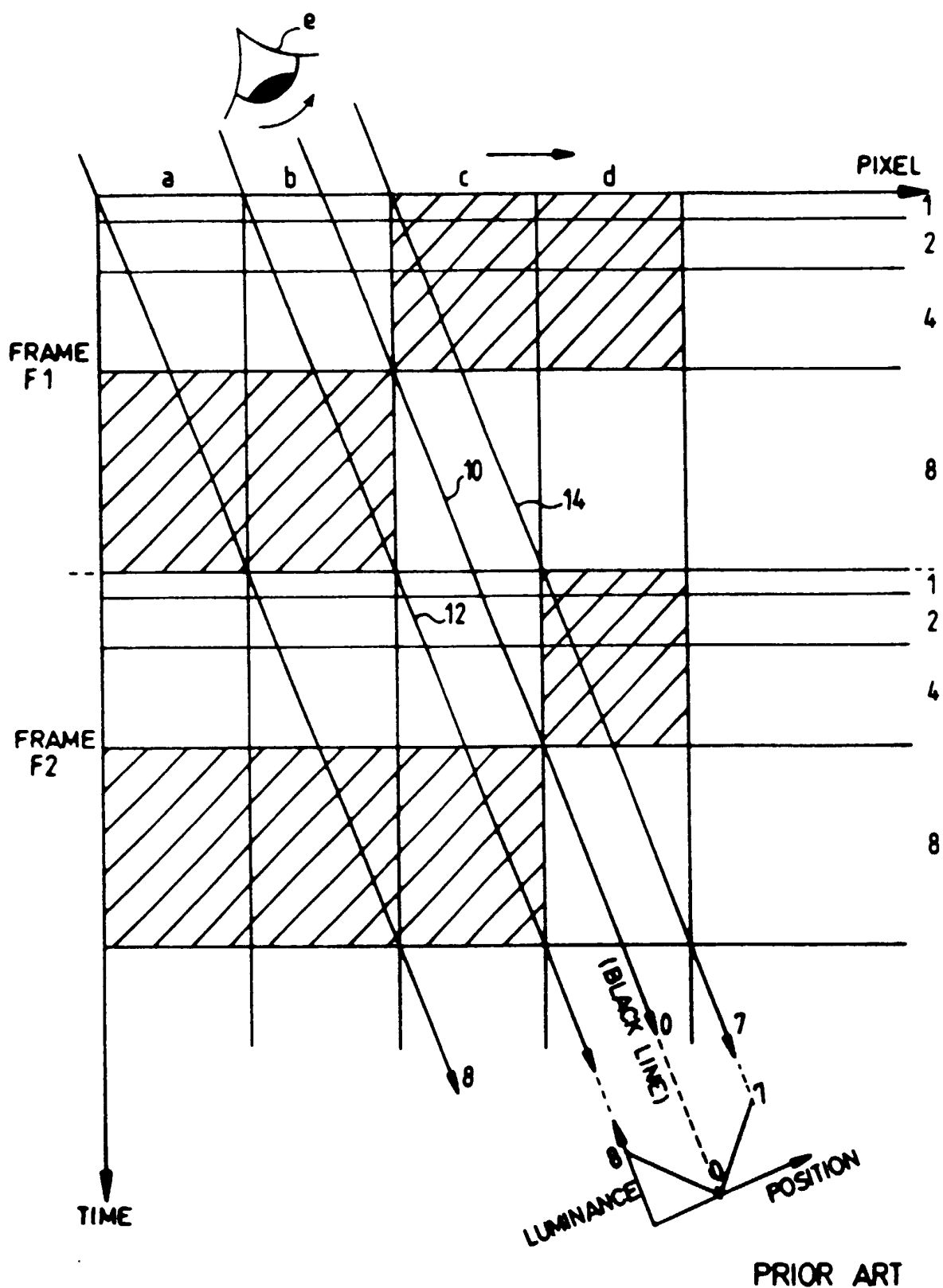


FIG.2

FIG.5

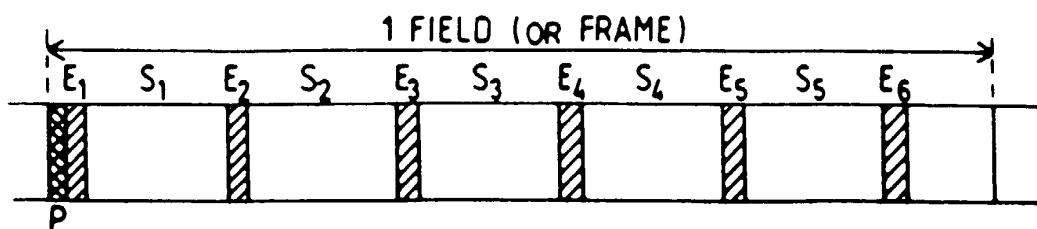


FIG.6

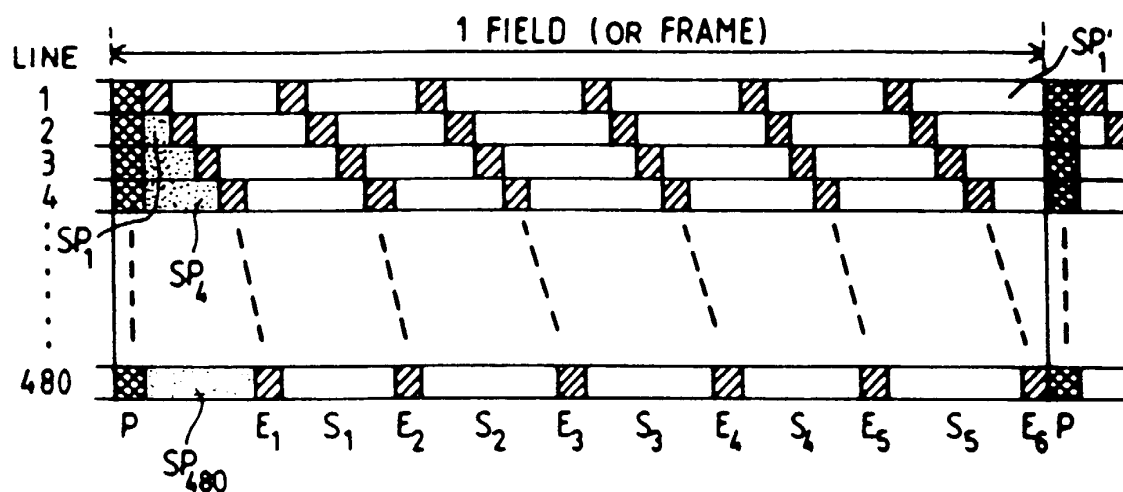
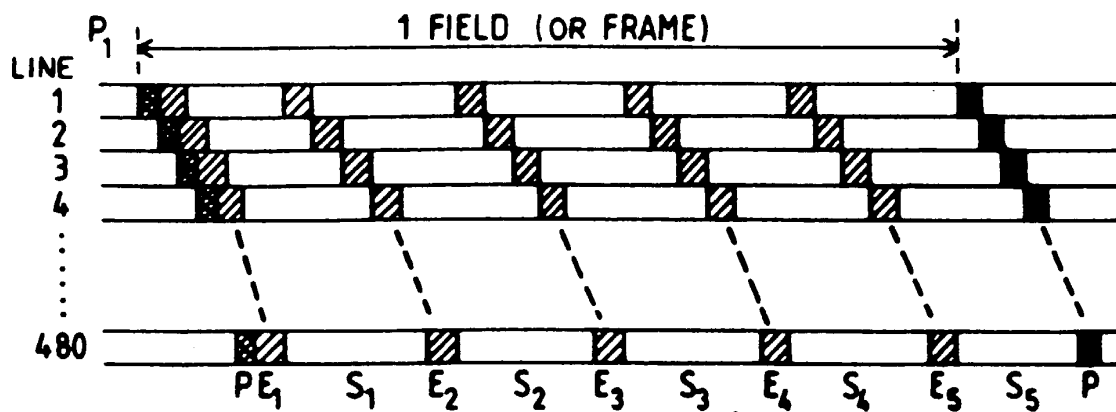


FIG.7



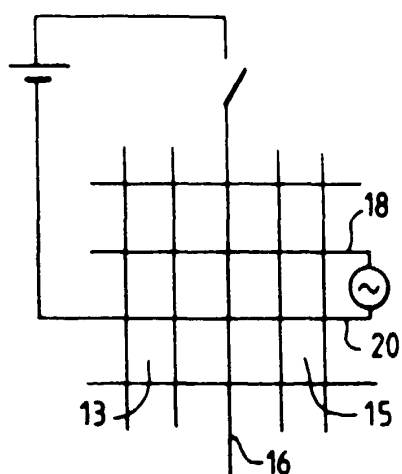


FIG. 8

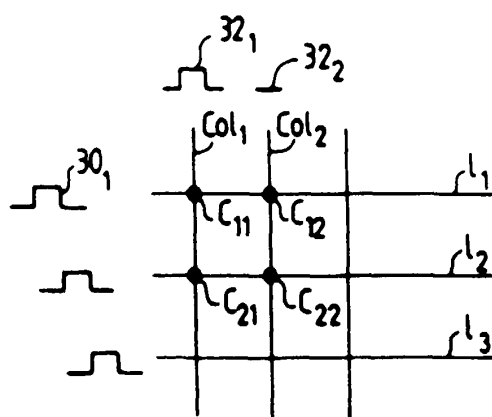


FIG. 9

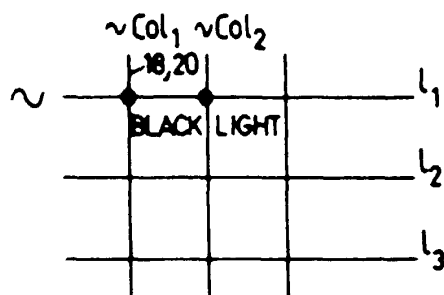


FIG. 10

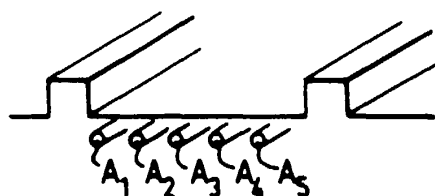


FIG. 11

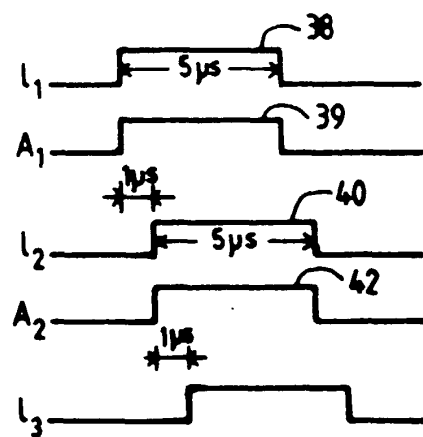


FIG. 12

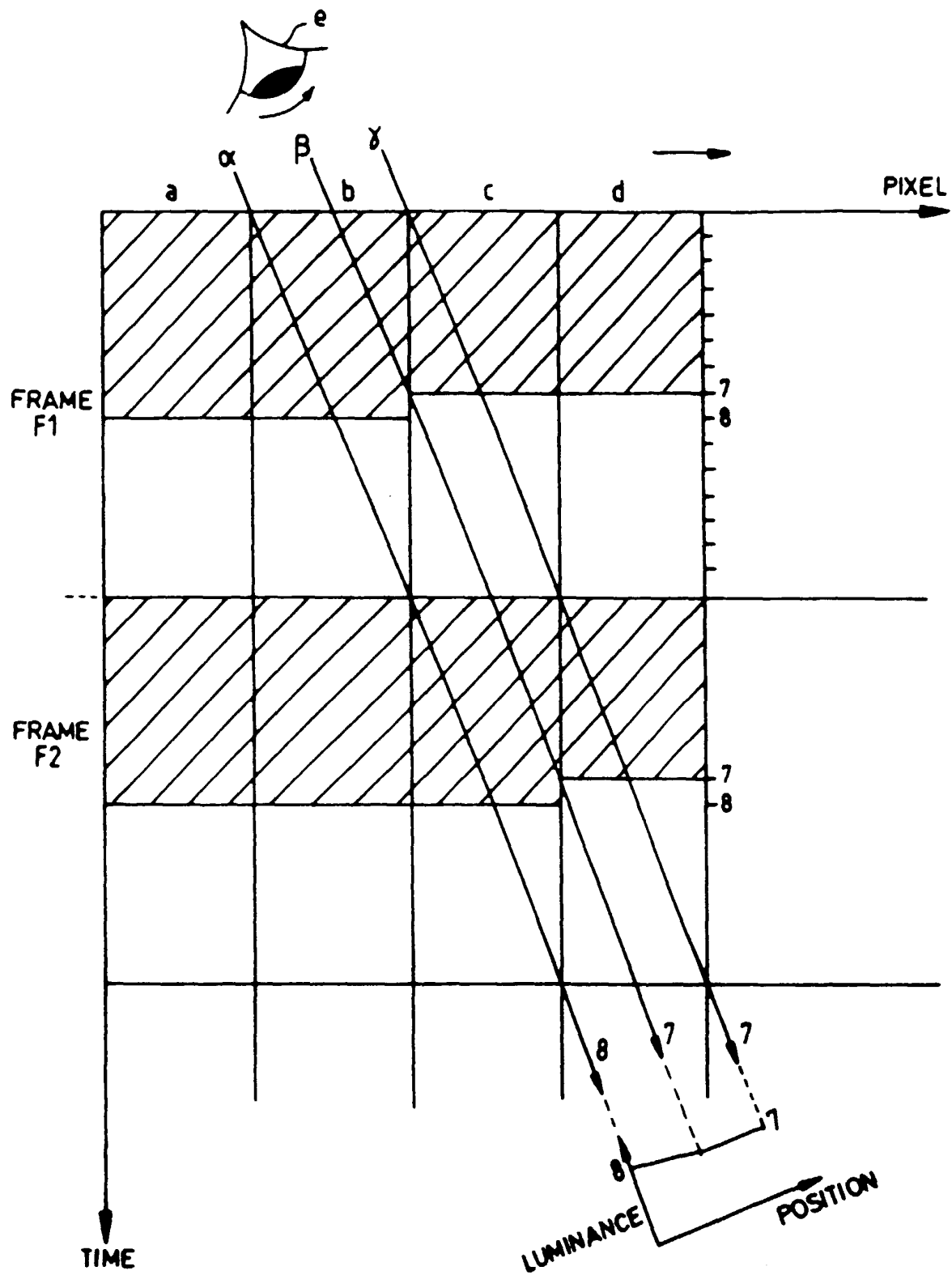


FIG.13

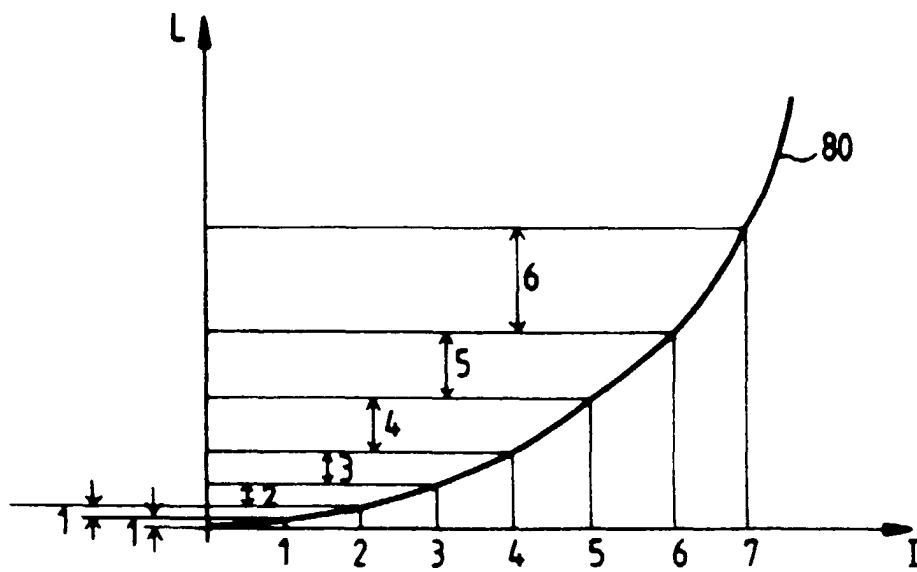


FIG.14



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 40 0457

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 834 856 A (LG ELECTRONICS INC.) 8 April 1998 (1998-04-08)	1,2,4,9	G09G3/28
Y	* abstract *	3,6,8	
A	* page 3, line 23 - line 26 * * page 4, line 20 - line 47; figures 6-8 * ---	5,7	
Y	FR 2 740 253 A (FUJITSU LTD.) 25 April 1997 (1997-04-25) * abstract * * page 26, line 19 - line 26 * * page 51, line 3 - line 15; figures 16,49-52 * ---	3	
Y	EP 0 762 373 A (FUJITSU LTD.) 12 March 1997 (1997-03-12) * column 27, line 3 - column 28, line 14; figures 2,27-29 * ---	6	
Y	EP 0 833 299 A (NIPPON ELECTRIC CO) 1 April 1998 (1998-04-01) * abstract * * column 7, line 51 - column 8, line 4 * * column 16, line 1 - line 55; claims 9,10 * -----	8	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G09G
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 6 June 2000	Examiner O'Reilly, D
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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 00 40 0457

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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06-06-2000

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82