(19) **Europäisches Patentamt**
European Patent Office
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(11) **EP 1 049 154 A3**

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
18.12.2002 Bulletin 2002/51

(43) Date of publication A2:
02.11.2000 Bulletin 2000/44

(21) Application number: **00303599.5**

(22) Date of filing: **28.04.2000**

(51) Int Cl.⁷: **H01L 21/762**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.04.1999 JP 12109599**

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(54) Process for forming device isolation region

(57) A process for forming a device isolation region comprising the steps of: forming a pad oxide film and a silicon nitride film on a semiconductor substrate; removing the pad oxide film and the silicon nitride film on a region for device isolation and forming a trench in the semiconductor substrate by etching using the remaining pad oxide film and silicon nitride film as an etching mask; forming a first oxide film at least on the bottom and sidewalls of the trench and below the pad oxide film under an end portion of the silicon nitride film using the silicon nitride film as a mask resistant to oxidization; forming a gap between the silicon nitride film and the semiconductor substrate by removing the first oxide film on the bottom and the sidewalls of the trench and the first oxide film and the pad oxide film below the end portion of the silicon nitride film by etching using the silicon nitride film as an etching mask; forming a second oxide film at least on the bottom and the sidewalls of the trench and in the gap using the silicon nitride film as a mask resistant to oxidization; and forming a third oxide film so as to fill the trench, thereby to form a device isolation region.

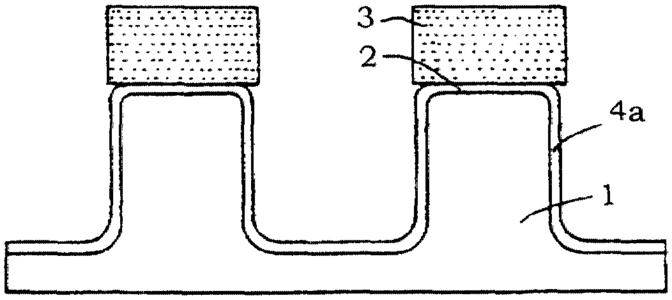

Fig. 1 (c)

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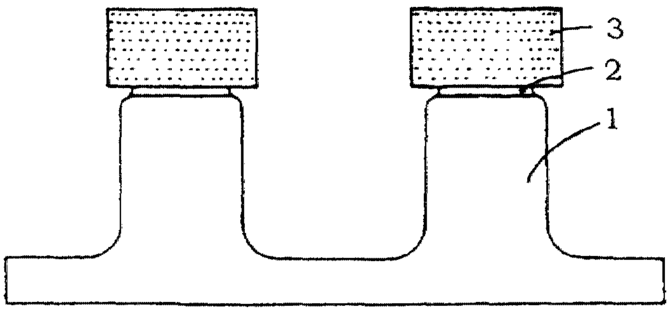

Fig. 1 (d)

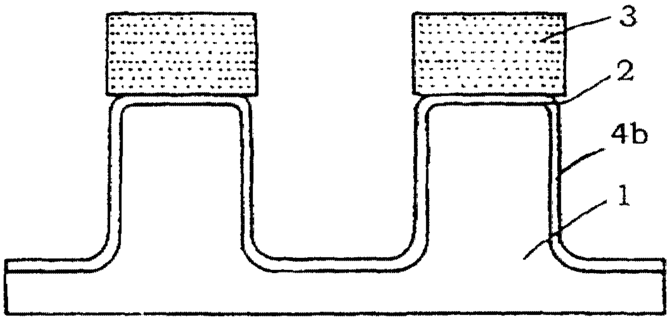

Fig. 2 (a)

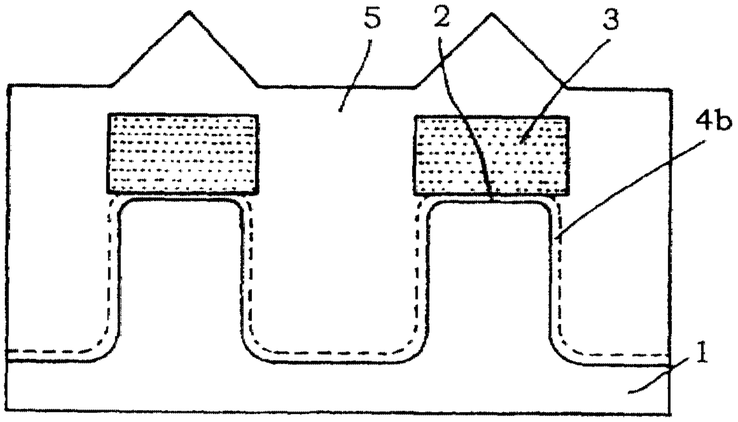

Fig. 2 (b)

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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 3599

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 05, 30 April 1998 (1998-04-30) -& JP 10 012716 A (TOSHIBA CORP), 16 January 1998 (1998-01-16) * abstract; figures 6-13 * ---	1-7	H01L21/762
Y	US 5 863 827 A (JOYNER KEITH) 26 January 1999 (1999-01-26) * figures * * column 3, line 26 - line 54 * ---	1-7	
A	YEH W-K ET AL: "A NOVEL SHALLOW TRENCH ISOLATION WITH MINI-SPACER TECHNOLOGY" JAPANESE JOURNAL OF APPLIED PHYSICS, PUBLICATION OFFICE JAPANESE JOURNAL OF APPLIED PHYSICS. TOKYO, JP, vol. 38, no. 4B, April 1999 (1999-04), pages 2300-2305, XP000923618 ISSN: 0021-4922 * abstract; figure 2 * ---	1-7	
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A	CHATTERJEE A ET AL: "A shallow trench isolation using LOCOS edge for preventing corner effects for 0.25/0.18 /spl mu/m CMOS technologies and beyond" ELECTRON DEVICES MEETING, 1996., INTERNATIONAL SAN FRANCISCO, CA, USA 8-11 DEC. 1996, NEW YORK, NY, USA,IEEE, US, 8 December 1996 (1996-12-08), pages 829-832, XP010207668 ISBN: 0-7803-3393-4 * abstract; figure 1 * ---	1-7	H01L
A	US 5 834 358 A (PAN PAI-HUNG ET AL) 10 November 1998 (1998-11-10) * abstract; claims; figures 9-14 * -----	1-7	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 October 2002	Wirner, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 30 3599

24-10-2002

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82