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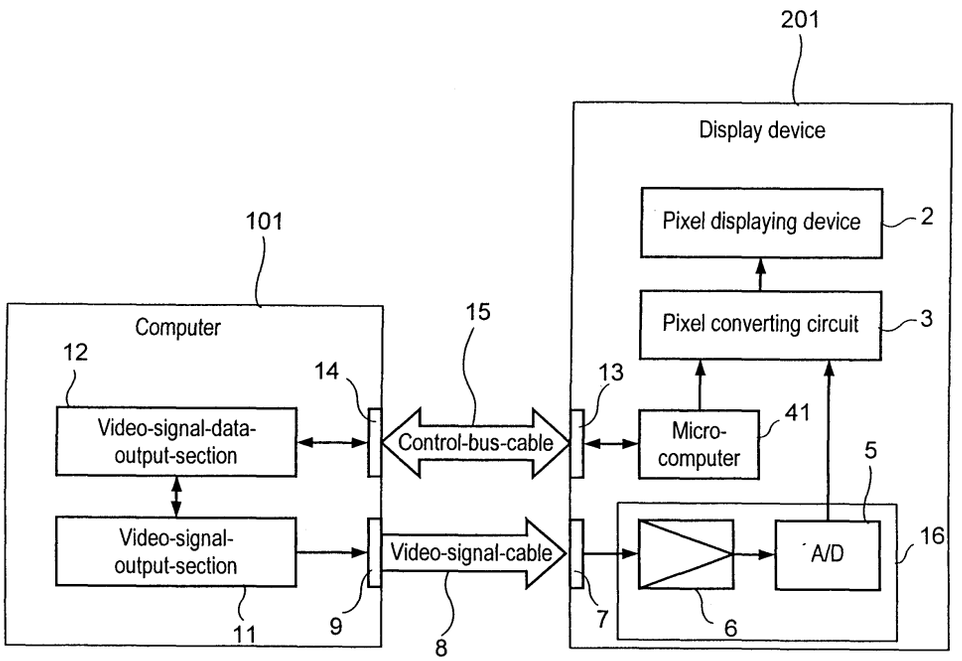
(54) Interconnection between a computer and a display

(57) A display device includes video-signal-processor for receiving an input-video-signal and pixel-converting-circuit for converting a pixel of an output signal from the video signal processor so that display device can display the input video signal as an appropriate video on a pixel-displaying device, where the display device receives pixel-format-data of the input video signal through a control bus independent of the input video signal. A computer system includes a computer having video-signal-outputting-section for outputting a video signal to display device, video-signal-data-outputting-section for outputting format data of the video signal output from section, and a control bus for transmitting the format data of the input video signal as well as a request of transferring the format data from the display device.

FIG. 1



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Description

Field of the Invention

[0001] The present invention relates to a pixel displaying device such as a liquid crystal display (LCD), and a computer as well as a computer system.

Background of the Invention

[0002] Fig. 2 is a block diagram of a conventional computer system. In Fig. 2, display device 202 comprises the following elements:

(a) video-signal-processor 16 for receiving an input video signal;

(b) pixel displaying device 2 for displaying a video such as an LCD;

(c) micro-computer 42 for counting a number of sync. signals of the input video signal and determining a pixel format of the input video signal; and

(d) pixel converting circuit 3 for converting pixels of an output signal from video-signal-processor 16 and then outputting the converted signal to pixel displaying device 2, by referring to an output from micro-computer 42.

[0003] Video-signal-processor 16 comprises the following elements:

video amplifier 6 for amplifying a video signal; and

A/D converter 5 for converting a signal amplified by amplifier 6 into a digital signal.

[0004] When receiving a video signal via video-signal-cable 8 from video-signal-output-section 11 incorporated in computer 102, display device 202 structured above, counts a number of pulses in horizontal sync. signal and vertical sync. signal of the video signal using micro-computer 42. Then micro-computer 42 specifies a pixel format of the video signal.

[0005] A digital-video-signal is converted by an output signal - following the specified pixel format - from micro-computer 42.

[0006] Pixel-converting-circuit 3 converts the pixels of the digital video signal, so that pixel displaying device 2 displays a video correctly.

[0007] However, in the conventional computer system discussed above, display device 202 counts the data of the video signal supplied from computer 102 with micro-computer 42, and specifies the video signal by detecting a polarity of the sync. signal. Therefore, counting of pulses of sync. signals largely depends on the performance of micro-computer 42. Further, pixel-conversion capability also largely depends on a number of interrupts handled by micro-computer 42.

[0008] Signals similar to the input signals to display device 202 from computer 102 are available in the market. Therefore, only a frequency and polarity of the horizontal sync. signal and vertical sync. signal are not enough to exactly specify the pixel format of the video signal.

[0009] As a result, pixel displaying device 2 including an LCD panel does not display a video, or even if it could display the video, the displayed video is not in an optimal condition.

Summary of the Invention

[0010] A display device displays a video signal on a pixel displaying device by allowing the display device to receive the pixel format data (PFD) specified by the computer.

[0011] The computer outputs PFD independently of a video signal and the display device receives and determines the PFD independently of the video signal.

[0012] This structure allows the display device to determine the PFD of an input video signal exactly, so that the pixel displaying device can display a video in an optimal condition.

Brief Description of the Drawings

[0013] Fig. 1 is a block diagram of a computer system in accordance with an exemplary embodiment of the present invention.

[0014] Fig. 2 is a block diagram of a conventional computer system.

Description of the Preferred Embodiment

[0015] A preferred embodiment of the present invention is demonstrated hereinafter with reference to the accompanying drawings. The same elements shown in the conventional computer system in Fig. 2 are marked with the same reference numbers in Fig. 1.

[0016] In this embodiment, a control bus for receiving PFD corresponding to input video signals is provided in order to carry out pixel conversion more accurately than the conventional display device. Further, microcomputer 42 is replaced with microcomputer 41 having a specific structure.

[0017] Conventional microcomputer 42 counts an H. sync frequency of an H. sync signal and a V. sync frequency of a V. sync signal. Based on the counted H and V frequencies, microcomputer 42 calculates a pixel format of the video signal using a calculation formula, e.g. VESA-GTF (Video Electronics Standards Association - Generalized Timing Formula Standard).

[0018] In contrast, microcomputer 41 receives a pixel format of a video signal through control bus 15. (The pixel format includes an H. sync frequency, V. sync fre-

quency, H display area, H back porch and the like.) Thus, microcomputer 41 does not need a calculation formula such as VESA-GTF.

[0019] The elements of the computer system of the present invention other than the control bus and microcomputer 41 remain the same as the conventional computer system shown in Fig. 2. In other words, display device 201 shown in Fig. 1 differs from conventional display device 202 shown in Fig. 2 in microcomputer 41 and an input/output terminal 13 of a first control bus coupled to microcomputer 41.

[0020] In computer 101, video-signal-data-output section 12 and input/output terminal 14 of a second control bus coupled to section 12 are provided to a conventional computer 102 shown in Fig. 2.

[0021] A control bus on the side of display device 201 comprises input/output terminal 13 of the first control bus and microcomputer 41.

[0022] To be more specific, microcomputer 41 requests to transfer the PFD of an input video signal from computer 101 through input/output terminal 13 of the first bus, control bus cable 15, and input/output bus terminal 14 of the second control bus. Then at the next timing, microcomputer 41 receives the PFD from video-signal-data-output section 12 through the same route as discussed above but in the reverse order.

[0023] The structure discussed above allows display device 201 to receive the PFD of the input video signal from computer 101 through an independent control bus of the input video signal. Therefore, even if the input video signal is changed or a signal similar thereto is handled, display device 201 can determine a pixel format of the video signal exactly and free from erroneous recognition of the input video signal. As a result, pixel-displaying-device 2 can constantly display videos in an optimal condition.

[0024] Details of the PFD include e.g. the following items in a Video Graphic Array (VGA) format:

(a) horizontal frequency = 31.46 kHz (800 dot)

(b) horizontal display time = 25.423 μsec (640 dot)

(c) horizontal sync. time = 3.813 μsec (96 dot)

(d) horizontal-back-porch time = 1.907 μsec (48 dot)

(e) horizontal-front-porch time = 0.636 μsec (16 dot)

(f) vertical frequency = 59.93 Hz (525 line)

(g) vertical display time = 15.254 msec (480 line)

(h) vertical sync. time = 0.064 msec (2 line)

(i) vertical-back-porch = 1.049 msec (33 lines)

(j) vertical-front-porch = 0.318 msec (10 line)

(k) dot clock frequency = 25.17 MHz

(l) interlace = not available

[0025] The details of the PFD are not limited to the items discussed above, and even a small number of items included are acceptable as long as the PFD can be specified.

[0026] This structure eliminates a fine tuning by a user or with a circuit and assures an optimal display of videos constantly on pixel displaying device 2.

[0027] In the embodiment discussed above, video-signal-output section 11 and video amplifier 6 are coupled by video-signal-cable 8, video-signal-input-terminal 7 and video-signal-output-terminal 9. However, video amplifier 6 can be directly connected to section 11.

[0028] Video-signal-data-output section 12 and microcomputer 41 are coupled by control-bus-cable 15, input/output terminal 13 of the first control bus and input/output terminal 14 of the second control bus; however, microcomputer 41 can be directly connected to section 12.

[0029] The display device of the present invention, as discussed above, comprises: the video signal processor for receiving an input video signal; and the pixel-converting-circuit for converting the pixels of an output signal from the video signal processor so that the display device can display the input video signal as an appropriate video on the pixel-displaying device. This structure allows the display device to display videos in the optimal condition because the exact PFD can be obtained. An exemplary pixel conversion method is described in U.S. Patent No. 5,933,196. Any method for pixel conversion, however, may be used.

[0030] To be more specific, the control bus transmits a request of transferring the PFD to the computer from the display device, and also transmits the PFD from the computer to the display device, so that the input-video-signal is free from erroneous recognition of its pixel format and can be displayed in the optimal condition constantly on the display device. As a result, a fine tuning for the video signal can be eliminated.

Claims

1. A display device comprising:

a video signal processor for receiving an input video signal and for generating an output video signal corresponding to said input video signal; and

a pixel-converting-circuit for converting a plurality of pixels included in saidoutput video signal, based upon pixel-format-data received via

a control bus independently of the input video signal.

2. The display device as defined in Claim 1 wherein the control bus transfers the pixel-format-data to said display device responsive to a request for the pixel-format-data from the display device.

3. A computer comprising:

a video-signal-outputting section for outputting a video signal to a display device; and

a video-signal-data-outputting section for outputting pixel-format-data corresponding to said video signal output from said video-signal-outputting section; and

a control bus for transmitting the pixel-format-data of the video signal to the display device and a request of transferring the pixel-format-data to a computer from the video display device.

4. A computer system comprising:

a video signal processor for receiving an input video signal and for generating an output video signal which corresponds to said input video signal;

a display device having a pixel-converting-circuit for converting a plurality of pixels of said output signal based upon pixel-format-data received via a control bus independently of the input video signal,

a video signal outputting section for outputting the output video signal to said display device;

a video-signal-data-outputting section for outputting said pixel-format-data; and

a computer having a control bus which transmits the pixel-format-data signal to said video display device.

5. The computer system as defined in Claim 4 wherein the control bus transmits the pixel-format-data to said display device and also transmits a request of transferring the pixel-format-data to said computer.

FIG. 1

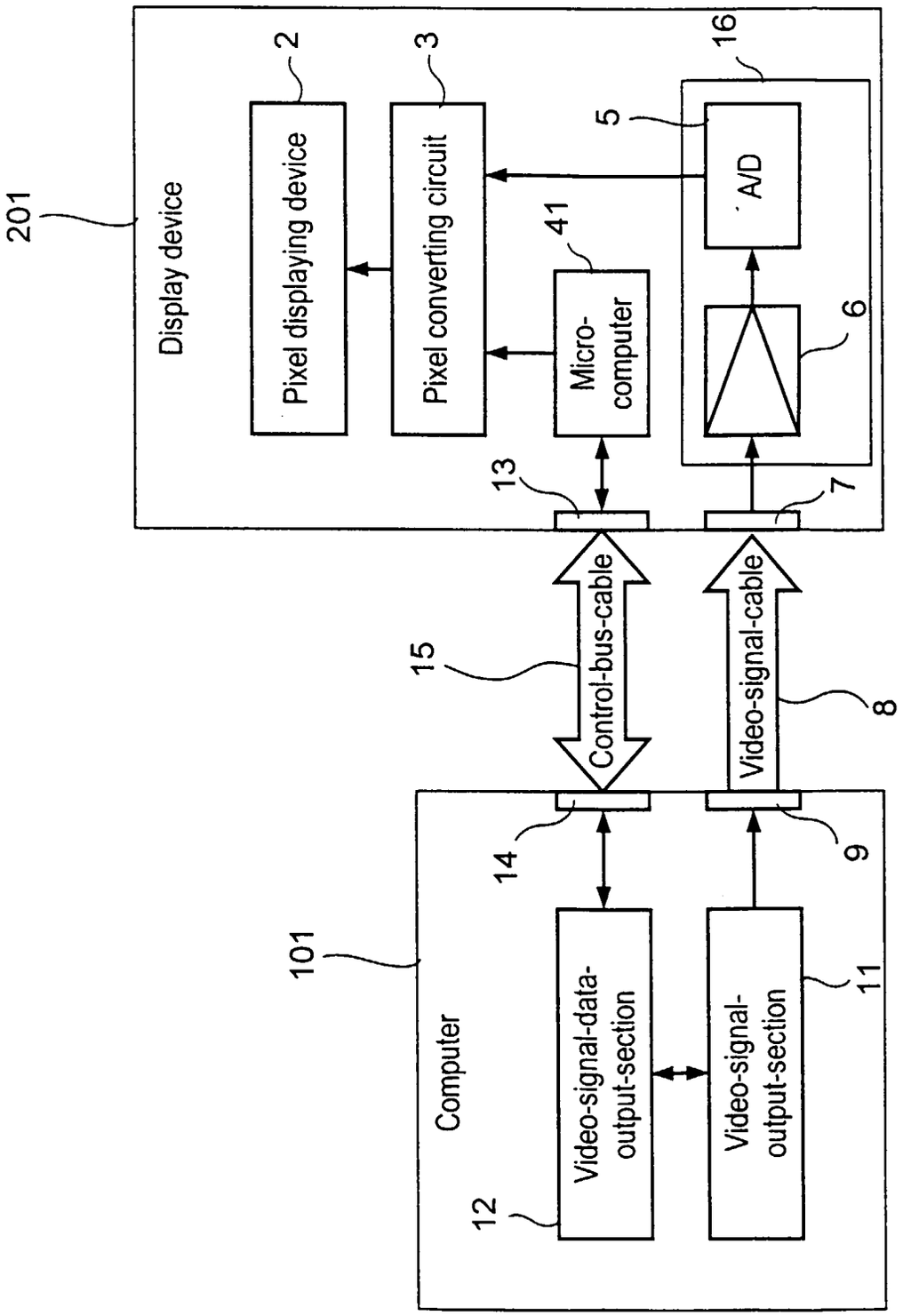
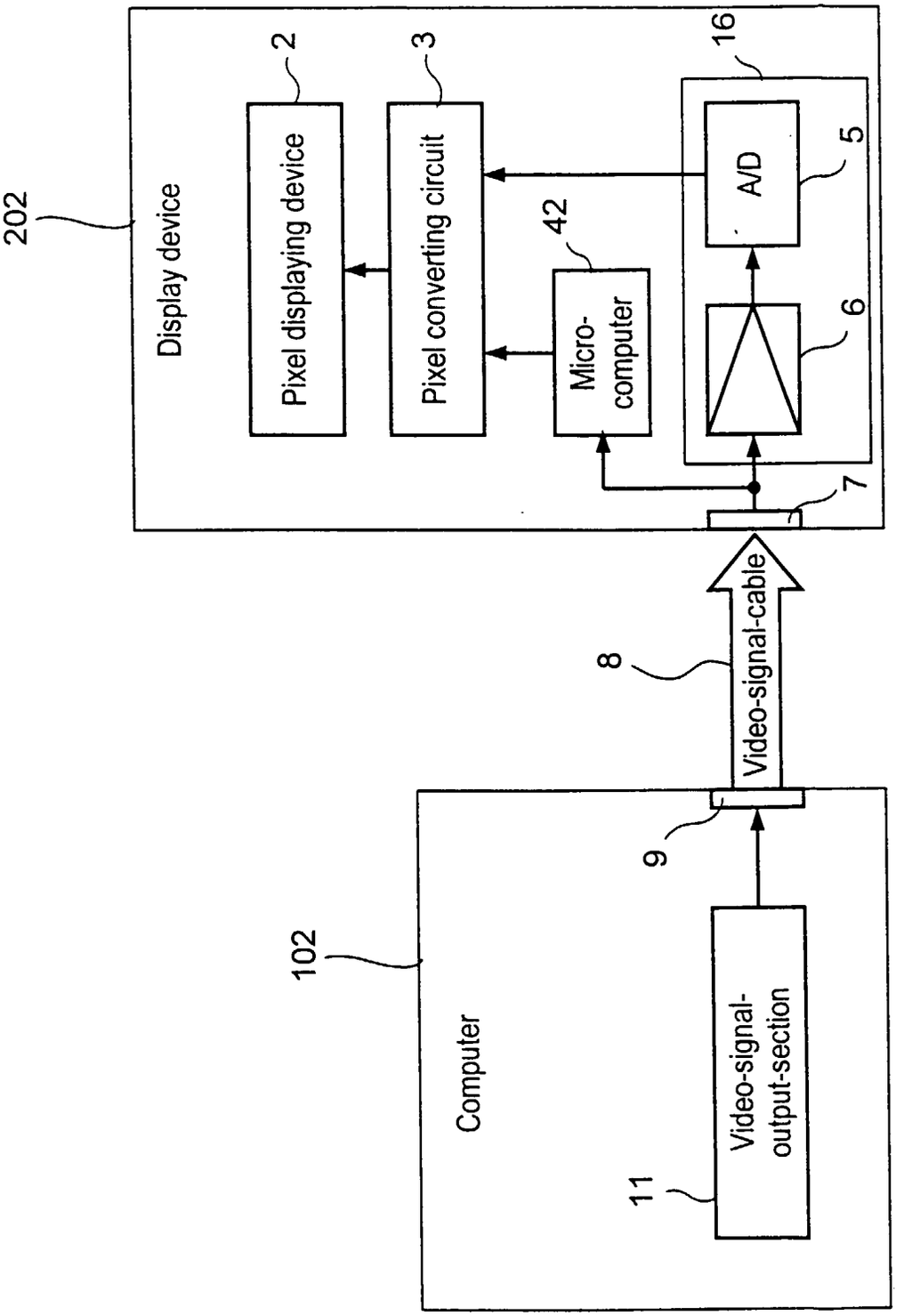

201
Display device
2
Pixel displaying device
3
Pixel converting circuit
41
Micro-computer
16
5
A/D
6
13
7
15
Control-bus-cable
Video-signal-cable
8
101
Computer
14
9
12
Video-signal-data-output-section
Video-signal-output-section
11

FIG. 2


202
Display device
2
Pixel displaying device
3
Pixel converting circuit
42
Micro-computer
16
A/D
5
6
7
8
Video-signal-cable
9
102
Computer
11
Video-signal-output-section