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(54) **Method of addressing a memory-effect display panel**

(57) The present invention relates to a method of addressing a memory-effect display panel comprising cells defined at the intersection of arrays of crossed electrodes, the cells having two states, one being the "written" state and the other the "erased" state, the method consisting, over a given cycle time, in applying a sustain signal to all the cells, the sustain signal producing a sus-

tain discharge in the cells in the written state, and in applying an address signal, comprising a semi-selective signal and a selective signal, in succession to the electrodes of one array, the semi-selective signal being applied simultaneously to different electrodes for at least part of the cycle time of the selective signal.

The invention applies to coplanar-type and matrix-type AC plasma display panels.

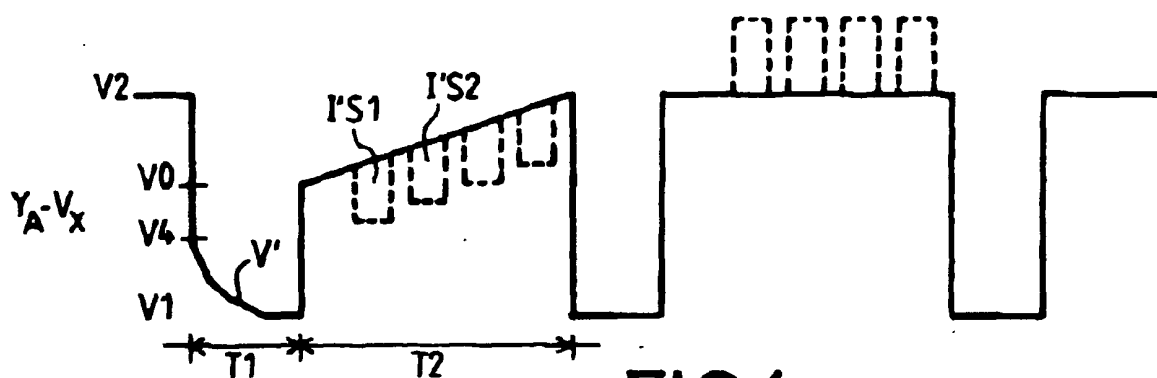


FIG.4

Description

[0001] The present invention relates to a method of addressing a memory-effect display panel, more particularly to a AC-type plasma display panel.

[0002] Plasma display panels, abbreviated to PDPs in the rest of the description, are flat display screens which use the emission of radiation in the visible or ultraviolet spectrum, this emission being obtained from a discharge in a gas.

[0003] PDPs form two large families:

- DC-type PDPs
- AC-type PDPs.

[0004] AC-type PDPs, because of their particular structure, benefit in their operation from an effect called the memory effect which makes them particularly suitable for forming large screens with a large number of elementary cells both for professional applications and for commercial applications, such as high-definition colour television.

[0005] The present invention relates to this type of PDP.

[0006] There are various types of AC-PDPs:

- so-called matrix PDPs which comprise only two arrays of crossed electrodes for defining the cells and for addressing and activating each cell. These PDPs are described in particular in French Patent No. 2,417,848;
- so-called coplanar PDPs which comprise an array of two so-called sustain electrodes on a first tile and an array of electrodes on a second tile which, with one of the sustain electrodes, define address electrodes, the cells being defined at the intersection of the two arrays. This type of PDP is described especially in European Patent EP-A-0,135,382.

[0007] The operation of AC or memory-effect PDPs generally includes an addressing function and a sustain function whose purpose is to produce the light energy. The sustain function consists in applying to a set of electrodes, in general to all the rows of the panel, an approximately squarewave alternating sustain signal whose purpose is to maintain each cell in the state to which it has been assigned previously by an address signal. This sustain signal generates a sustain discharge in the cells in the written state.

[0008] Addressing generally takes place by scanning the panel row by row. The cells of a selected row are driven simultaneously by a semi-selective operation, for example an erase operation, this operation being followed by a selective operation during which the cells of the row may then be written. The semi-selective operation followed by the selective operation is accomplished with a time shift from one row to another. Moreover, as is known, the semi-selective operation may be a write

operation and the selective operation may be an erase operation.

[0009] In an AC-type plasma display panel the discharge current is limited by a capacitor in series with each cell, in order to prevent the display panel from being destroyed if the source is not current-limited. The capacitor is generally produced by covering the electrode array with a dielectric layer, namely a borosilicate glass for example.

[0010] Erasing a cell therefore consists in removing the charges stored on the dielectric in the cells of the row in question. To erase, a voltage is generally applied to the electrode forming the corresponding row, this voltage causing a discharge whose intensity is chosen in such a way that the charges that are stored opposite it combine with one another so as to be cancelled out. Erasing a cell creates a discharge current whose intensity is approximately equal to half that of the sustain current, since about half the usual sustain charges are transferred.

[0011] At the present time, the selective erase operation is carried out in various ways.

[0012] According to one embodiment, called "shuffling", a matrix-type AC PDP receives an address signal of the type shown by the dotted lines in Figure 1, the signal shown as the solid line representing the gas-discharge voltage. In this case, all the row electrodes receive the sustain signal, shown as the broken line, simultaneously. This signal V_{ref} is approximately a squarewave with high extreme levels at a potential V_2 and low extreme levels at a potential V_1 which lie on either side of a mid-potential V_0 at which, in some cases, mid-levels (not shown in this embodiment) may be formed. The extreme levels are separated by rising and falling edges. The sustain signal V_{ref} causes sustain discharges in the cells in the written state. In the embodiment shown, the address signal superimposed on the sustain signal is applied to the electrodes of one array, each electrode in turn. For example, it may be applied to the row electrodes. However, it is conceivable that it is applied to the column electrodes. The address signal is decomposed into a semi-selective signal and a selective signal. The semi-selective signal is, for example, the erase signal while the selective signal is the write signal. However, as known by those skilled in the art, the semi-selective and selective signals may be reversed.

[0013] As shown in Figure 1, the selective write signal consists of a pulse referenced IE which is superimposed on the high level of the sustain signal. The semi-selective erase signal consists of an erase pulse IR generated from a low level of the sustain signal. The erase pulse IR generates an erase discharge at all the cells in the written state of the selected row and replaces the one which should have been generated by the sustain signal. The erase pulse IR may last until the next rising edge of the sustain signal or may be shorter. It is usual in the case of matrix-type AC colour PDPs to apply several write pulses which are superimposed on the high

level of the sustain signal. With this type of addressing, called "multiple pulse" addressing, the duration of the high level must be long enough, which means reducing the duration of the low level in order not to extend the address cycle time. This reduces the time during which the erasing is carried out since, at the present time, the erase pulse is generated from a low level. However, if the erase time is too short the charges stored at the terminals of the dielectric are not completely removed.

[0014] The object of the present invention is to remedy the abovementioned drawback by providing an addressing method which makes it possible to remove the charges as fully as possible during erasure for AC plasma display panels both of the matrix type and of the coplanar type.

[0015] The subject of the present invention is a method of addressing a memory-effect display panel comprising cells defined at the intersection of arrays of crossed electrodes, the cells having two states, one being the "written" state and the other the "erased" state, the process consisting, over a given cycle time, in applying a sustain signal to all the cells, the sustain signal producing a sustain discharge at the cells in the written state, and in applying an address signal, comprising a semi-selective signal and a selective signal, in succession to the electrodes on one array, characterized in that the semi-selective signal is applied simultaneously to different electrodes for at least part of the cycle time of the selective signal.

[0016] According to one embodiment, with addressing while displaying, in which the sustain signal is a squarewave signal having at least two extreme levels on either side of a mid-potential, the semi-selective signal is applied over at least part of the extreme level of the sustain signal to which the selective signal is also applied. The semi-selective signal is applied during the high level or the low level of the squarewave sustain signal and consists of a signal portion having a rising or falling slope, this portion starting at an intermediate potential between the mid-potential and the potential of the extreme level and terminating at the extreme level. In this case, since the pulses of the multiple-pulse selective signal are superimposed on the slope of the semi-selective signal, for example the erase signal, a succession of short erase pulses is obtained, the amplitude of which is controlled according to this slope. Consequently, the cells receive a succession of discharges with progressively varying voltage. This characteristic associated with a long discharge time makes it possible to obtain good erasure of the cells whatever the structural homogeneity of the said cells.

[0017] Preferably, the pulses associated with the selective signal are adjustable in terms of width, these having fixed or variable widths which may be between 0.5 μ s and less than 10 μ s, typically about 1.5 μ s, and the spacing of which is also adjustable within this order of magnitude.

[0018] According to another characteristic of this em-

bodiment, a semi-selective signal is applied during the other extreme level of the sustain signal. This signal has the waveform of the semi-selective address signal described in French Patent Application No. 96/01060 in the name of THOMSON-CSF, the content of which is included in the present application.

[0019] Further features and advantages of the present invention will appear upon reading the description given below of various embodiments, this description referring to the drawings appended hereto and in which:

- Figure 1, already described, shows a timing diagram for the address and sustain signals applied to a row of a plasma display panel of the MAC PDP type according to the prior art;
- Figure 2 shows schematically the structure of a plasma display panel of the MAC PDP type to which a first embodiment of the method of the present invention applies;
- Figures 3a and 3b show timing diagrams for the address and sustain signals according to the present invention, applied to the PDP in Figure 2;
- Figure 4 shows a timing diagram for the address and sustain signals according to a variant of the Present invention;
- Figure 5 is a schematic representation of a coplanar PDP to which the method of the present invention may be applied; and
- Figure 6 shows the timing diagrams for the address and sustain signals according to the invention, applied to the electrodes of the PDP in Figure 5.

[0020] To simplify the description, in the figures the same elements bear the same references.

[0021] A first embodiment of an image display device to which the method of the present invention applies will firstly be described with reference to Figure 2. This display device comprises a matrix-type plasma display panel or PDP1 and means for driving this panel.

[0022] The matrix-type plasma display panel PDP1 comprises a first array of row electrodes Y1 to Y4 which intersects a second array of column electrodes X1 to X5. A plasma cell C corresponds to each electrode intersection, these cells being arranged in a matrix configuration. In matrix-type PDPs, the sustain and address signals are applied between the row-electrode array and the column-electrode array.

[0023] Thus, as shown in Figure 2, each row electrode Y1 to Y4 is connected to a row-address circuit or row driver, RD. For large panels, there are generally several row drivers, each supplying a group of rows with sustain and address signals. Likewise, each column electrode X1 to X5 is connected to a column-address circuit or column driver, CD. The column drivers generate pulses which mask those generated by the semi-selective write address signal on a selected row in the cells C, this row not having to be written, as will be explained below.

[0024] As shown in Figure 2, the row driver RD receives the sustain signal from a sustain signal generator SSG. This sustain signal consists of a squarewave signal between two extreme voltage levels V1 and V2, having a low level of duration T1 and a high level of duration T2, the time T1 being less than the time T2 in the embodiment shown. The row driver RD also receives the address signal, which is superimposed on the sustain signal, from a row address signal generator RASG.

[0025] In the embodiment shown in Figure 2, the operation of the row driver RD is shown symbolically by switches I1, I2, I3, I4 which can switch between the line RSS supplying the sustain signal and the line RAS supplying the address signal. The state of the switches is controlled by a signal SC coming from a scan generator (not shown). In Figure 2, the switches I1, I2, I4 are positioned so as to receive the signal RSS, so that the rows Y1, Y2, Y4 are in sustain mode. On the other hand, the switch I3 is switched so as to receive the address signal RAS formed from selective and semi-selective signals, in such a way that the row Y3 is the row addressed.

[0026] As shown in Figure 2, the column driver CD also consists schematically of switches I'1, I'2, I'3, I'4, I'5. These switches may receive an address signal CAS coming from a column address signal generator CASG, or may be earthed as shown by the line M. The state of the switches I'1 to I'5 is controlled by a signal V corresponding to the video content of the row addressed. In the embodiment shown, the switches I'1, I'2, I'5 are earthed so that the cells lying at the intersections between the row Y3 and the columns X1, X2, X5 are in the "on" state shown symbolically by a "*" whereas the switches I'3 and I'4 are connected so as to receive the column address signal CAS from the column address signal generator CASG so that the cells C lying at the intersections between the row Y3 and the columns X3, X4 are in the "off" state shown symbolically by an "O". The cells of the other rows are in the sustained state as shown symbolically by an "S".

[0027] The waveform of the address and sustain signals according to the present invention, which are applied to a matrix-type PDP as shown in Figure 2, will now be described with reference to Figures 3a and 3b. The addressing described with reference to Figures 3a and 3b will be "multiple pulse" addressing. However, it is obvious to a person skilled in the art that the present invention may also apply to single-pulse addressing. In this case, the sustain signals applied to the rows Y_A therefore consist of squarewaves having a low level of duration T1 at a voltage V1 followed by a high level of duration T2 at a voltage V2. The sustain signal shown does not have an intermediate level at the mean voltage V0 but the present invention could also apply to sustain signals having this intermediate level, as described in Patent Application No. 96/01060 filed in the name of THOMSON-CSF. In a known manner, an address signal may be superimposed on this sustain signal, the address signal being of the type consisting of a semi-se-

lective signal which, in the embodiment shown, is an erase signal, and of a selective signal which, in the embodiment shown, is a write signal.

[0028] According to the present invention, the semi-selective erase signal consists of a signal applied during the high level of the sustain signal, namely during the period T2, that is to say during the same cycle time as that receiving the selective write signal.

[0029] As shown in Figure 3a, this semi-selective erase signal consists of a rising ramp r which starts from a voltage V3 slightly above the intermediate voltage V0 and rises up to the voltage V2 of the high level.

[0030] As shown in Figure 3a, during the time T2, which also corresponds to the selective address time, the column driver CD sends the selected columns pulses IS1, IS2, etc., as shown by V_X . Thus, in a matrix PDP, a signal $Y_A - V_X$ as shown in Figure 3b will be obtained at the terminals of the addressed cells. During the erase period, what is obtained is not a continuous slope but, randomly, a succession of short erase pulses I'S1, I'S2, etc., having an amplitude controlled according to the slope r . The cells are therefore treated with a succession of discharges at a progressively varying voltage. This type of erase discharge makes it possible to cover the various cases of structural homogeneity of the cells and lasts long enough for the discharges to be stabilized before the next sustain pulse.

[0031] Figure 3b shows that, after the erase period P, a multiple-pulse write period P' of known type is obtained. The pulses I'S1, I'S2 have been shown with a constant width. However, it is obvious to those skilled in the art that they may have a varying width, especially a width of between 0.5 μ s and less than 10 μ s, typically 1.5 μ s. In addition, the spacing between the pulses may also be adjusted within the same order of magnitude.

[0032] Figure 4 shows another embodiment of the present invention, in which, added to the long erasure described above is a short erase pulse during the period T1 of the sustain pulse, this erase pulse being of the type described in French Patent Application No. 96/01060 (THOMSON-CSF).

[0033] In the embodiment shown in Figure 4, the semi-selective address signal in erase mode includes a signal part V' whose slope decreases over the low level V1 of the sustain signal, this part starting at an intermediate potential referenced V4 with respect to the potential V1 of the low level, which is between the potential V1 of the low level and the mid-potential V0, and terminating approximately at the potential V1 of the low level. This conventional erase signal is followed by a semi-selective address signal in erase mode of the type described with reference to Figures 3a and 3b. It is obvious to those skilled in the art that the semi-selective address signal in erase mode may be given other waveforms, such as those described in the abovementioned patent application.

[0034] Another embodiment of the present invention, applicable more particularly to coplanar-type plasma

display panels, will now be described with reference to Figures 5 and 6.

[0035] As shown in Figure 5, a coplanar-type PDP comprises a screen formed from a set of two parallel arrays of electrodes Ys1...YsN, and Y's1...Y'sN, called row electrodes, which are crossed with a second array of electrodes X'1 to X'N, called column electrodes. A cell Ce, which is bounded by barriers B, corresponds to each intersection of row and column electrodes. In the case of a coplanar PDP, the two parallel arrays of row electrodes constitute sustain electrodes between which the sustain signals are applied, whereas the address signals are applied between one row-electrode array and the column-electrode array.

[0036] As shown in Figure 6, according to the present invention the array of sustain electrodes Ys1 to YsN receives low-level squarewave pulses of duration T'1 followed by a high level 2 of duration T'2, the latter duration with corresponding to the time needed for a selective write operation, followed by a pulse of duration T'3 and again a low level with duration T'1. The combination of durations T'1, T'2 and T'3 corresponds to a base cycle.

[0037] According to the present invention and as shown in Figure 6 by Y's, the second array of sustain electrodes Y's1 to Y'sN receives address pulses which, according to the present invention, comprise, during the first high level of duration T'2, an erase signal Ve of slightly shorter duration than T'2 but which lasts longer than the duration T'1 during which the erase signal is normally applied. Between the two parallel arrays of row electrodes Ys1 to YsN and Y's1 to Y'sN, a signal as shown by Y's - Ys in Figure 6 is therefore obtained. During a period T'2, different from the base cycle, a selective write signal is applied, giving the pulse Ie. The array of electrodes X' receives, in a known manner, the pulses IS'1...IS'n. Thus, with the present invention, the duration T'1 may be shortened significantly compared with the conventional duration, since this time is no longer used for erasing. Consequently, the base cycle is also shortened.

[0038] Indeed, the generation of the signals allowing the present invention to be implemented entails certain constraints owing to the fact that the semi-selective erase signal has, especially in the case of matrix-type AC plasma display panels, a voltage value which is the inverse of that of the selective write signal. This requires high-voltage drivers operating at both positive voltages and negative voltages. One solution allowing easy implementation of the present invention consists in using one amplifier per driver circuit and in integrating this semi-selective erase signal into the sustain signal. The same type of constraint also applies to a coplanar-type plasma display panel.

Claims

1. A method of addressing a memory-effect display

panel comprising cells defined at the intersection of arrays of crossed electrodes, the cells having two states, one being the "written" state and the other the "erased" state, the method consisting, over a given cycle time, in applying a sustain signal to all the cells, the sustain signal producing a sustain discharge in the cells in the written state, and in applying an address signal, comprising a semi-selective signal and a selective signal, in succession to the electrodes of one array, characterized in that the semi-selective signal is applied simultaneously to different electrodes for at least part of the cycle time of the selective signal.

2. Method according to Claim 1, characterized in that, in the case of addressing while displaying, with a sustain signal consisting of a squarewave signal having at least two extreme levels on either side of a mid-potential, the semi-selective signal is applied over at least part of the extreme level of the sustain signal to which the selective signal is also applied.
3. Method according to Claim 2, characterized in that the semi-selective signal is applied during the high level or the low level of the squarewave sustain signal.
4. Method according to either of Claims 2 and 3, characterized in that the semi-selective signal consists of a signal portion having a rising slope, this portion starting at an intermediate potential between the mid-potential and the potential of the extreme level, and terminating at the extreme level.
5. Method according to any one of Claims 1 to 4, characterized in that the semi-selective signal obtained in the cells forms a succession of pulses whose amplitude progressively varies.
6. Method according to Claim 5, characterized in that the pulses have varying widths of about 0.5 μ s to less than 10 μ s.
7. Method according to any one of the preceding claims, characterized in that an additional selective signal is applied during the other extreme level of the sustain signal.
8. Method according to any one of the preceding claims, characterized in that it applies to matrix-type AC plasma display panels.
9. Method according to any one of Claims 1 to 7, characterized in that it applies to coplanar-type AC plasma display panels.

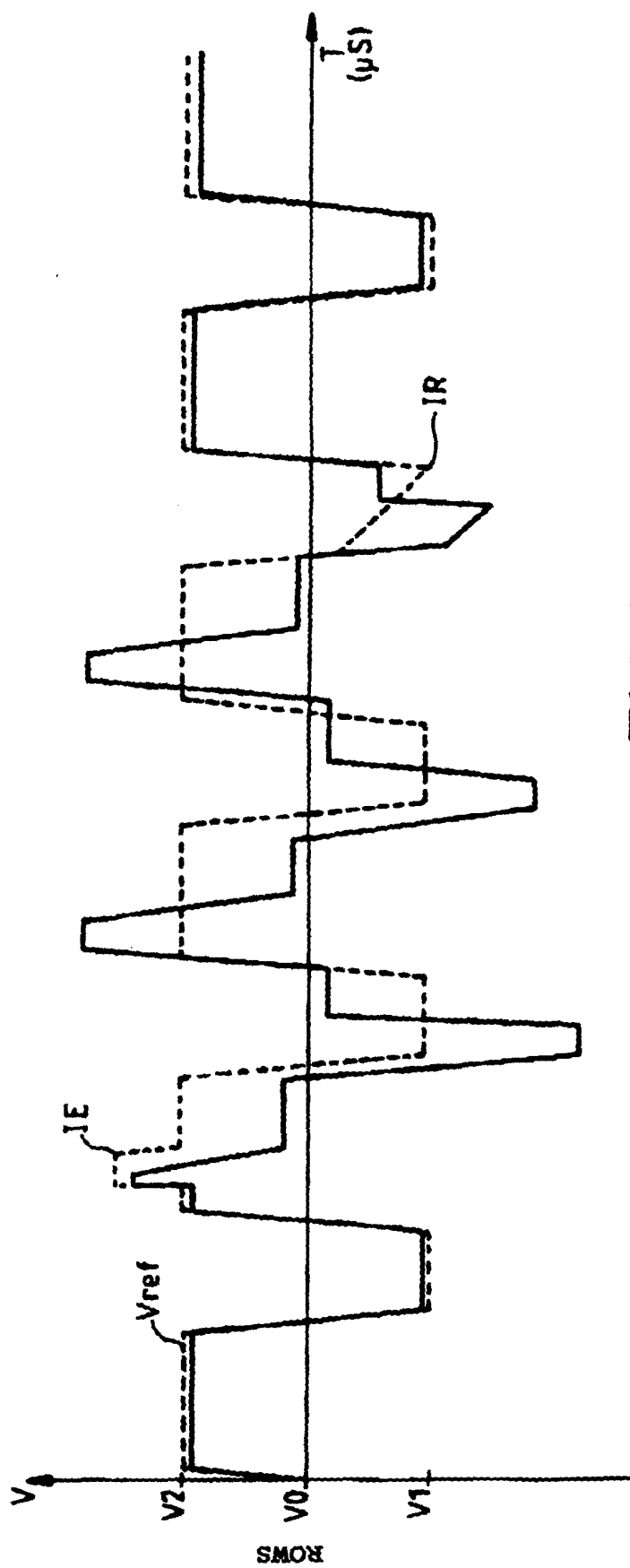


FIG.1

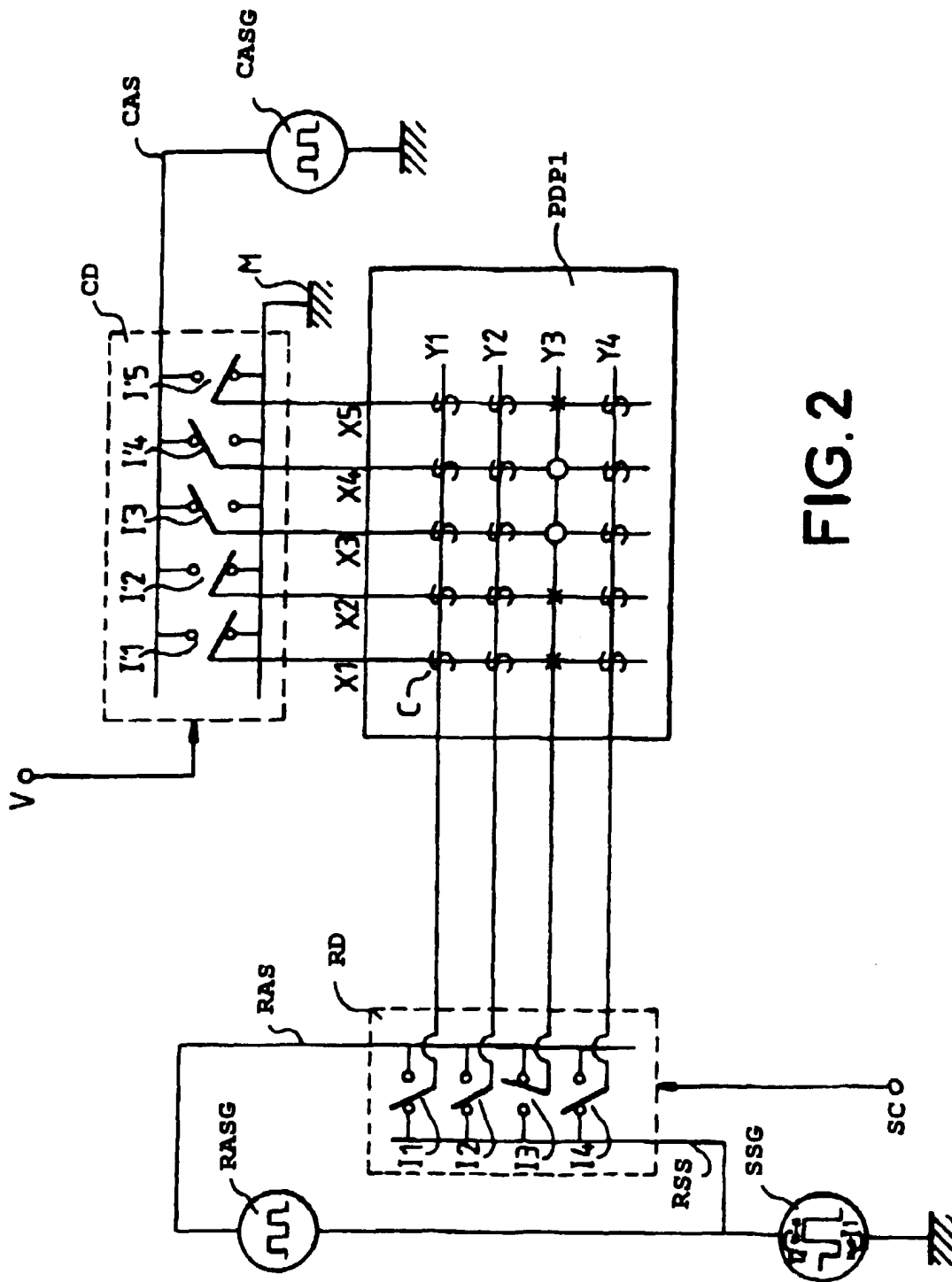


FIG. 2

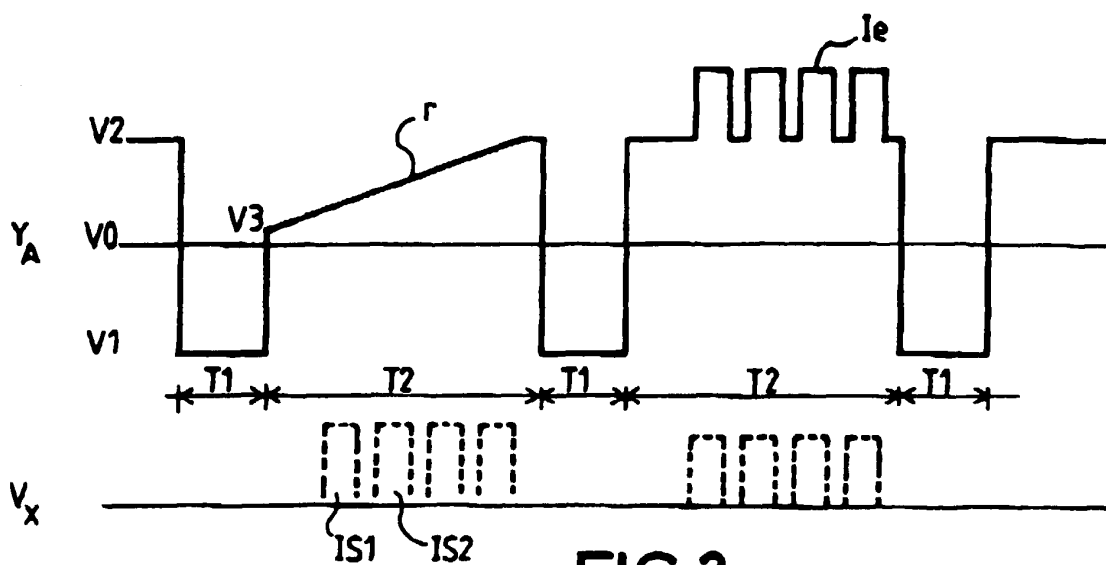


FIG. 3a

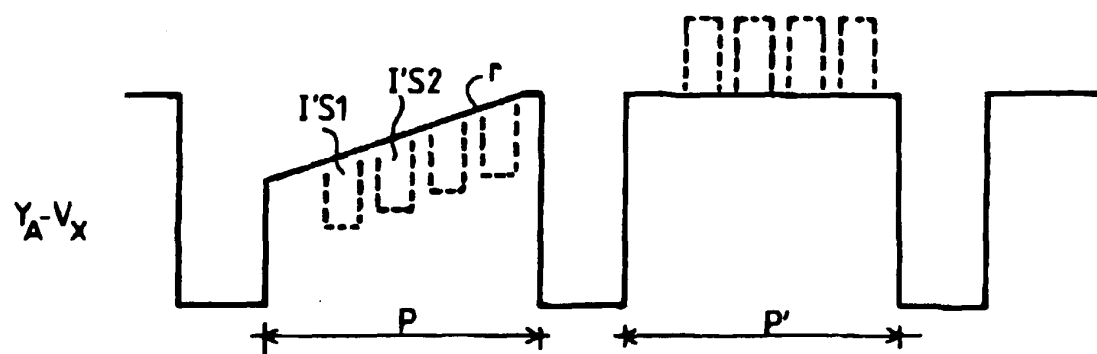


FIG. 3b

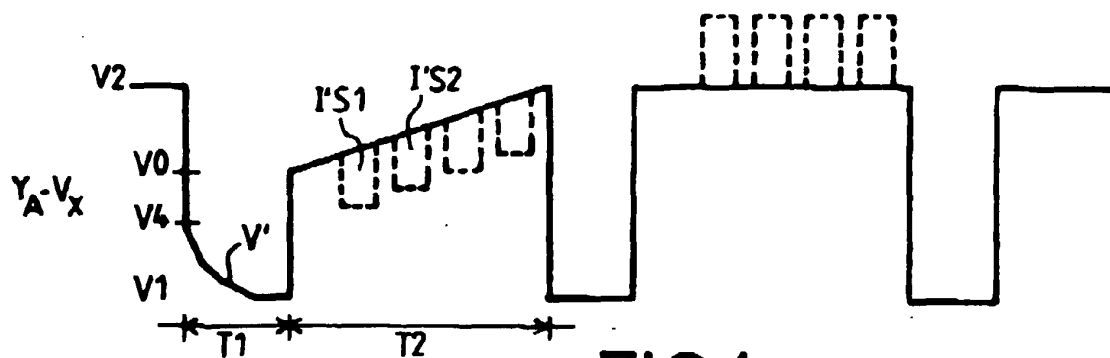


FIG. 4

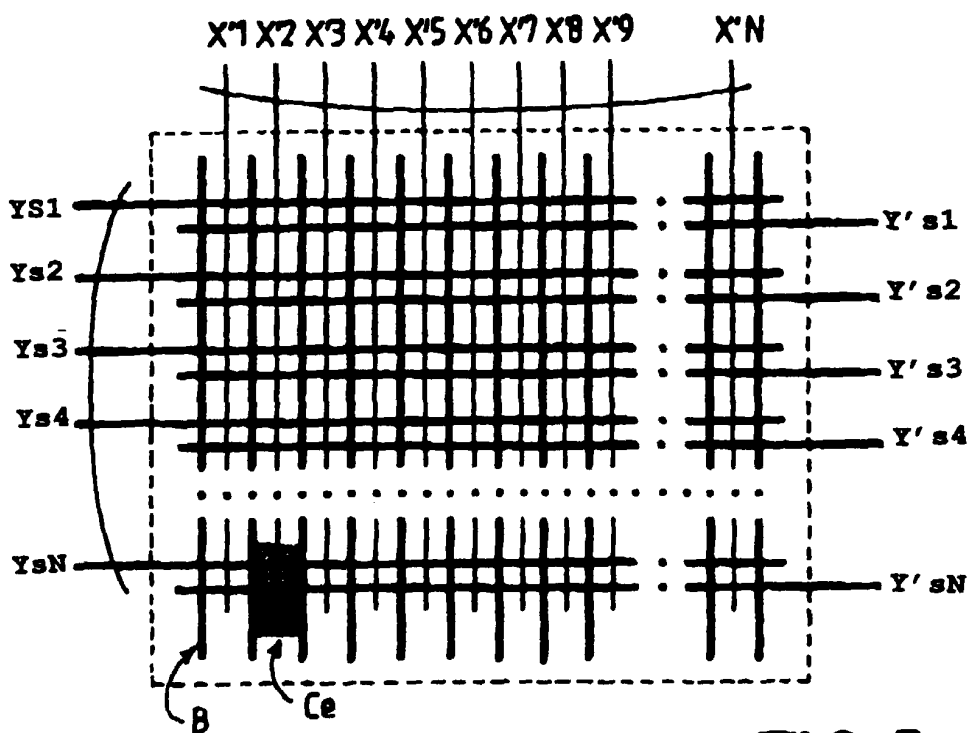


FIG. 5

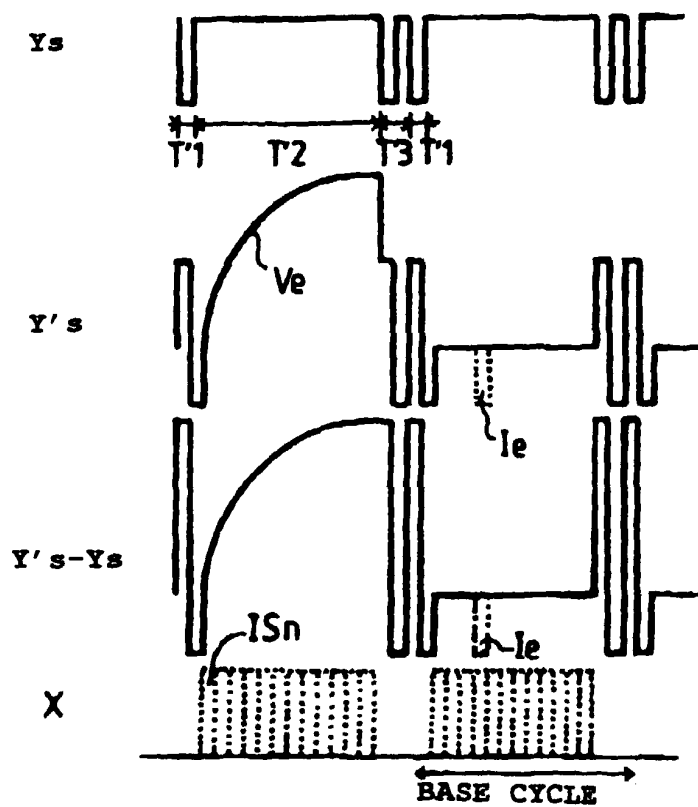


FIG. 6



European Patent
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EUROPEAN SEARCH REPORT

Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT			
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
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