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Flüssigkristallanzeige

Dispositif d'affichage à cristaux liquides

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Description**BACKGROUND OF THE INVENTION****Field of the Invention**

[0001] The present invention relates to a liquid crystal display and, more particularly, to a driver of liquid crystal display, in which the driving signal applied to the two scanning lines adjacent to each other is controlled to allow one data line to send two video signal to both pixels, respectively, thereby reducing the number of the data lines by half in comparison with the conventional liquid crystal display.

Discussion of Related Art

[0002] A liquid crystal display generally consists of upper and lower plates and a liquid crystal being sealed between the two plates. The upper plate has a black matrix, a common electrode and R, G, and B color filter layers for displaying colors formed thereon. On the lower plate, data lines and gate lines are arranged, intersecting each other, to form pixel regions in matrix form. Each of the pixel regions includes one thin film transistor and one pixel electrode.

[0003] FIG. 1 is a cross-sectional view of a general liquid crystal display. Referring to FIG. 1, thin film transistors each of which consists of a gate electrode extended from a scanning line (gate line), source and drain electrodes S and D extended from a data line are arranged in matrix form on a lower plate 1, having a predetermined distance. A pixel electrode 2a connected to the drain electrode D of each thin film transistor 2 is formed in each pixel region. An upper plate 3 has black matrix layers 4 formed thereon in mesh form, for blocking light transmitted to regions other than the pixel region 2a. R, G, B color filters 5 for displaying colors are formed between the black matrix layers 4. A common electrode 6 is formed on the color filters 5 and black matrix layers 4.

[0004] FIG. 2 shows the configuration of the general conventional liquid crystal display. Referring to FIG. 2, the liquid crystal display includes a display panel part 21 consisting of the upper and lower plates and the liquid crystal sealed therebetween to display images, a gate driver part 22 consisting of gate drivers GD each of which applies a driving signal to the panel part 21 in row direction, and a source driver part 23 consisting of source drivers SD each of which supplied a driving signal to the panel part 21 in column direction.

[0005] There is explained below a conventional liquid crystal display and a circuit for driving the same with reference to the attached drawings. FIG. 3 shows the configuration of the conventional liquid crystal display. Referring to FIG. 3, a plurality of scanning lines G1, G2, ..., Gn-1, Gn are arranged in row direction, having a predetermined distance, and a plurality of data lines D1, D2, ..., Dn-1, Dn are arranged, intersecting the scanning lines.

A thin film transistor T1 is formed at the portion where each scanning line intersects each data line intersect. A pixel electrode C_{lc} is connected to each thin film transistor T1. Accordingly, a driving voltage is sequentially applied to the scanning lines to turn on the thin film transistors, and signal voltages of corresponding data lines are charged into the pixel electrodes through the turned-on thin film transistors.

[0006] FIG. 4 shows the waveform of a driving signal applied to the scanning lines of the conventional liquid crystal display. Referring to FIG. 4, the driving signal is sequentially applied to the scanning lines, starting from the first one G1 to the nth one Gn during one frame, and the signal voltages of corresponding data lines are delivered to the pixel electrodes through the thin film transistors turned on by corresponding scanning lines, to thereby display an image.

[0007] FIG. 5A shows the configuration of the source driver of the conventional liquid crystal display, and FIG. 5B shows the operation waveforms of the source driver. The source driver shown in FIG. 5A is 384-channel 6-bit driver. That is, it has R, G, and B data items each of which is 6-bit and the number of its column lines is 384. Referring to FIG. 5A, the source driver includes a shift register 51, a sampling latch 52, a holding latch 53, a digital/analog (D/A) converter 54, and an amplifier 55. The shift register 51 shifts a horizontal synchronous signal pulse HSYNC depending on a source pulse clock HCLK, to output a latch clock to the sampling latch 52. The sampling latch 52 samples and latches the digital R, G, and B data items by column lines according to the latch clock supplied by the shift register 51.

[0008] The holding latch 53 receives and latches the R, G, and B data items, simultaneously, latched by the sampling latch 52 in response to a load signal LD. The D/A converter 54 converts the digital R, G, B data stored in the holding latch 53 into analog R, G, and B data signals. The amplifier 55 amplifies the currents of the analog R, G, and B data signals and sends them to the data lines. That is, the digital R, G, and B data is sampled and held, converted into the analog R, G, and B data, and then current-amplified to be outputted. Here, if the holding latch 53 holds the R, G, and B data corresponding to the nth row line, the sampling latch 52 samples the R, G, and B data of the (n+1)th row line.

[0009] FIG. 6A shows the configuration of the gate driver of the conventional liquid crystal display, and FIG. 6B shows the input and output waveforms of the gate driver. Referring to FIG. 6A, the gate driver consists of a shift register 61, a level shifter 62, and an output buffer 63. The shift register 61 shifts a vertical synchronous signal pulse VSYNC depending on a gate pulse clock VCLK, to sequentially enable the scanning lines. The level shifter 62 sequentially level-shifts a signal applied to the scanning lines, to output it to the output buffer 63. Accordingly, the plurality of scanning lines connected to the output buffer 63 are sequentially enabled.

[0010] In the conventional liquid crystal display, as de-

scribed above, the driving voltage is sequentially applied to the scanning lines to turn on or off the thin film transistors each of which is connected to each data line, and signal voltages of corresponding pixel regions through the turned on thin film transistors, to thereby display an image.

[0011] However, the aforementioned conventional liquid crystal display has the following problem. In case where the number of pixels increases in order to realize a large-sized liquid crystal display with a higher resolution, the number and the size of its drivers also increase to raise the cost. This brings about a new problem such as connection between the drivers and panel.

[0012] US5,856,816 discloses a data driver including a first signal generating circuit for externally producing a start signal, a second signal generating circuit for externally producing a first clock signal, a third signal generating circuit for externally producing a load signal, a generator externally generating a source video signal having a frequency, and a single integrated circuit including a m-bit register circuit for receiving the start signal corresponding to the first clock signal and outputting a latch clock signal. A data latch circuit is provided for latching and outputting at least two sets of three video signals corresponding to the source video signal.

[0013] JP 02 168229 discloses a driving system for a liquid crystal display device that comprises two sample hold circuits. Switches are provided so as to provide each data line with the output of one of the sample hold circuits.

[0014] JP 02 087190 discloses a driving system for a display device. In this arrangement, first and second sample hold circuits are provided, with switches to provide a data line with an output from either of the sample and hold circuits.

[0015] JP 05265045 discloses an active matrix liquid crystal display with reduced production cost due to a reduced number of data electrodes by connecting each data line via switches to two adjacent columns of pixels.

SUMMARY OF THE INVENTION

[0016] Accordingly, the present invention is directed to a liquid crystal display that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

[0017] An object of the present invention is to provide a liquid crystal display, which is able to display images with the same resolution as that of the conventional liquid crystal display while its data lines are as many as half the number of the data lines of the conventional one, resulting in cost reduction.

[0018] To accomplish the object of the present invention, there can be provided a liquid crystal display having first and second plates and a liquid crystal being sealed therebetween, including: a plurality of scanning lines arranged on the first plate in one direction; a plurality of data lines arranged on the first plate, intersecting the scanning lines; first and second pixel regions, located at

both sides of each data line, respectively; a first switch for selectively transmitting a video signal loaded on a corresponding data line to the first pixel region; and a second switch for selectively transmitting the video signal loaded on the data line to the second pixel region.

[0019] According to an aspect of the invention there is provided a liquid crystal display as set out in Claim 1. Preferred features of this aspect are set out in Claims 2, 3, 4, and 5.

[0020] there can also be provided a gate driver for driving the liquid crystal display, which includes: a shift register for shifting a starting pulse depending on a gate pulse clock; a logic circuit for selectively receives a plurality of output signals of the shift register, logically operating them and outputting them; a level shifter for shifting the output of the logic circuit to a predetermined level, to sequentially output it; and an output buffer for sequentially applying the level-shifted signal to scanning lines.

[0021] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

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[0022] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention:

[0023] In the drawings:

35 FIG. 1 is a cross-sectional view of a general liquid crystal display;
FIG. 2 roughly shows the configuration of the general liquid crystal display;
FIG. 3 shows the configuration of a conventional liquid crystal display;
FIG. 4 shows the waveform of a driving signal applied to the scanning lines of the conventional liquid crystal display;
40 FIG. 5A shows the configuration of the source driver of the conventional liquid crystal display;
FIG. 5B shows the operation waveforms of the source driver of the conventional liquid crystal display;
FIG. 6A shows the configuration of the gate driver of the conventional liquid crystal display;
FIG. 6B shows the operation waveforms of the gate driver of the conventional liquid crystal display;
45 FIG. 7A shows the configuration of a liquid crystal display according to a first embodiment of the present invention;
FIG. 7B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 7A;

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FIG. 8A shows the configuration of a liquid crystal display according to a second embodiment of the present invention;

FIG. 8B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 8A;

FIG. 9A shows the configuration of a liquid crystal display according to a third embodiment of the present invention;

FIG. 9B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 9A;

FIG. 10A shows the configuration of a liquid crystal display according to a fourth embodiment of the present invention;

FIG. 10B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 10A;

FIG. 11A shows the configuration of a liquid crystal display according to a fifth embodiment of the present invention;

FIG. 11B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 11A;

FIG. 12A shows the configuration of a liquid crystal display according to a sixth embodiment of the present invention;

FIG. 12B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 12A;

FIG. 13A shows the configuration of a liquid crystal display according to a seventh embodiment of the present invention;

FIG. 13B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 13A;

FIG. 14A shows the configuration of a liquid crystal display according to an eighth embodiment of the present invention;

FIG. 14B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 14A;

FIG. 15A shows the configuration of the source driver of the liquid crystal display according to the present invention;

FIG. 15B shows the operation waveforms of the source driver of FIG. 15A;

FIG. 16A shows another embodiment of the source driver of the liquid crystal display of the present invention;

FIG. 16B shows the operation waveforms of the source driver of FIG. 16A;

FIG. 17A shows the configuration of the gate driver of the liquid crystal display according to the present invention;

FIG. 17B shows the operation waveforms of the gate driver of FIG. 17A; and

FIG. 18 shows a video signal writing order and the

polarities of image signals according to the liquid crystal display of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0024] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0025] A liquid crystal display according to the present invention is characterized in that a driving signal applied to neighboring two scanning lines is controlled to allow one data line to send a video signal to pixel regions placed at both sides thereof, resulting in reduction in the number of the data lines.

[0026] FIG. 7A shows the configuration of a liquid crystal display according to a first embodiment of the present invention. Referring to FIG. 7A, a plurality of scanning lines G1, G2, ..., Gn-1, Gn are arranged in row direction whereas a plurality of data lines D1, D2, ..., Dn-1, Dn are arranged in column direction, intersecting the scanning lines. At the portion where each scanning line intersects each data line, first and second switches 71 and 73 transmitting a video signal are located at pixel regions placed on the left and right hands of the data line, respectively. First and second pixel electrodes 71c and 73c are respectively connected to the first and second switches 71 and 73. Here, each of the first and second switches is preferably configured of an N-type or P-type thin film transistor.

[0027] The configuration of the liquid crystal display of the present invention is described below in more detail with reference to the portion "X" of FIG. 7A. The first switch 71 located at the left side of a data line D1 includes a first thin film transistor 71a whose source or drain is connected to the data line D1 and whose gate is connected to a corresponding scanning line G1, and a second thin film transistor 71b whose gate is connected to the next scanning line G2, the second thin film transistor 71b being serially connected to the first thin film transistor 71a. The second thin film transistor 71b is connected to the first pixel electrode 71c so that a video signal is selectively delivered to the first pixel electrode according to ON/OFF operation of the first and second thin film transistors 71a and 71b.

[0028] The second switch 73 located at the right side of the data line D1 includes a third thin film transistor 73a whose gate is connected to the corresponding scanning line G1 and whose source or drain is connected to the drain line D1, and a fourth thin film transistor 73b whose gate is connected to the corresponding scanning line G1, the fourth thin film transistor 73b being serially connected to the third thin film transistor 73a. Here, the second switch 73 may be configured of only the third thin film transistor 73a.

[0029] In the liquid crystal display according to the first embodiment of the present invention, constructed as above, the procedure of transmitting a video signal to the

first and second pixel electrodes is explained below with reference to the waveforms shown in FIG. 7B. FIG. 7B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display according to the first embodiment of the present invention.

[0030] Referring to FIG. 7B, with one horizontal period being divided into two sections (a) and (b), the video signal is applied to both of the pixels located at the left and right sides of the data line D1 during the first section (a), and it is applied to only the right pixel during the second section (b). That is, the first scanning line G1 receives a 'high' signal during the single horizontal period, and the second scanning line G2 receives the 'high' signal only during the first half horizontal period (it may not be exact one half), i.e., section (a), and receives a 'low' signal during the second half horizontal period, i.e., second (b).

[0031] Accordingly, when both of the first scanning line G1 and second scanning line G2 are at the 'high' state, the first and second thin film transistors 71a and 71b of the first switch 71 and the third and fourth thin film transistors 73a and 73b of the second switch 73 are all turned on, to deliver the video signal to the first and second electrodes 71c and 73c. Thereafter, upon application of the 'low' signal to the second scanning line G2, the second thin film transistor 71b is turned off so that the video signal is not transmitted to the first pixel electrode 71c, being delivered to only the second pixel electrode 73c.

[0032] With one horizontal period being divided into two sections (a) and (b), as described above, the video signal loaded on one data line can be selectively delivered to the left and right pixel electrodes. Consequently, the driving signal applied to the scanning lines is controlled to allow one data line to send a video signal to its left and right pixels, thereby reducing the number of the data lines by half in comparison with the conventional liquid crystal display. This also decreases the number of the source drivers by half. FIG. 8A shows the configuration of a liquid crystal display according to a second embodiment of the present invention. Referring to FIG. 8A, the liquid crystal display of this embodiment has a difference from the first embodiment in the connection points of the gates of the first and second thin film transistors 71a and 71b constructing the first switch 71. Specifically, the first switch 71 includes the first thin film transistor 71a whose source or drain is connected to the data line D1 and whose gate is connected to the scanning line G2 next to the corresponding scanning line G1, and a second thin film transistor 71b whose gate is connected to the corresponding scanning line G1, the second thin film transistor being serially connected to the first thin film transistor 71a. The second switch 73 has the same configuration as that of the first switch 71.

[0033] In the liquid crystal display having the above-described configuration according to the second embodiment of the present invention, upon application of a driving signal with the waveform of FIG. 8B to the scanning lines, an image is displayed, moving from the upper part to the lower part of the liquid crystal panel, and a corre-

sponding data line delivers the video signal to the pixels located at the left and right sides thereof, resulting in reduction in the total number of the data lines.

[0034] FIG. 9A shows the configuration of a liquid crystal display according to a third embodiment of the present invention, and FIG. 9B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 9A. Referring to FIG. 9A, in this embodiment, the first switch 71 is placed at the right side of the data line D1 and the second switch 73 is located at its left side. That is, the first switch 71 is formed at the right side of the data line in the third embodiment whereas it is located at the left side of the data line in the first and second embodiments.

[0035] Specifically, the liquid crystal display according to the third embodiment of the present invention includes the plurality of scanning lines G1, G2, ..., Gn-1, Gn arranged in row direction, the plurality of data lines D1, D2, ..., Dn-1, Dn intersecting the scanning lines, the first switches 71 each of which is located at the right side of each data line intersecting each scanning line, the second switches 73 each of which is placed at the left side of each data line, the first pixel electrodes 71c each of which is connected to each first switch 71, and the second pixel electrodes 73c each of which is connected to each second switch 73.

[0036] The configuration of the liquid crystal display according to the third embodiment of the invention is explained below in detail with reference to the portion "X" of FIG. 9A. At the portion where the scanning line G1 and data line D1 intersect each other, the first switch 71 is disposed at the right side of the data line D1 and the second thin film transistor 71b constructing the first switch 71 is connected to the next scanning line G2. That is, the first switch 71 includes the first thin film transistor 71a whose source or drain is connected to the data line D1 and whose gate is connected to the corresponding scanning line G1, and the second thin film transistor 71b whose gate is connected to the next scanning line G2, the second thin film transistor being serially connected to the first thin film transistor 71a.

[0037] The second switch 73 is located at the left side of the data line D1 and has two thin film transistors. Specifically, the second switch 73 includes the third thin film transistor 73a whose source or drain is connected to the data line D1 and whose gate is connected to the corresponding scanning line G1, and the fourth thin film transistor 73b whose gate is connected to the corresponding scanning line G1, the fourth thin film transistor being serially connected to the third thin film transistor 73a. Here, the second switch 73 may be configured of a single thin film transistor.

[0038] The liquid crystal display of the third embodiment of the invention, constructed as above, is driven by a driving signal having the waveform of FIG. 9B. Referring to FIG. 9B, during one horizontal period, the first scanning line G1 receives a 'high' signal while the second scanning line G2 receives the 'high' signal during the section (a)

corresponding to the first half of the horizontal period but receives a 'low' signal during the section (b), i.e., the second half of the horizontal period. When the 'high' signal is applied to both of the first and second scanning lines G1 and G2, the thin film transistors constructing the first and second switches 71 and 83 are all turned on, to deliver a video signal to the first and second pixel electrodes 71c and 73c. When the 'high' signal is applied to the first scanning line G1 and the 'low' signal is applied to the second scanning line G2, the second thin film transistor of the first switch 71 is turned off so that the video signal is not delivered to the first pixel electrode 71c, being sent to only the first pixel electrode 71c. In this manner, a corresponding image is displayed, moving from the upper portion to the lower portion of the liquid crystal panel.

[0039] FIG. 10A shows the configuration of a liquid crystal display according to a fourth embodiment of the present invention, and FIG. 10B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 10A. Referring to FIG. 10A, the liquid crystal display according to the fourth embodiment of the present invention has a difference from the third embodiment in the connection points of the gates of the first and second thin film transistors 71a and 71b constructing the first switch 71. That is, the gate of the first thin film transistor 71a of the first switch 71 is connected to the scanning line G2 next to the corresponding scanning line G1 in the fourth embodiment, while the gate of the second thin film transistor 71b of the first switch 71 is connected to the scanning line G2 in the third embodiment.

[0040] Specifically, the first switch 71 according to the fourth embodiment of the present invention includes the first thin film transistor 71a whose source or drain is connected to the data line D1 and whose gate is connected to the next scanning line G2, and the second thin film transistor 71b whose gate is connected to the corresponding scanning line G1, the second thin film transistor 71b being serially connected to the first thin film transistor 71a. Accordingly, upon application of a driving signal having the waveform of FIG. 10B to the scanning lines, a corresponding video signal can be selectively supplied to the pixels respectively placed at the left and right sides of the data line D1. The image corresponding to the video signal is displayed, moving from the upper portion to the lower portion of the liquid crystal panel.

[0041] FIG. 11A shows the configuration of a liquid crystal display according to a fifth embodiment of the present invention, and FIG. 11B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 11A. The fifth embodiment has a difference from the first to fourth embodiments in the location where the thin film transistors constructing the first and second switches are formed.

[0042] In the first to fourth embodiments of the present invention, the thin film transistors and pixel electrodes are located at portions where the data lines D1, D2, ..., Dn-1, Dn intersect the scanning lines G1, G2, ..., Gn-1,

Gn, sequentially, starting from the first intersecting portion where the first scanning line intersects the data lines to the (n-1)th intersecting portion where the (n-1)th scanning line intersects the data lines. The thin film transistors and the pixel electrodes are not formed at the portion where the nth scanning line intersects the data lines.

[0043] In the fifth embodiment of the invention, on the other hand, the thin film transistors and the pixel electrodes are not placed at the portion where the first scanning line intersects the data lines, but located at the portions, sequentially starting from the second intersecting portion where the second scanning line intersect the data lines to the nth intersecting portion where the nth scanning line intersects the data line.

[0044] In addition, one of the four thin film transistors, formed at the portion where (n-1)th scanning line intersects the data lines, is connected to the (n-1)th scanning line in the fifth embodiment, while it is connected to the nth scanning line in the first to fourth embodiments. When a driving signal having the waveform of FIG. 11B is applied to the scanning lines of the liquid crystal display of the fifth embodiment, a corresponding image is displayed, moving from the lower portion to the upper portion of the liquid crystal panel. The scanning lines are provided with the driving signal, in one horizontal period being split into two sections (a) and (b), as shown in FIG. 11B, so that the video signal can be selectively applied to the pixels respectively located at the left and right sides of each data line.

[0045] There is described below the fifth embodiment of the present invention in detail. Referring to FIG. 11A, the plurality of scanning lines G1, G2, ..., Gn-1, Gn are arranged in one direction, and the plurality of data lines D1, D2, ..., Dn-1, Dn intersect the scanning lines. The first and second switches 71 and 73 are formed at the left and right sides of each data line, respectively. Each of the first and second switches 71 and 73 consists of thin film transistors, each thin film transistor being an N-type or P-type thin film transistor. The gate of the second thin film transistor 71b of the first switch 71 located at the left of the data line D1 is connected to the (n-1)th scanning line, and the gate of its first thin film transistor 71a is connected to the nth scanning line. The second switch 73 formed at the right side of each data line includes the third and fourth thin film transistors both of which are connected to the nth scanning line. Here, the second switch 73 can be configured of a single thin film transistor.

[0046] There is explained below in more detail the operation of the liquid crystal display according to the fifth embodiment of the present invention with reference to the portion "X" of FIG. 11A. As shown in FIG. 11B, the scanning line Gn receives a 'high' signal during one horizontal period, and the previous scanning line Gn-1 receives the 'high' signal during only the first half section (a) thereof. During the period where both of the corresponding scanning line Gn and previous scanning line Gn-1 are in the 'high state', the thin film transistors constructing the first and second switches 71 and 73 are all

turned on, to deliver a corresponding video signal to the first and second pixel electrodes 71c and 73c.

[0047] When a 'low' signal is applied to the previous scanning line Gn-1 during the second half section (b) of the horizontal period, the second thin film transistor of the first switch 71 is turned off, to transmit no video signal to the first pixel electrode 71c. At this time, the switch 73 located at the right side of the data line is held in turn-on state, to deliver the video signal to the second pixel electrode 73c. As described above, the video signal can be selectively transmitted to the pixels respectively formed at the left and right sides of each data line, resulting in reduction in the total number of the data lines by half.

[0048] FIG. 12A shows the configuration of a liquid crystal display according to a sixth embodiment of the present invention, and FIG. 12B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 12A. The sixth embodiment of the present invention has a difference from the fifth embodiment in the connection points of the gates of the first and second thin film transistors 71a and 71b constructing the first switch 71. That is, the gate of the first thin film transistor 71a is connected to the (n-1)th scanning line Gn-1 and that of the second thin film transistor 71b is connected to the nth scanning line Gn in the sixth embodiment: whereas the gate of the first thin film transistor 71a is connected to the nth scanning line Gn and that of the second thin film transistor 71b is connected to the (n-1)th scanning line in the fifth embodiment. Here, the second switch 73 has the same configuration as that of the fifth embodiment.

[0049] Upon application of the driving signal shown in FIG. 12B to the scanning lines, a video signal from a corresponding data line can be selectively delivered to the pixels located at the left and right of that data line. Further, a corresponding image is displayed, moving from the lower portion to the upper portion of the liquid crystal panel as in the fifth embodiment.

[0050] FIG. 13A shows the configuration of a liquid crystal display according to a seventh embodiment of the present invention, and FIG. 13B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 13A. The liquid crystal display according to the seventh embodiment of the invention is constructed in such a manner that, as shown in FIG. 13A, the first and second switches are located at the right and left sides of each data line, respectively. That is, the liquid crystal display of the seventh embodiment includes the plurality of scanning lines G1, G2, ..., Gn-1, Gn arranged in one direction, the plurality of data lines D1, D2, ..., Dn-1, Dn intersecting the scanning lines, the first and second switches 71 and 73 formed at both sides of each data line and controlled by a corresponding scanning line and the scanning line previous thereto, and the first and second pixel electrodes 73a and 73c respectively connected to the first and second switches 71 and 73.

[0051] This is described below in more detail with reference to the portion "X" of FIG. 13A. The first switch 71

includes the first thin film transistor 71a whose source or drain is connected to the data line D1 and whose gate is connected to the corresponding scanning line Gn, and the second thin film transistor 71b whose gate is connected to the previous scanning line Gn-1, the second thin film transistor being serially connected to the first thin film transistor. The second switches 73 includes the third thin film transistor 73a whose source or drain is connected to the data line D1 and whose gate is connected to the corresponding scanning line Gn, and the fourth thin film transistor 73b whose gate is connected to the corresponding scanning line Gn, the fourth thin film transistor 73b being serially connected to the third thin film transistor 73a. The second switch 73 can be configured of only the third thin film transistor 73a. When a driving signal with the waveform of FIG. 13B is applied to the scanning lines of the liquid crystal display constructed as above, a corresponding image is displayed, moving from the lower portion to the upper portion of the liquid crystal panel. This is the same operation as that of the fifth and sixth embodiments.

[0052] FIG. 14A shows the configuration of a liquid crystal display according to an eighth embodiment of the present invention, and FIG. 14B shows the waveform of a driving signal applied to the scanning lines of the liquid crystal display of FIG. 14A. The eighth embodiment of the present invention has a difference from the seventh embodiment in the connection points of the gates of the first and second thin film transistors 71a and 71b constructing the first switch 71. That is, the first switch 71 according to the eighth embodiment of the invention includes the first thin film transistor 71 whose source or drain is connected to the data line D1 and whose gate is connected to the scanning line Gn-1 previous to the corresponding scanning line Gn, and a second thin film transistor 71b whose gate is connected to the corresponding scanning line Gn, the second thin film transistor 71b being connected to the first thin film transistor 71a. Here, the second switch 73 has the same configuration as that of the second switch 73 according to the seventh embodiment.

[0053] When a driving signal with the waveform of FIG. 14B is applied to the scanning lines of the liquid crystal display according to the eighth embodiment, constructed as above, an image is displayed, moving from the lower portion to the upper portion of the liquid crystal panel. As described above, the liquid crystal display of the present invention can deliver a video signal to the pixels located at the left and right sides of each data line, resulting in reduction in the total number of the data lines by half. This also decreases the number of the source drivers each of which applies a driving signal to each data lines by half.

[0054] There is explained below a circuit for driving the liquid crystal display according to the present invention.

[0055] First of all, there is needed a source driver having a configuration for satisfying the liquid crystal display of the invention with the reduced number of the data lines.

That is, the source driver for driving the liquid crystal display of the present invention is required to be able to handle video signals corresponding to 768 lines in total in case of 384 data lines. For this, the source driver may be configured as shown in FIG. 15A. FIG. 15A shows a source driver according to an embodiment of the present invention. The source driver of FIG. 15A includes a sampling latch having cells twice the number of that of the sampling latch of a conventional source driver. This is because the source driver should process image data corresponding to 784 lines though it drives the 384 data lines.

[0056] Referring to FIG. 15A, the source driver of the present invention includes: a 128-clock shift register 151 for shifting a horizontal synchronous signal pulse depending on a source pulse clock HCLK to output a latch clock; a first sampling latch 152 for sampling and latching digital R, G, B data corresponding to odd-numbered column lines among the 768 column lines according to the latch clock sent from the shift register 151; a second sampling latch 153a for sampling and latching digital R, G, B data corresponding to even-numbered column lines among the 768 lines; a holding latch 153 for receiving and latching the data items, respectively stored in the first and second sampling latches 152 and 152a, according to first and second load signals LDO and LDE, respectively; a D/A converter 154 for converting the digital R, G, B data corresponding to the odd-numbered column lines or the digital data corresponding to the even-numbered column lines, stored in the holding latch 153, into analog data signals; and an amplifier 155 for amplifying the currents of the analog R, G, and B data signals corresponding to the odd-numbered columns or the analog data signals corresponding to the even-numbered columns, supplied by the D/A converter 154.

[0057] The source driver according to the first embodiment of the present invention has the first sampling latch 152 which samples and latches the image data corresponding to the odd-numbered column lines among the 768 lines in total, and the second sampling latch 152a which samples and latches the image data corresponding to the even-numbered column lines. With one horizontal period, being divided into two sections, the R, G, and B data corresponding to the odd-numbered column lines is sampled and latched by the first sampling latch 152 during the first half of the horizontal period (it may not be the exact one-half), and the R, G, and B data corresponding to the even-numbered column lines is sampled and latched by the second sampling latch 152a during the second half. By doing so, the R, G, and B data of the 768 column lines can be sampled.

[0058] The digital video signals latched by the first and second sampling latches 152 and 152a, being divided into the odd-numbered column line data and the even-numbered column data, are sequentially transmitted to the holding latch 153. Specifically, the image data stored in the first sampling latch 152 is loaded in the holding latch 153 according to the first load signal LDO whereas

the image data stored in the second sampling latch 152a is loaded into the holding latch 153 according to the second load signal LDE. The digital R, G, B data loaded into the holding latch 153 is converted into the analog signal by the D/A converter 154, to be amplified by the amplifier 155. The R, G, and B data corresponding to the odd-numbered column lines are applied to the liquid crystal panel to be displayed during the first half of the horizontal period, and the R, G, B data of the even-numbered column lines is applied to the panel to be displayed during the second half.

[0059] FIG. 15B shows the operation waveforms of the source driver of FIG. 15A. It can be known from the FIG. 15B that the sampled odd-numbered column data and the sampled even-numbered column data are loaded into the holding latch 153 during one horizontal period. FIG. 16A shows a source driver according to another embodiment of the present invention. The source driver of FIG. 16A has first and second sampling latches 162 and 162a, first and second holding latches 163 and 163a, first and second D/A converters 164 and 164a and first and second amplifiers 165 and 165a for the purpose of applying image data to the liquid crystal panel, dividing it into odd-numbered column data and even-numbered column data, during one horizontal period. Further, the source driver according to the second embodiment of the invention includes a switch 166 for selectively delivering the outputs of the two amplifiers 165 and 165a to the data lines.

[0060] The first sampling latch 162 samples image data corresponding to the odd-numbered column lines while the second latch 162a sampled image data of the even-numbered column lines. The image data of the odd-numbered column lines latched by the first sampling latch 162 are loaded into the first holding latch 163 according to a load signal LD. On the other hand, the image data of the even-numbered column lines latched by the second sampling latch 162a are loaded into the second holding latch 163a according to the load signal LD. The digital image data stored in the first holding latch 163 are converted by the first D/A converter 164 into analog signals while the image data stored in the second holding latch 163a are converted by the second D/A converter 164a into analog signals. Here, the first and second D/A converters 164 and 164a convert the image data corresponding to the odd-numbered column lines and the image data of the even-numbered column lines into the analog signals, respectively.

[0061] The converted analog video signals corresponding to the odd-numbered and even-numbered column lines are amplified by the first and second amplifiers 165 and 165a, respectively. During the first half of the horizontal period, the analog video signals corresponding to the odd-numbered column lines are applied to the data lines under the operation of the switch 166. During the second half, on the other hand, the analog video signals corresponding to the even-numbered column lines are applied to the data lines according to the switch 166. Here, the switch 166 electrically connects the outputs of

the first amplifier 165 to the data lines D1, D2, ..., Dn-1, Dn during the first half of the horizontal period while it electrically connects the outputs of the second amplifier 165a to the data lines during the second half.

[0062] As described above, the source driver according to another embodiment of the present invention consists of two sampling latches, holding latches, D/A converters and amplifiers, to thereby apply the video signals corresponding to $2n$ column lines using n column lines.

[0063] There is explained below a gate driver for driving the liquid crystal display according to the present invention. FIG. 17A shows a gate driver according to a first embodiment of the present invention. Referring to FIG. 17A, the gate driver includes a shift register 171, a logic circuit 172, a level shifter 173 and an output buffer 174. The shift register 171 shifts a vertical synchronous signal pulse VSYNC depending on a gate pulse clock VCLK. The logic circuit 172 consists of a plurality of 3-input OR-gates OR1, OR2, ..., ORn each of which selectively receives three outputs of the shift register 171 and logically operates them.

[0064] According to a predetermined embodiment of the present invention, the first 3-input OR-gate OR1 receives outputs S1, S3 and S4 from S1 to Sn of the shift register 171, the second one receives outputs S3, S5 and S6, and the third one receives outputs S5, S7 and S8. Each of the fourth 3-input OR-gate to the final one also receives three outputs of the shift registers 171 in this manner. The level shifter 173 sequentially level-shifts a signal applied to the scanning lines to send the level-shifted signals to the output buffer 174. Accordingly, the plural scanning lines connected to the output buffer 174 are sequentially enabled. The operation of the gate driver according to the first embodiment of the present invention is described below with reference to FIG. 17B.

[0065] Referring to FIG. 17B, the first scanning line G1 receives the output waveform of the first OR-gate OR1, and the second scanning line G2 receives the output waveform of the second OR-gate OR2. The first scanning line to the last one are sequentially enabled in this manner. Here, each of the signals applied to the scanning lines G1, G2, ..., Gn-1, Gn repeats 'high' and 'low' states during one horizontal period. This is the same as the waveform of one of the driving signals shown in FIGS. 7B to 10B.

[0066] Meanwhile, the OR-gates shown in FIG. 17A may receive the outputs of the shift register 171 in a different manner. For example, the first OR-gate receives the outputs S1 and S2, the second OR-gate receives the outputs S1, S3 and S4, the third one receives outputs S3, S5 and S6 and so forth. Each of the fourth OR-gate to the last one receives three outputs of the shift register according to this rule. In this case, the driving signal applied to the scanning lines has waveforms G1', G2' and G3' shown in the lower portion of FIG. 17B.

[0067] As described above, the liquid crystal display of the present invention which transmits two video signals to two pixels, respectively, during one horizontal period

by the gate driver and source driver constructed as above can reduce the total number of the data lines, resulting in decrease in the number of the source drivers. However, the line time during which a video signal is delivered to each pixel is reduced because two video signals are needed to be sent to two pixels during one horizontal period. This requires the analog circuit to have the operation speed twice that of the conventional circuit. This problem remarkably appears in dot inversion. Accordingly, the video signal is written into the pixel electrodes in such a manner shown in FIG. 18.

[0068] The video signals are written in the order indicated by numbers shown in FIG. 18. Th is precharged at the moment when is is written because both of is and an are positive signals. Thus, charging can be carried out during only one-half of one horizontal period. ar and an require longer time for charging and discharging since their polarities are opposite to those of e and an. Accordingly, during the blanking time between writing of A and an and writing of an and an, the charging and discharging time is reduced by data line precharge or charge sharing between the data lines. There is no writing time problem with because it is precharged during be is written. However, there may be a problem in writing of is. To solve this, the magnitudes of the 'high' and 'low' sections (a) and (b) of the driving signal applied to the scanning lines during one horizontal period are controlled to secure the time required for writing al.

[0069] The liquid crystal display and driving circuit thereof according to the present invention has the following advantages. First of all, one data line can selectively deliver a video signal to two pixels located at the left and right sides thereof, resulting in reduction in the number of the data lines by half. This also decreases the number of the source drivers by half. Accordingly, it is possible to reduce the size of the display and the cost for manufacturing it. Moreover, more images can be displayed in the same size than in the conventional display, realizing a high resolution. It will be apparent to those skilled in the art that various modifications and variations can be made in the liquid crystal display and circuit for driving the same of the present invention without departing from the scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims.

Claims

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1. A liquid crystal display having first and second plates and a liquid crystal being sealed therebetween, wherein the liquid crystal display comprises 2N columns of pixels, the liquid crystal display including:

55 a plurality of scanning lines (D1, 2, ...Dn) arranged on the first plate in one direction:

N data lines arranged on the first plate, intersecting the scanning lines, each of the N data lines being for supplying data signals to two adjacent columns of the pixels, wherein each data line is connected to one of the adjacent columns of pixels via switches having

two transistors connected in series and having the control terminals connected to the same scanning line, and is connected to the other one of the two adjacent columns of pixels via switches having two transistors connected in series and having the control terminals connected to two different adjacent scanning lines and an arrangement of switches (71a, 71b, 73a, 73b) configured to connect each of the data lines selectively to the electrodes (71c, 73c) of two adjacent columns of pixels:

a source driver comprising:

an $(n/3)$ -clock shift register (151, 161) for shifting a horizontal synchronous signal pulse, to output a latch clock;

a first sampling latch (152, 162) for sampling and latching digital video signals corresponding to odd-numbered column lines among the $2N$ column lines according to the latch clock sent from the shift register (151, 161);

a second sampling latch (152a, 162a) for sampling and latching digital video signals corresponding to even-numbered column lines among $2N$ column lines according to the latch clock outputted from the shift register (151, 161);

a holding latch (153, 163, 163a) for receiving and latching the data stored in the first sampling latch (152, 162) according to a first load signal, and for receiving and latching the data stored in the second sampling latch (152a, 162a) according to a second load signal;

a D/A converter (154, 164, 164a) for converting the digital video signals corresponding to the odd-numbered column lines or the digital video signals corresponding to the even-numbered column lines, stored in the holding latch (153, 163, 183a), into analog data signals;

and an amplifier (155, 165, 165a) for amplifying the analog video signals corresponding to the odd-numbered column lines or the analog video signals corresponding to the even-numbered column lines, supplied from the D/A converter (154, 164, 164a), wherein the output of the amplifier (155, 165, 165a) is supplied to the N data lines;

and a gate driver configured to supply control signals (G1, G2, ... Gn) sequentially over one frame of the video signal to the scanning lines (G1, G2, ... Gn), the control signal in each sequential horizontal period (H) within the frame

comprising two successive periods (a, b) at which the signal is in selectively a high or a low state; the control signals (G1, G2) being arranged to control the connection of the two pixels for each row and each data line selectively in each period (a, b) to the respective data line by means of the switches for that data line and that row of pixels;

the gate driver comprising:

a shift register (171) having n outputs and configured to shift a vertical synchronous pulse depending on a gate pulse clock so that non-overlapping pulses are output sequentially in time at the n outputs, groups of whose outputs (S1, S2, ..., Sn) are connected to respective inputs of a plurality of three-input OR gates within a logic circuit (172) of the gate driver, one OR gate for each respective scanning line (G1, ..., Gn); and a level shifter (173) connected to level-shift the outputs of the OR gates and to provide the level-shifted signal to an output buffer (174) of the gate driver which is configured to output the level-shifter outputs to the respective scanning lines;

wherein the inputs of the OR gates are connected respectively to:

the first, third and fourth; the third, fifth and sixth; the fifth, seventh and eighth; and so on up to the $(n-3)^{th}$, $(n-1)^{th}$ and n^{th} shift register output

2. A display according to claim 1, wherein the number of each of the first and second sampling latches (152, 152a, 162, 162a) is determined by the number of the data lines.

3. A display according to claim 1, wherein:

the hold latch comprises first and second holding latches (163, 163a) for respectively receiving and latching the digital signals, respectively stored in the first and second sampling latches (162, 162a);

the D/A converter comprises first and second D/A converters (164, 164a) for respectively converting the digital video signals, respectively stored in the first and second holding latches (163, 163a), into the analog video signals;

the amplifier comprises first and second amplifiers (165, 165a) for respectively amplifying the analog video signals, respectively outputted from the first and second D/A converters (164, 164a), to a predetermined level; and

a switch (166) for selectively connecting the outputs of the first and second amplifiers to the n data lines.

4. A display according to claim 3, wherein the switch (166) is adapted to sequentially connect the output of the first amplifier(165) and output of the second amplifier (165a) to the N data lines during one horizontal period. 5

5. A display according to any preceding claim, in which the first OR gate is connected to the first and second shift register outputs, and the other OR gates are connected as aforesaid respectively to the first third and fourth; through to the (n-3)rd. (n-1)st and nth; shift register output. 10

Patentansprüche 15

1. Flüssigkristallanzeige, die erste und zweite Platten und einen dazwischen verschlossenen Flüssigkristall aufweist, wobei die Flüssigkristallanzeige 2N Spalten von Bildpunkten umfasst, die Flüssigkristallanzeige enthaltend:
 eine Vielzahl von Scanleitungen (D1, 2, ... Dn), die auf der ersten Platte in einer Richtung angeordnet sind; 20
 N Datenleitungen, die auf der ersten Platte angeordnet sind, die Scanleitungen kreuzen, wobei jede der N Datenleitungen zum Zuführen von Datensignalen zu zwei angrenzende Spalten von Bildpunkten ist, wobei jede Datenleitung mit einer der angrenzenden Spalten von Bildpunkten über Schalter, die zwei in Serie verbundene Transistoren aufweisen und die Steueranschlüsse mit derselben Scanleitung verbunden aufweisen, verbunden ist und mit der anderen der zwei angrenzenden Spalten von Bildpunkten über Schalter, die zwei in Serie verbundene Transistoren aufweisen und die Steueranschlüsse mit zwei verschiedenen Scanleitungen verbunden aufweisen, verbunden ist; 25
 und eine Anordnung von Schaltern (71a, 71b, 73a, 73b), die konfiguriert sind, um jede der Datenleitungen selektiv mit den Elektroden (71c, 73c) von zwei angrenzenden Spalten von Bildpunkten zu verbinden; 30
 einen Sourcetreiber, umfassend:
 einen (n/3)-Taktverschieberegister (151, 161) zum Verschieben eines horizontalen Syncsignalimpulses, um einen Zwischenspeicherungstakt auszugeben; 35
 einen ersten Abtastzwischenspeicher (152, 162) zum Abtasten und Zwischenspeichern von digitalen Videosignalen, die mit ungeradzahligen Spaltenleitungen unter den 2N Spaltenleitungen korrespondieren, gemäß dem von dem Verschieberegister (151, 161) gesandten Zwischenspeicherungs- 40
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ein (n/3)-Taktverschieberegister (151, 161) zum Verschieben eines horizontalen Syncsignalimpulses, um einen Zwischenspeicherungstakt auszugeben; 50
 einen ersten Abtastzwischenspeicher (152, 162) zum Abtasten und Zwischenspeichern von digitalen Videosignalen, die mit ungeradzahligen Spaltenleitungen unter den 2N Spaltenleitungen korrespondieren, gemäß dem von dem Verschieberegister (151, 161) gesandten Zwischenspeicherungs- 55

takt;
 einen zweiten Abtastzwischenspeicher (152a, 162a) zum Abtasten und Zwischenspeichern von digitalen Videosignalen, die mit geradzahligen Spaltenleitungen unter den 2N Spaltenleitungen korrespondieren, gemäß dem von dem Verschieberegister (151, 161) ausgegebenen Zwischenspeicherungstakt;
 einen Haltezwischenspeicher (153, 163, 163a) zum Empfangen und Zwischenspeichern der in dem ersten Abtastzwischenspeicher (152, 162) gespeicherten Daten gemäß einem ersten Ladesignal und zum Empfangen und Zwischenspeichern der in dem zweiten Abtastzwischenspeicher (152a, 162a) gespeicherten Daten gemäß einem zweiten Ladesignal;
 einen D/A-Umwandler (154, 164, 164a) zum Umwandeln der digitalen Videosignale, die mit den ungeradzahligen Spaltenleitungen korrespondieren, oder der digitalen Videosignale, die mit den geradzahligen Spaltenleitungen korrespondieren, die in dem Haltezwischenspeicher (153, 163, 163a) gespeichert sind, in analoge Daten signale;
 und einen Verstärker (155, 165, 165a) zum Verstärken der analogen Videosignale, die mit den ungeradzahligen Spaltenleitungen korrespondieren, oder der analogen Videosignale, die mit den geradzahligen Spaltenleitungen korrespondieren, die von dem D/A-Umwandler (154, 164, 164a) zugeführt werden, wobei der Ausgang des Verstärkers (155, 165, 165a) den N Datenleitungen zugeführt wird;
 und einen Gatetreiber, der konfiguriert ist, um den Scanleitungen (G1, G2, ... Gn) Steuersignale (G1, G2, ... Gn) sequenziell über einen Rahmen des Videosignals zuzuführen, wobei das Steuersignal in jeder sequenziellen horizontalen Periode (H) innerhalb des Rahmens zwei aufeinanderfol gende Perioden (a, b) umfasst, bei denen das Signal selektiv in einem hohen oder niedrigen Zustand ist; wobei die Steuersignale (G1, G2) angeordnet sind, um die Verbindung der zwei Bildpunkt für jede Reihe und jede Datenleitung selektiv in jeder Periode (a, b) zu der jeweiligen Datenleitung mittels der Schalter für diese Datenleitung und diese Reihe von Bildpunkten zu steuern;
 der Gatetreiber umfassend:

ein Verschieberegister (171), das n Ausgänge aufweist und konfiguriert ist, um einen vertikalen

synchronen Impuls in Abhängigkeit von einem Gateimpulstakt so zu verschieben, dass nicht überlappende Impulse sequenziell in der Zeit an den n Ausgängen ausgegeben werden, wobei Gruppen von diesen Ausgängen (S1, S2, ..., Sn) mit den jeweiligen Eingängen einer Vielzahl von OR-Gates mit drei Eingängen innerhalb einer logischen Schaltung (172) des Gatetreibers verbunden sind, einem OR-Gate für jede jeweilige Scanleitung (G1, ..., Gn); und einen Pegelschieber (173), der verbunden ist, um die Pegel der OR-Gates zu verschieben und um einem Ausgangspuffer (174) des Gatetreibers, der konfiguriert ist, um die pegelverschobenen Ausgänge zu den jeweiligen Scanleitungen auszugeben, das pegelverschobene Signal bereitzustellen; wobei die Eingänge der OR-Gates jeweils verbunden sind mit:

dem ersten, dritten und vierten; dem dritten, fünften und sechsten; dem fünften, siebten und achtten; und so weiter bis zu dem (n-3)-ten, (n-1)-ten und n-ten Verschieberegisterausgang.

2. Anzeige nach Anspruch 1, wobei die Zahl von jedem der ersten und zweiten Abtastzwischenspeicher (152, 152a, 162, 162a) durch die Zahl der Datenleitungen bestimmt ist.

3. Anzeige nach Anspruch 1, wobei:

der Haltezwischenspeicher erste und zweite Haltezwischenspeicher (163, 163a) zum jeweiligen Empfanden und Zwischenspeichern der digitalen Signale umfasst, die jeweils in den ersten und zweiten Abtastzwischenspeichern (162, 162a) gespeichert sind; der D/A-Umwandler erste und zweite D/A-Umwandler (164, 164a) zum jeweiligen Umwandeln der digitalen Videosignale, die jeweils in den ersten und zweiten Haltezwischenspeichern (163, 163a) gespeichert sind, in die analogen Videosignale umfasst; der Verstärker erste und zweite Verstärker (165, 165a) zum jeweiligen Verstärken der analogen Videosignale, die jeweils von den ersten und zweiten D/A-Umwandlern (164, 164a) ausgegeben werden, auf einen im Voraus bestimmten Pegel umfasst; und einen Schalter (166) zum selektiven Verbinden der Ausgänge der ersten und zweiten Verstärker mit den n Datenleitungen.

4. Anzeige nach Anspruch 3, wobei der Schalter (166) angepasst ist, um sequenziell den Ausgang des ersten Verstärkers (165) und den Ausgang des zweiten Verstärkers (165a) während einer horizontalen Periode mit den N Datenleitungen zu verbinden.

5. Anzeige nach einem der vorstehenden Ansprüche, wobei das erste Olt-Gate mit den ersten und zweiten Verschieberegisterausgängen verbunden ist und die anderen OR-Gates jeweils mit, wie oben erwähnt, dem ersten, dritten und vierten bis zu dem (n-3)-ten, (n-1)-ten und n-ten Verschieberegisterausgang verbunden sind.

Revendications

1. Dispositif d'affichage à cristaux liquides comprenant des première et seconde plaques et un cristal liquide étant scellé entre elles, dans lequel le dispositif d'affichage à cristaux liquides comprend 2N colonnes de pixels, le dispositif d'affichage à cristaux liquides comprenant :

une pluralité de lignes de balayage (D1, D2, ..., Dn) arrangées sur la première plaque dans une direction ;

N lignes de données arrangées sur la première plaque, coupant les lignes de balayage, chacune des N lignes de données servant à délivrer des signaux de données à deux colonnes adjacentes des pixels, où chaque ligne de données est connectée à une des colonnes adjacentes de pixels par l'intermédiaire de commutateurs ayant deux transistors connectés en série et ayant les bornes de commande connectées à la même ligne de balayage, et est connectée à l'autre des deux colonnes adjacentes de pixels par l'intermédiaire de commutateurs ayant deux transistors connectés en série et ayant les bornes de commande connectées à deux lignes de balayage adjacentes différentes ; et un arrangement de commutateurs (71a, 71b, 73a, 73b) configurés pour connecter chacune des lignes de données de manière sélective aux électrodes (71c, 73c) de deux colonnes de pixels adjacentes ;

un pilote source comprenant :

un registre à décalage d'impulsion (n/3) (151, 161) pour décaler une impulsion de signal synchrone horizontale, afin de délivrer une impulsion de bascule ;

une première bascule d'échantillonnage (152, 162) pour échantillonner et pour faire basculer les signaux vidéo numériques correspondant aux lignes de colonne de nombre impair parmi les 2N lignes de colonne en fonction de l'impulsion de bascule délivrée par le registre à décalage (151, 161) ;

une seconde bascule d'échantillonnage (152a, 162a) pour échantillonner et pour faire basculer

les signaux vidéo numériques correspondant aux lignes de colonne de nombre pair parmi 2N lignes de colonne en fonction de l'impulsion de bascule délivrée en sortie par le registre à décalage (151, 161);

une bascule de maintien (153, 163, 163a) pour recevoir et pour faire basculer les données stockées dans la première bascule d'échantillonnage (152, 162) en fonction d'un premier signal de charge, et pour recevoir et pour faire basculer les données stockées dans la seconde bascule d'échantillonnage (152a, 162a) en fonction d'un second signal de charge ;

un convertisseur numérique/analogique (D/A) (154, 164, 164a) pour convertir les signaux vidéo numériques correspondant aux lignes de colonne de nombre impair ou les signaux vidéo numériques correspondant aux lignes de colonne de nombre pair, stockés dans la bascule de maintien (153, 163, 163a), en signaux de données analogiques ;

et un amplificateur (155, 165, 165a) pour amplifier les signaux vidéo analogiques correspondant aux lignes de colonne de nombre impair ou les signaux vidéo analogiques correspondant aux lignes de colonne de nombre pair, provenant du convertisseur D/A (154, 164, 164a), où la sortie de l'amplificateur (155, 165, 165a) est délivrée aux N lignes de données ;

et un pilote de porte configuré pour délivrer des signaux de commande (G1, G2, ... Gn) séquentiellement sur une trame du signal vidéo vers les lignes de balayage (G1, G2, ... Gn), le signal de commande dans chaque période horizontale séquentielle (H) dans la trame comprenant deux périodes successives (a, b) dans lesquelles le signal est sélectivement dans un état haut ou dans un état bas ; les signaux de commande (G1, G2) étant arrangés pour contrôler la connexion des deux pixels pour chaque rangée et chaque ligne de données, sélectivement dans chaque période (a, b), à la ligne de données respective au moyen des commutateurs pour cette ligne de données et cette rangée de pixels ;

le pilote de porte comprenant :

un registre à décalage (171) comprenant n sorties et configuré pour décaler une impulsion synchrone verticale en fonction d'une impulsion de porte de manière à ce que des impulsions non chevauchantes soient délivrées séquentiellement dans le temps au niveau des n sorties, des groupes de ces sorties (S1, S2, ... Sn) sont connectés aux entrées respectives d'une pluralité de portes OU à trois entrées au sein d'un circuit logique (172) du pilote de porte, une porte

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OU pour chaque ligne de balayage respective (G1, ..., Gn); et un décaleur de niveau (173) connecté pour décaler le niveau des sorties des portes OU et pour délivrer le signal au niveau décalé à un tampon de sortie (174) du pilote de porte qui est configuré pour délivrer les sorties du décaleur de niveau aux lignes de balayage respectives ; où les entrées des portes OU sont respectivement connectées :

aux première, troisième et quatrième ; aux troisième, cinquième et sixième ; aux cinquième, septième et huitième; et ainsi de suite jusqu'aux (n-3)^{ième}, (n-1)^{ième} et n^{ième} sorties de registre à décalage.

2. Dispositif d'affichage selon la revendication 1, dans lequel le nombre de chacune des première et seconde bascules d'échantillonnage (152, 152a, 162, 162a) est déterminé par le nombre des lignes de données.
3. Dispositif d'affichage selon la revendication 1, dans lequel :

la bascule de maintien comprend des première et seconde bascules de maintien (163, 163a) pour respectivement recevoir et maintenir les signaux numériques respectivement stockés dans les première et seconde bascules d'échantillonnage (162, 162a);

le convertisseur numérique/analogique (D/A) comprend des premier et second convertisseurs numériques (164, 164a) pour respectivement convertir les signaux vidéo numériques, respectivement stockés dans les première et seconde bascules de maintien (163, 163a) dans les signaux vidéo analogiques ;

l'amplificateur comprend des premier et second amplificateurs (165, 165a) pour respectivement amplifier les signaux vidéo analogiques, respectivement délivrés en sortie par les premier et second convertisseurs numérique/analogique (D/A) (164, 164a), à un niveau prédéterminé ; et un commutateur (166) pour connecter sélectivement les sorties des premier et second amplificateurs aux n lignes de données.

4. Dispositif d'affichage selon la revendication 3, dans lequel le commutateur (166) est adapté pour connecter séquentiellement la sortie du premier amplificateur (165) et la sortie du second amplificateur (165a) aux N lignes de données au cours d'une période horizontale.
5. Dispositif d'affichage selon l'une quelconque des revendications précédentes, dans lequel la première

porte OU est connectée aux première et seconde sorties de registre à décalage, et les autres portes OU sont respectivement connectées, comme précédemment mentionné, aux première, troisième et quatrième jusqu'aux $(n-3)^{\text{ième}}$, $(n-1)^{\text{ième}}$ et $n^{\text{ième}}$ sorties de registre à décalage. 5

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FIG. 1

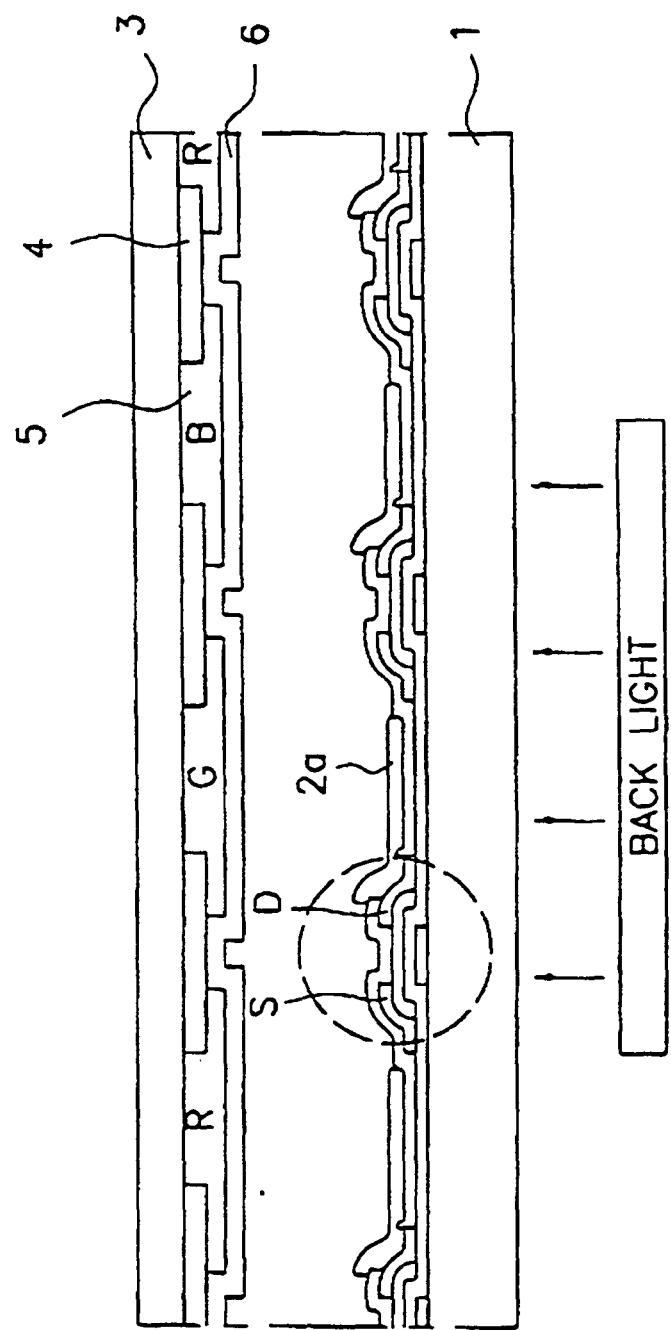


FIG.2

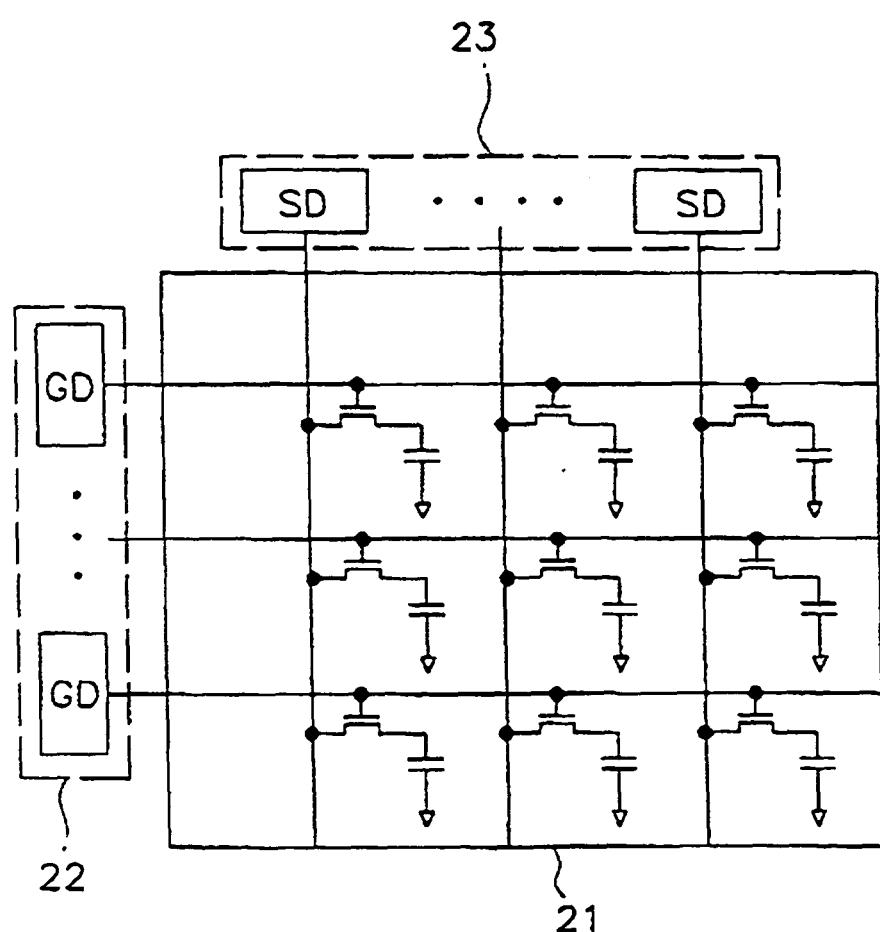


FIG.3

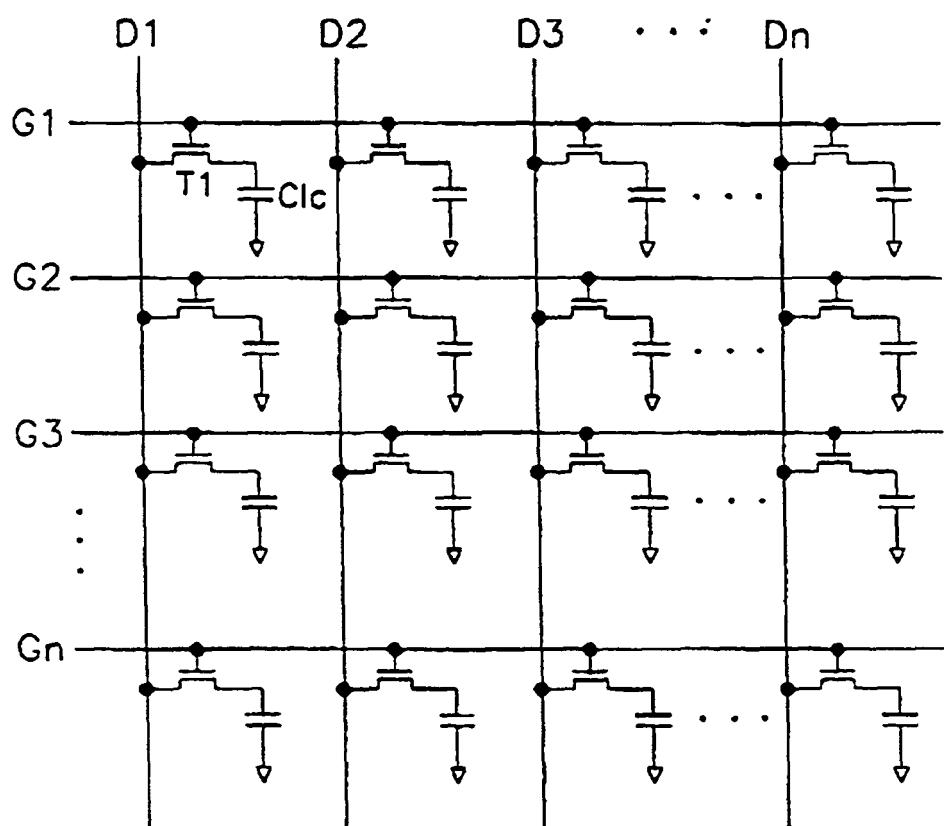


FIG. 4

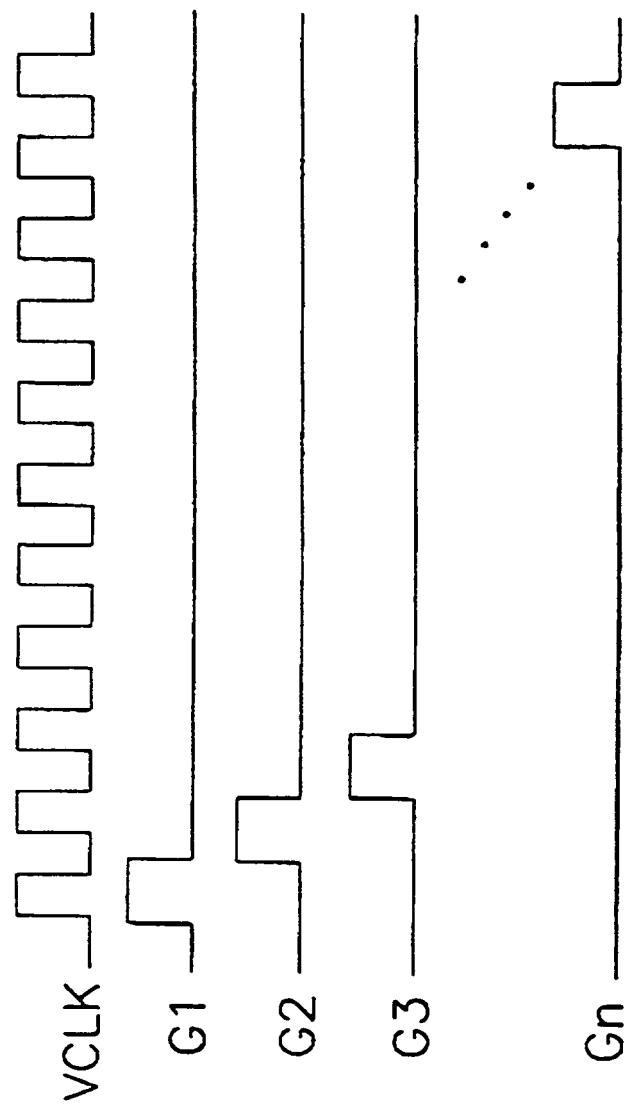


FIG.5A

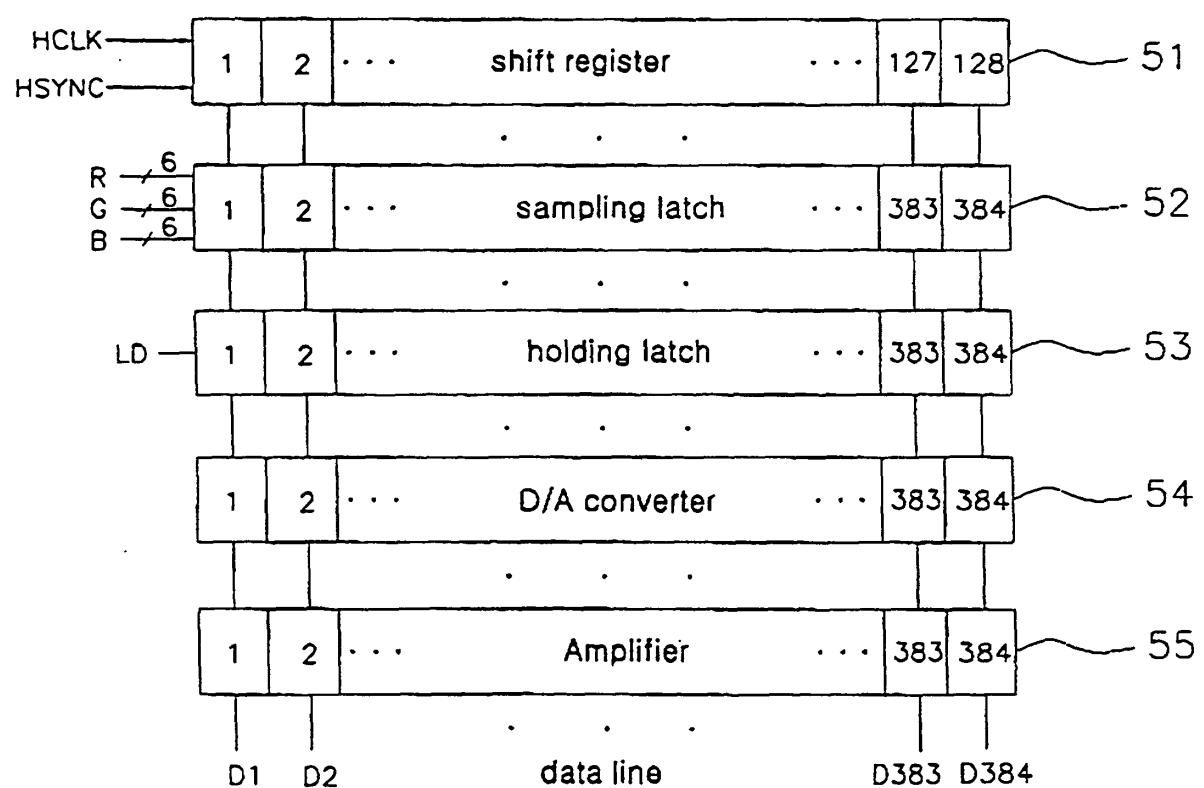


FIG.5B

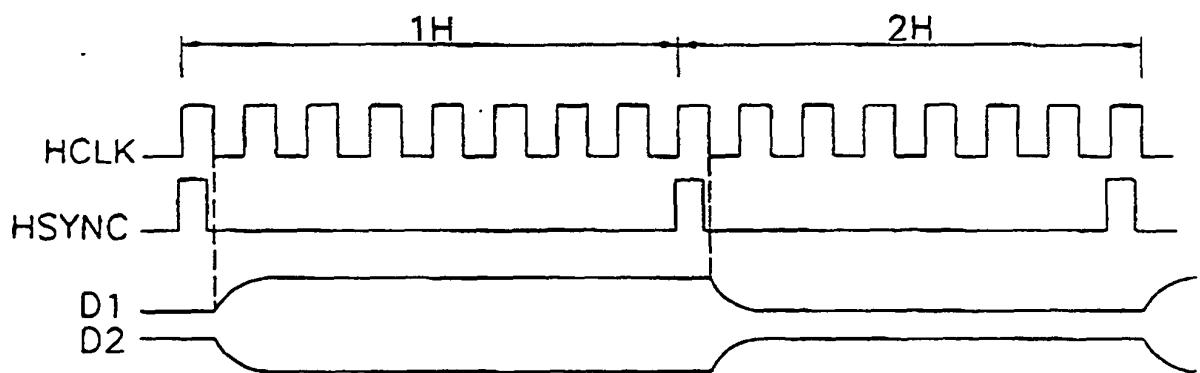


FIG.6A

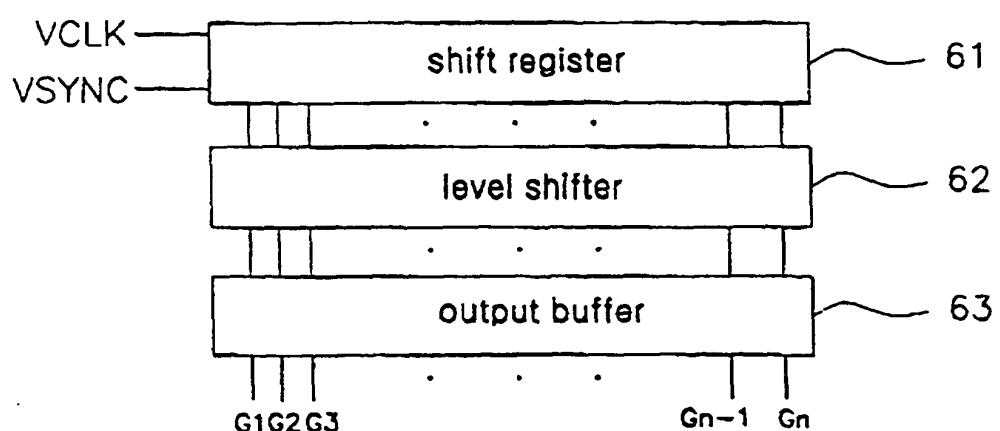


FIG. 6B

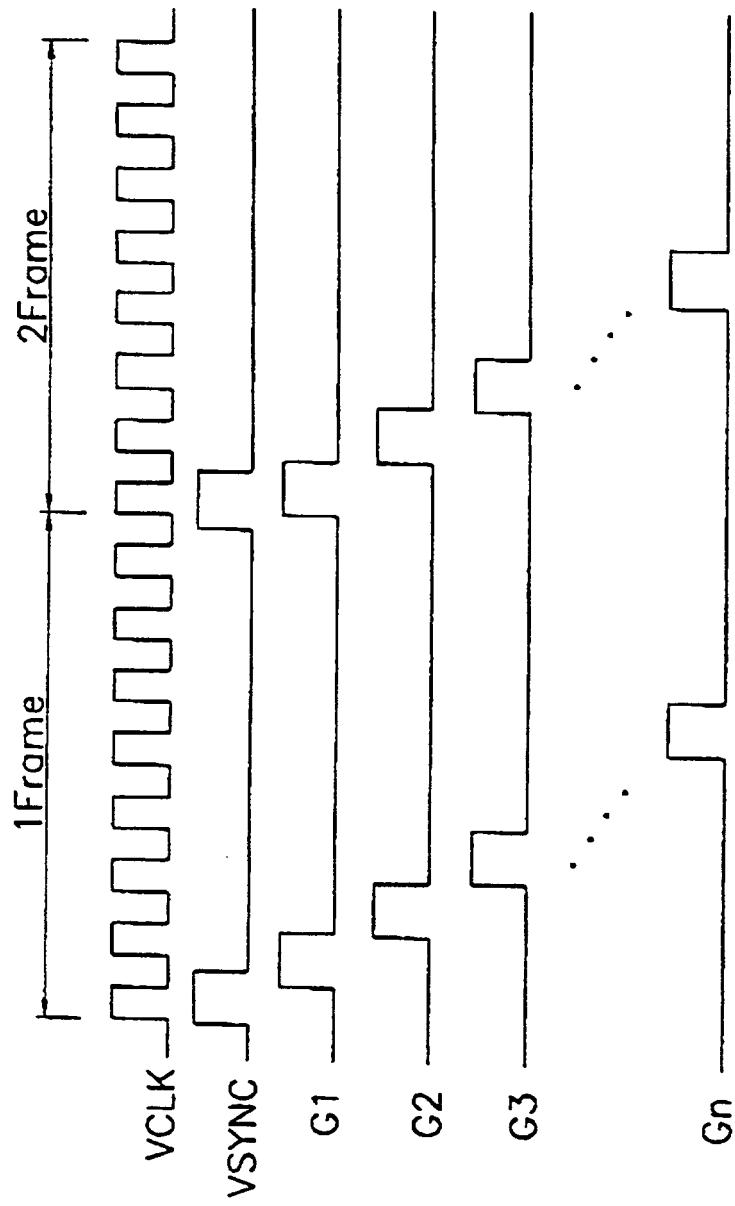


FIG. 7A

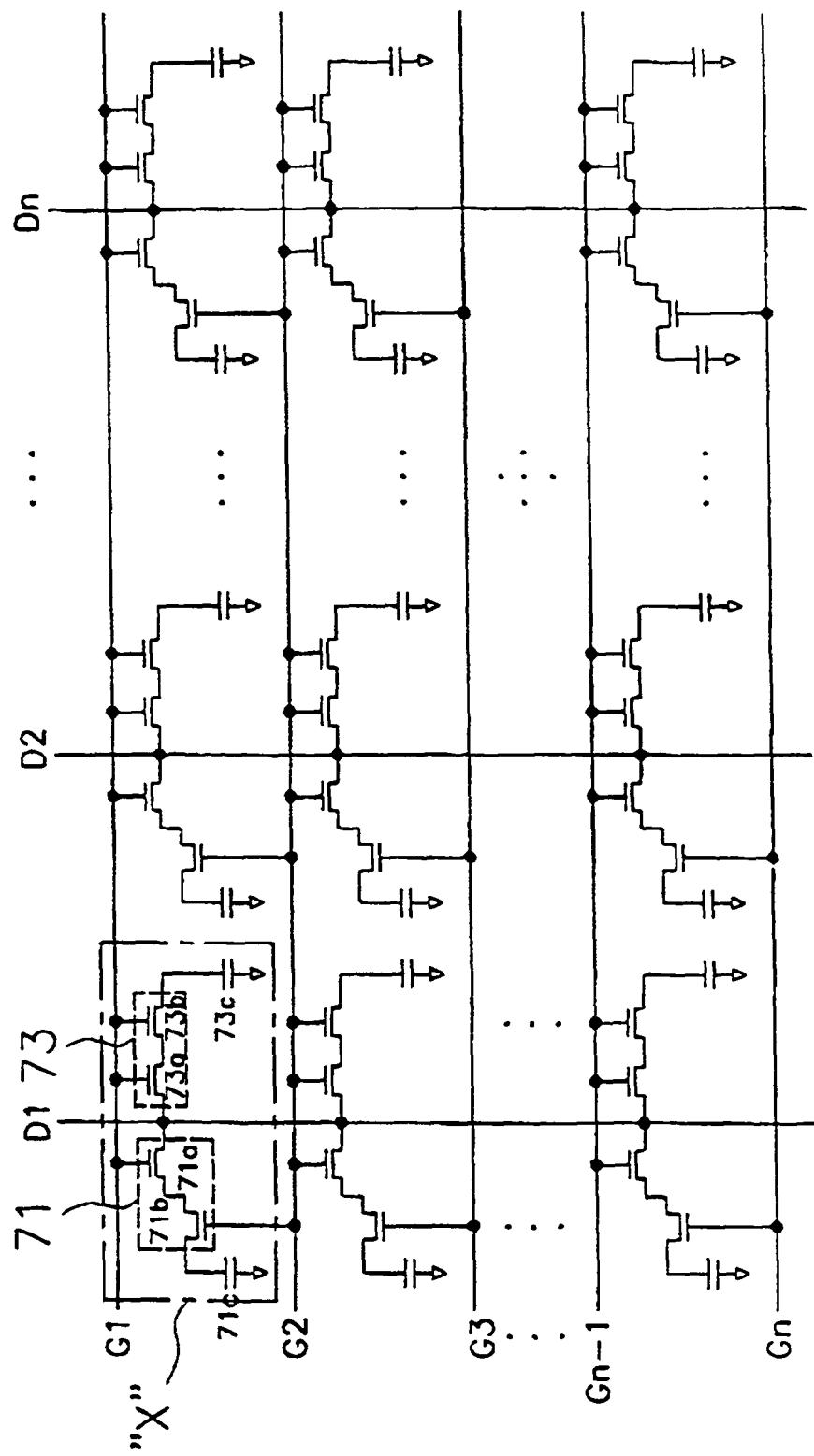


FIG. 7B

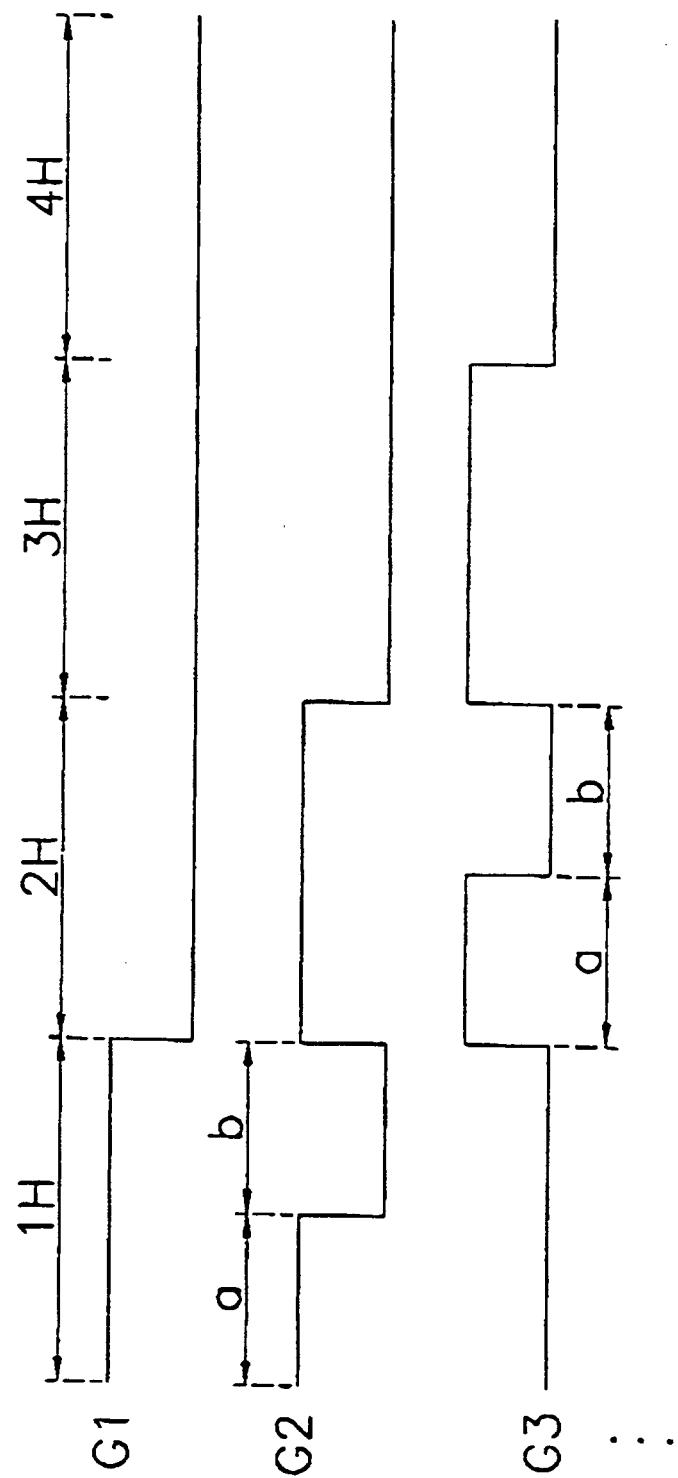


FIG. 8A

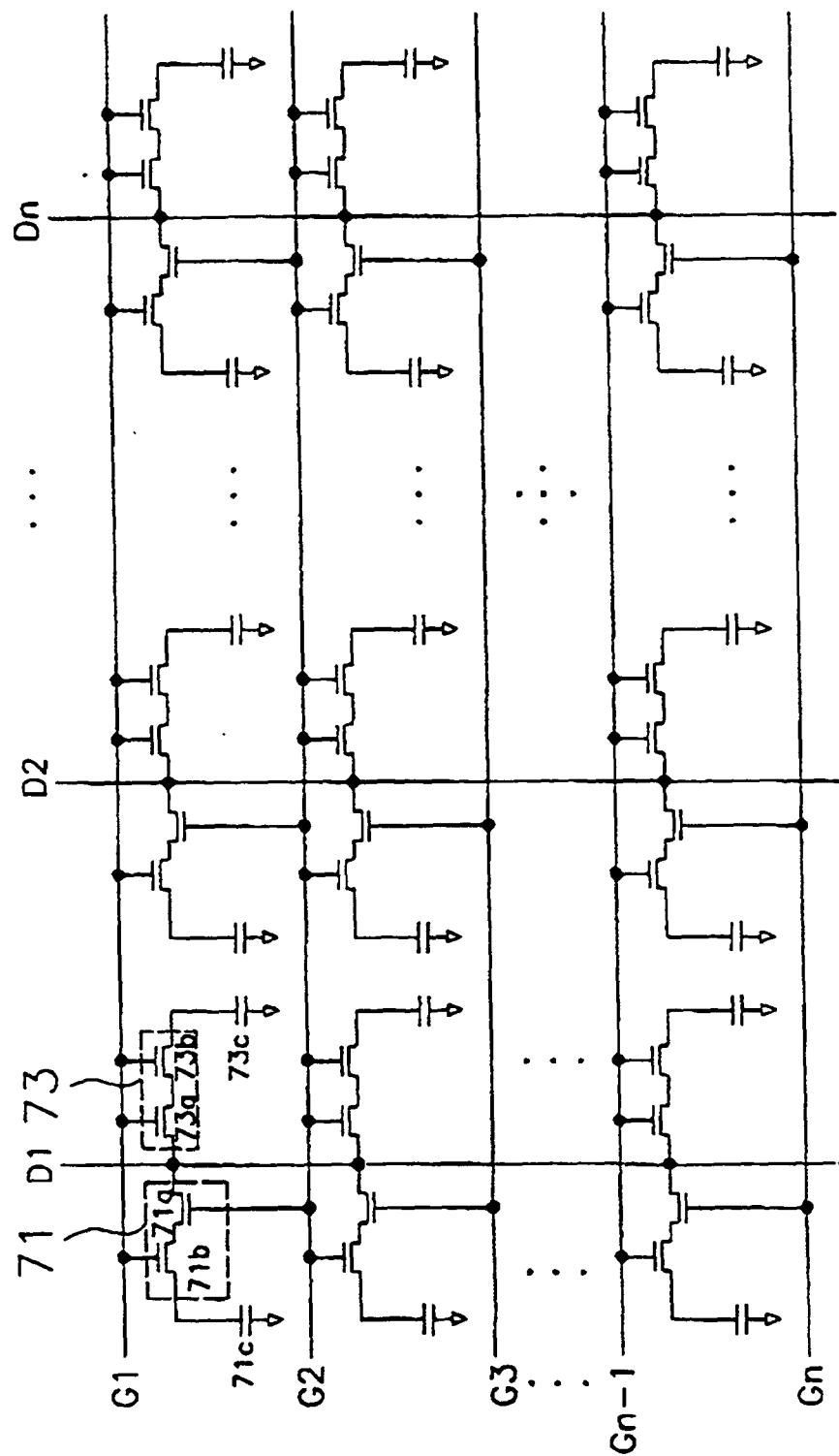


FIG. 8B

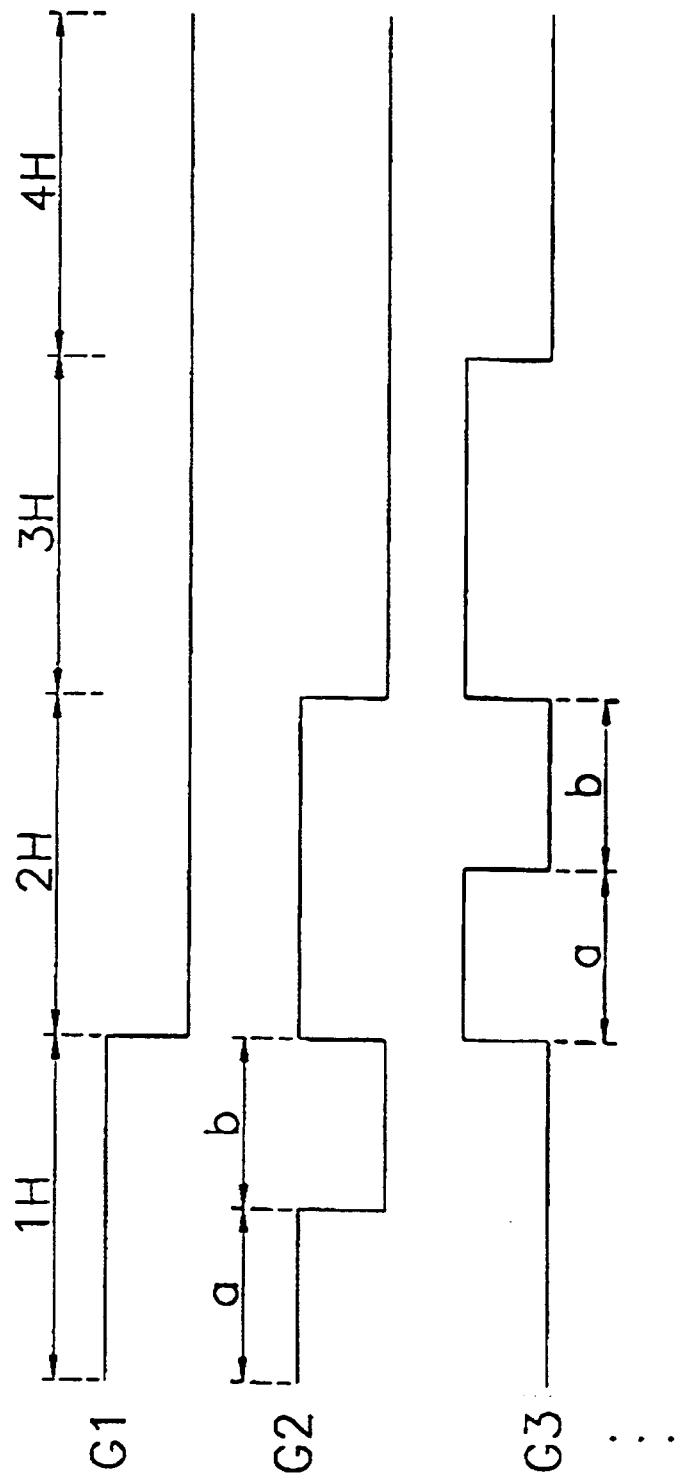


FIG. 9A

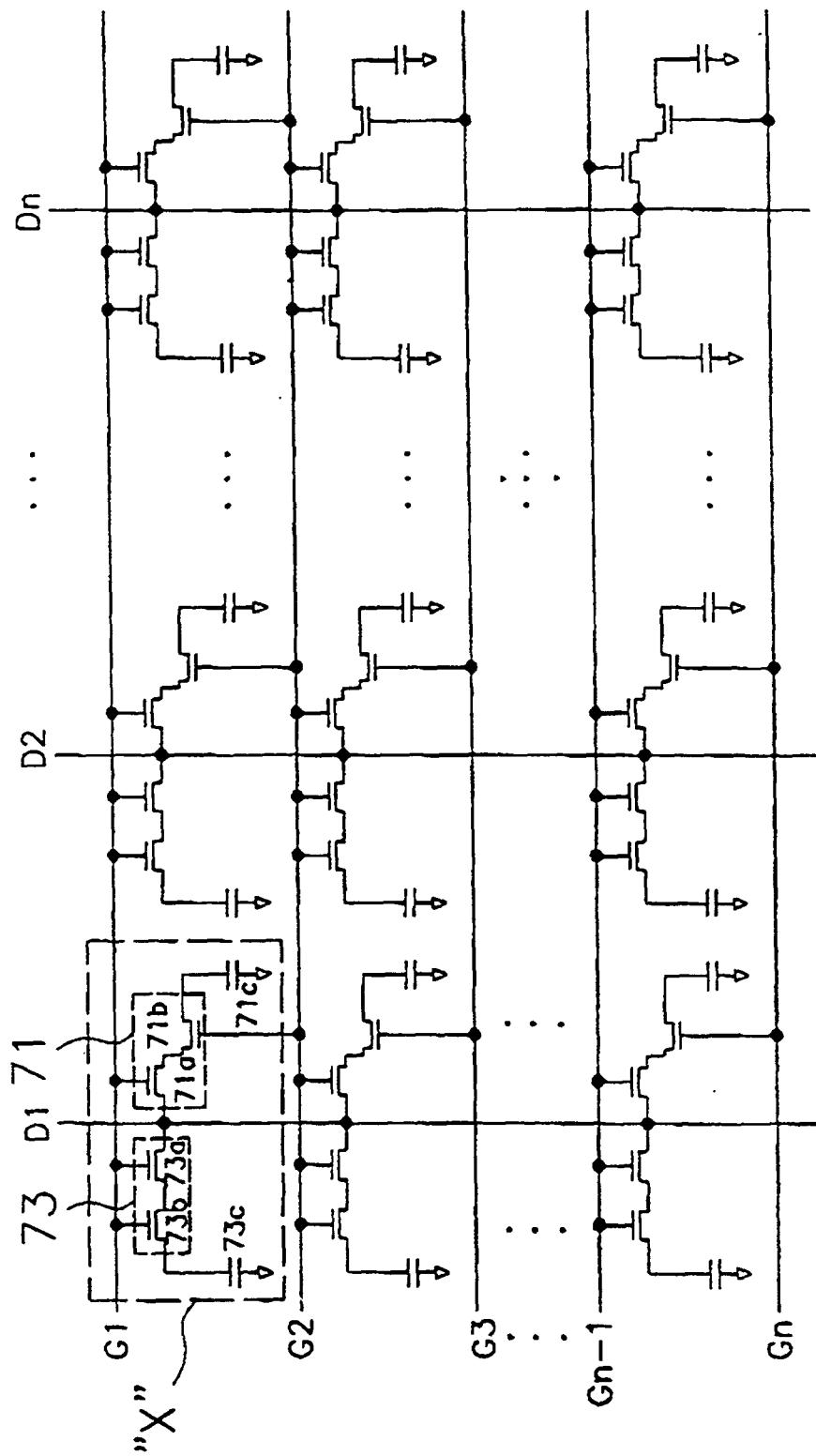


FIG. 9B

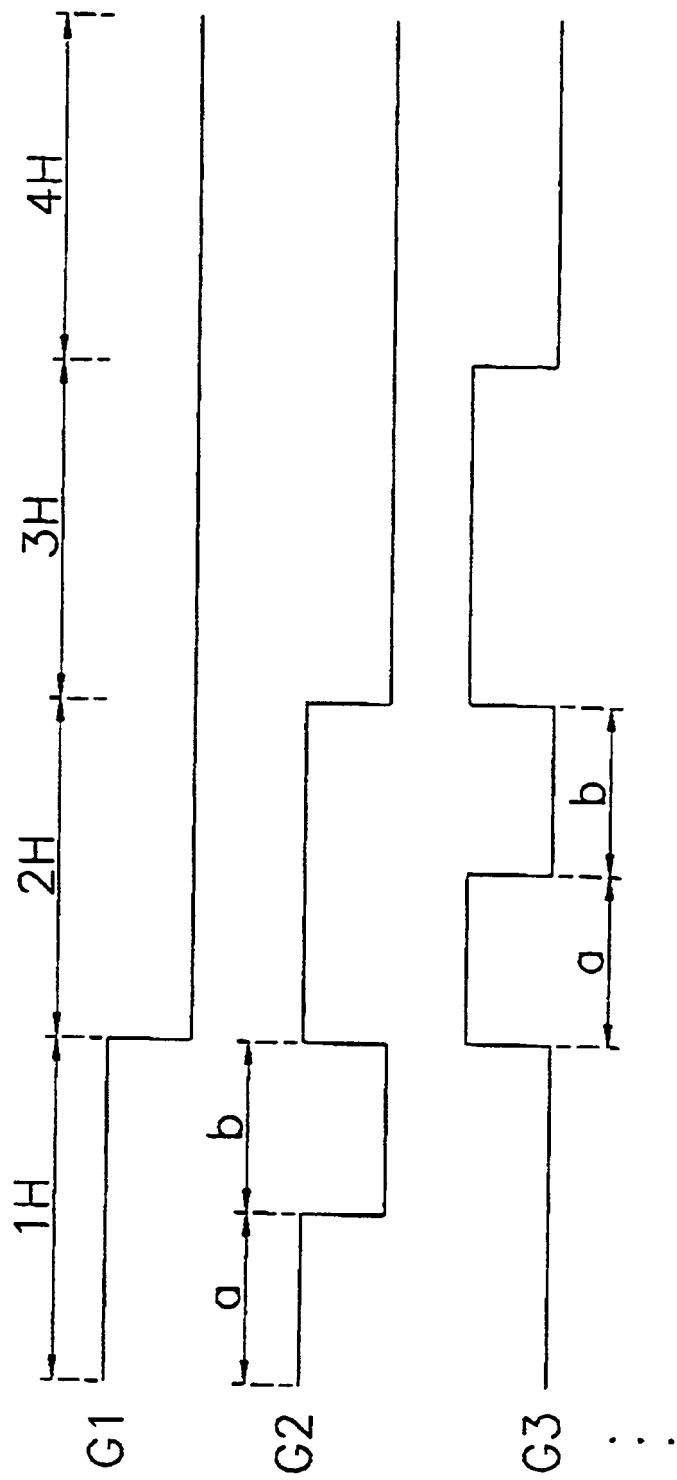


FIG. 10A

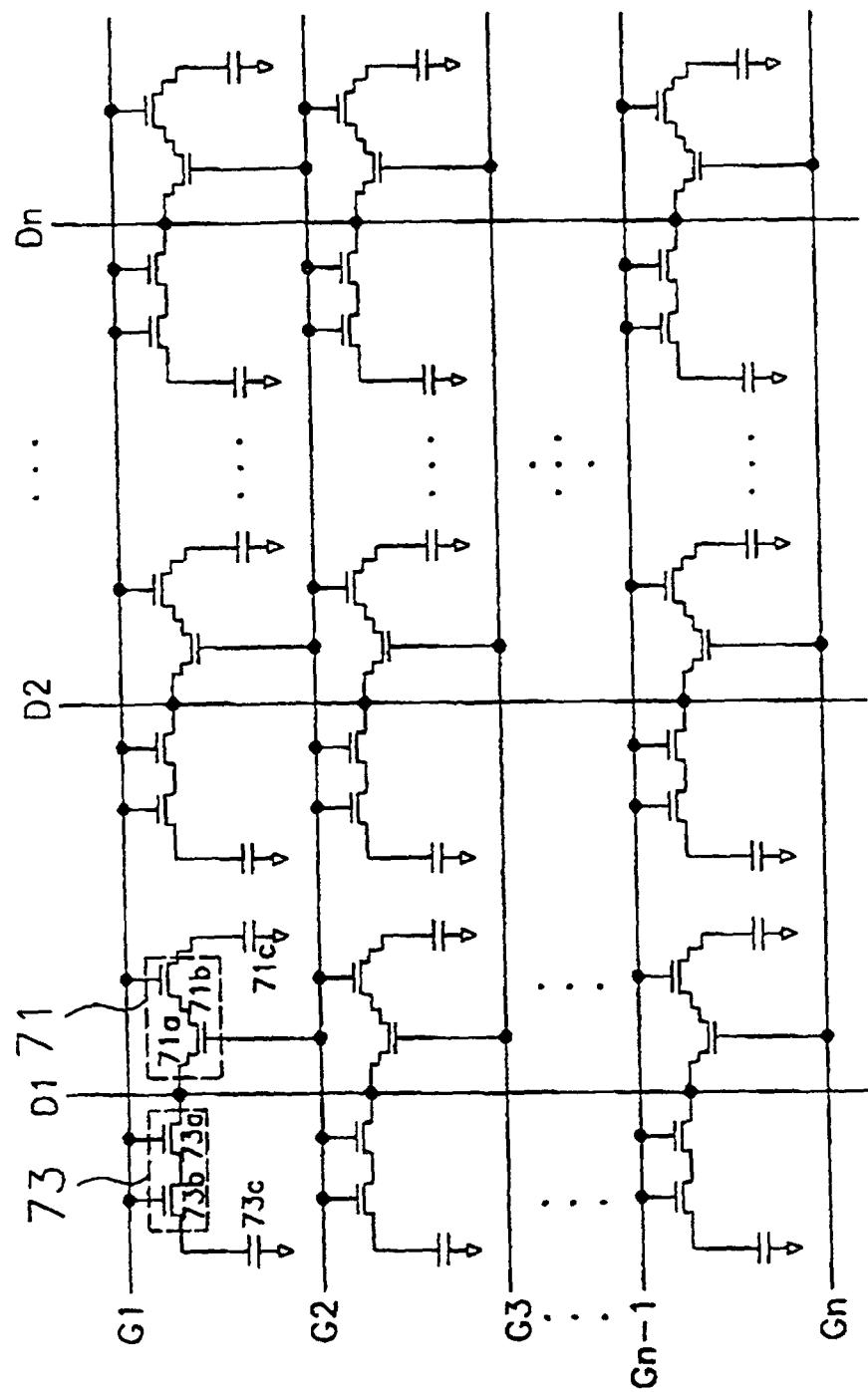


FIG. 10B

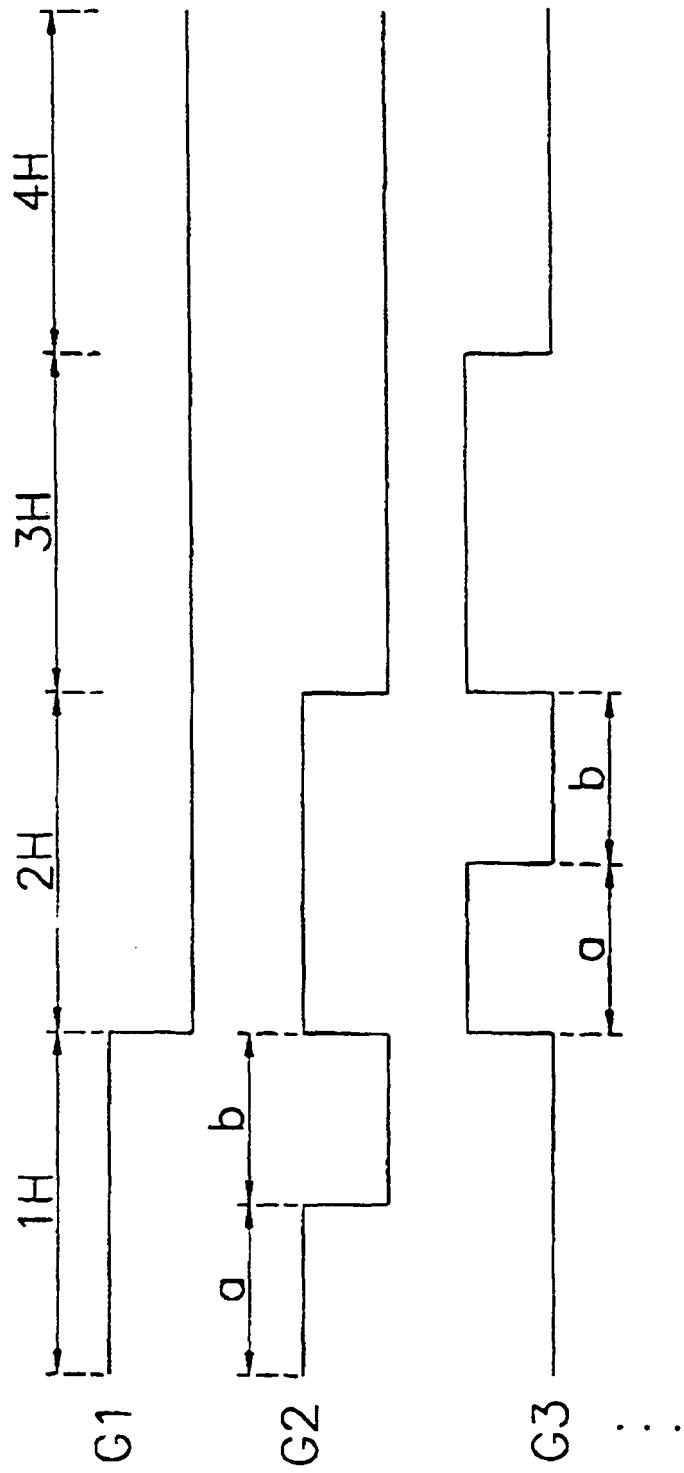


FIG. 11A

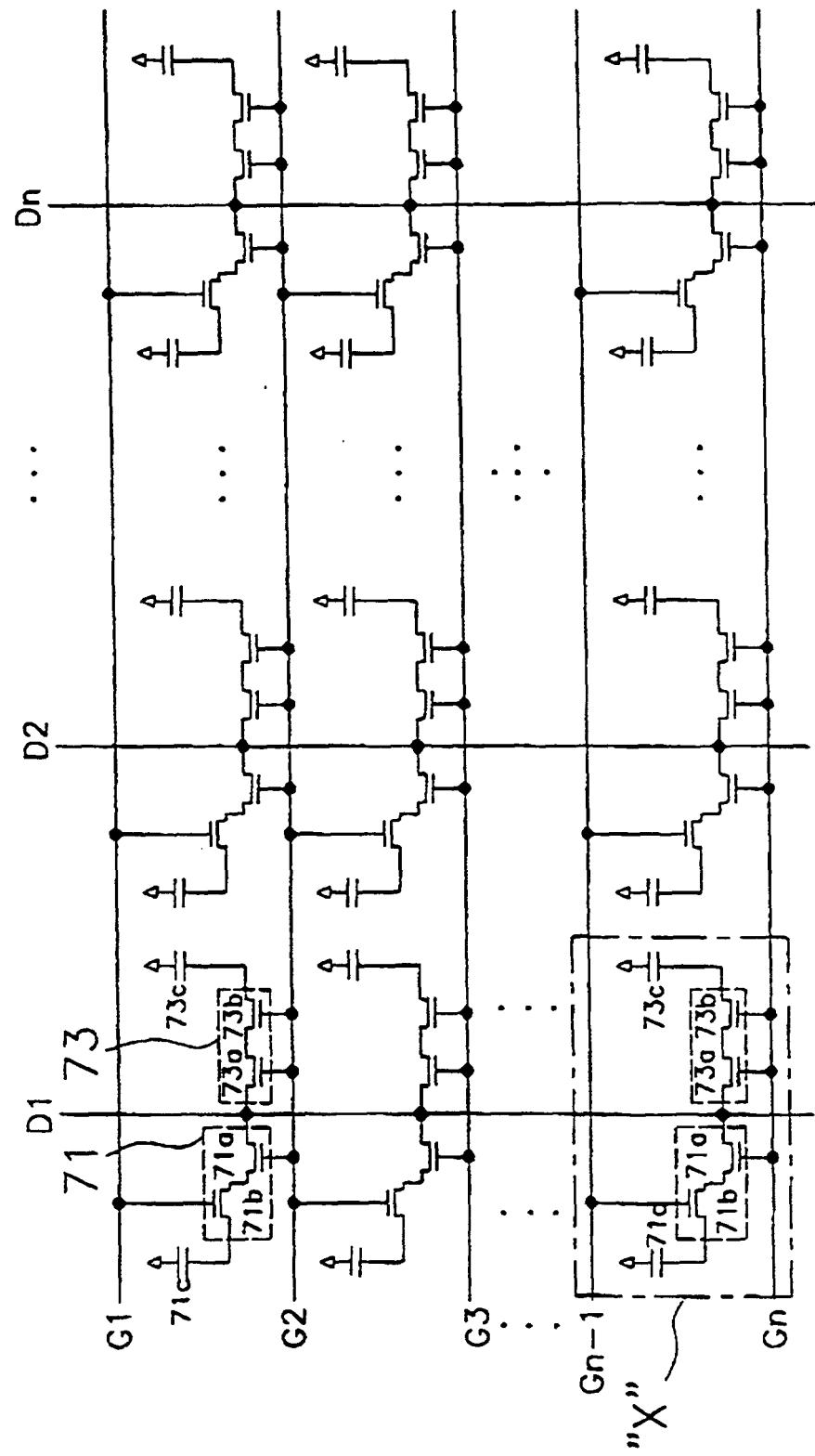


FIG. 11B

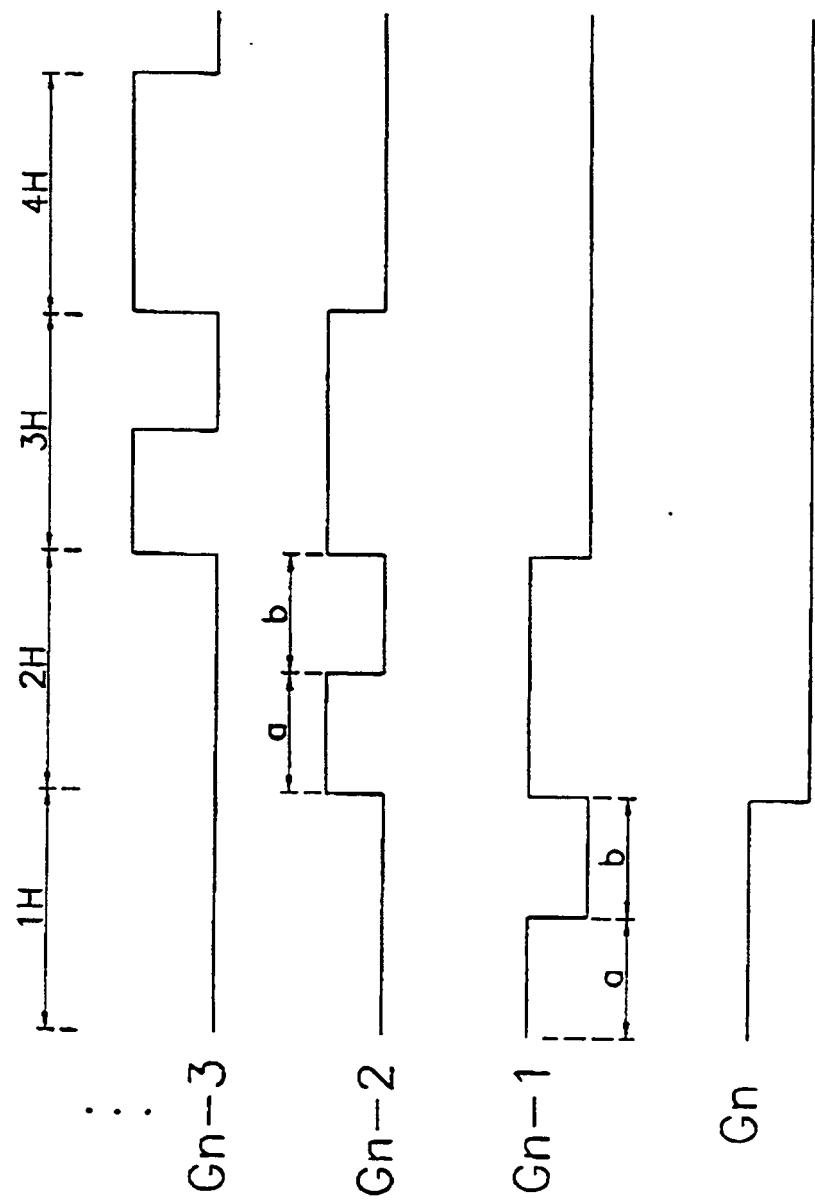


FIG. 12A

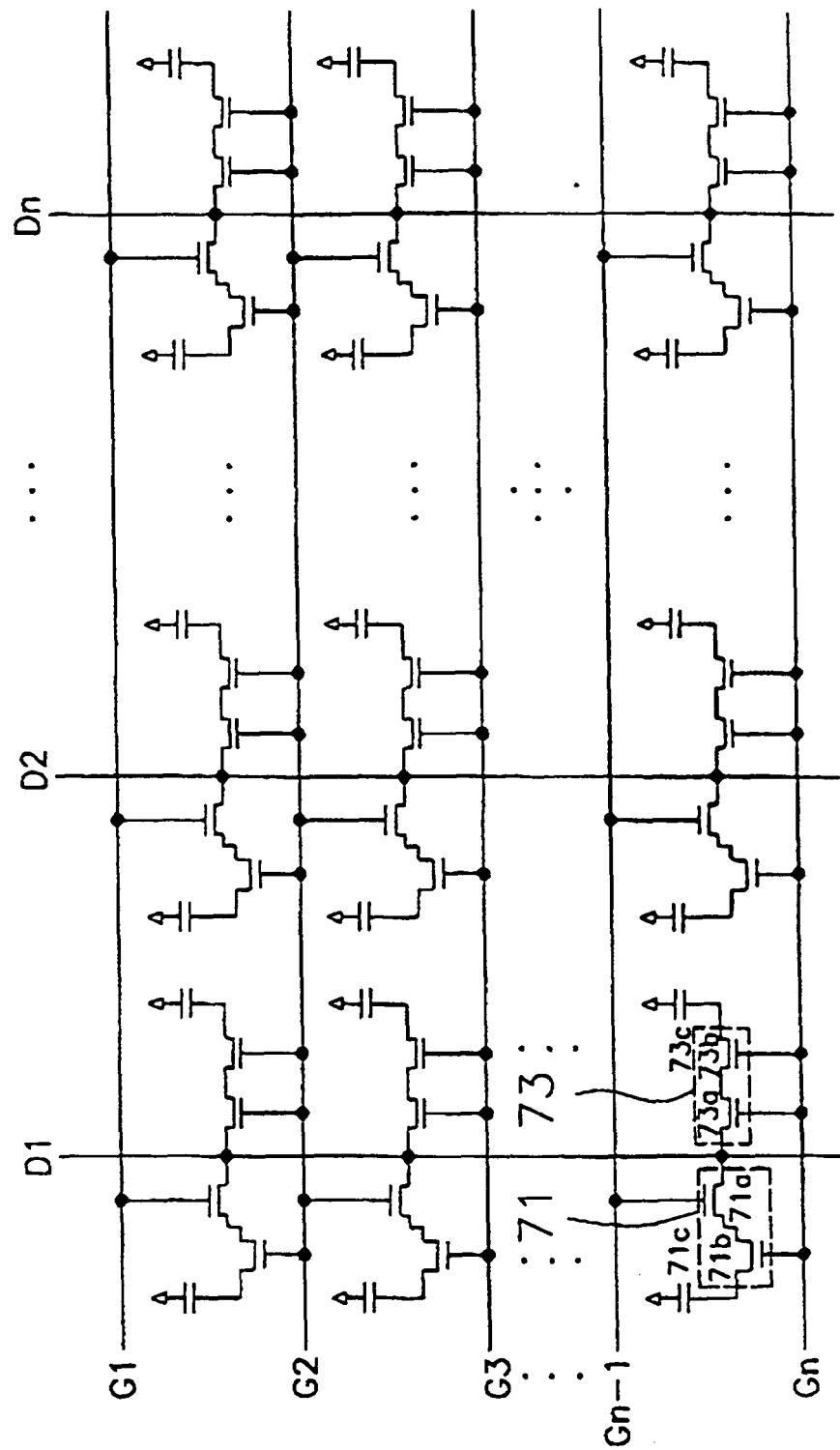


FIG. 12B

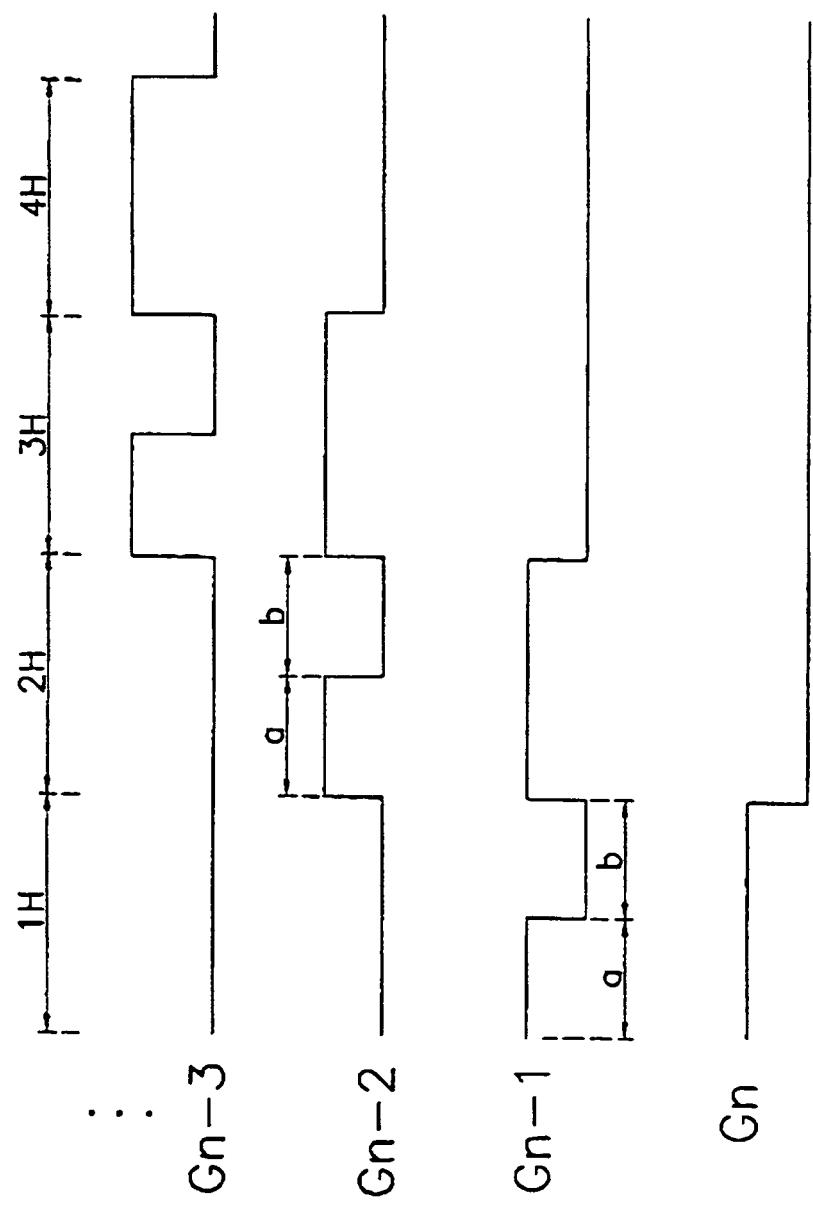


FIG. 13A

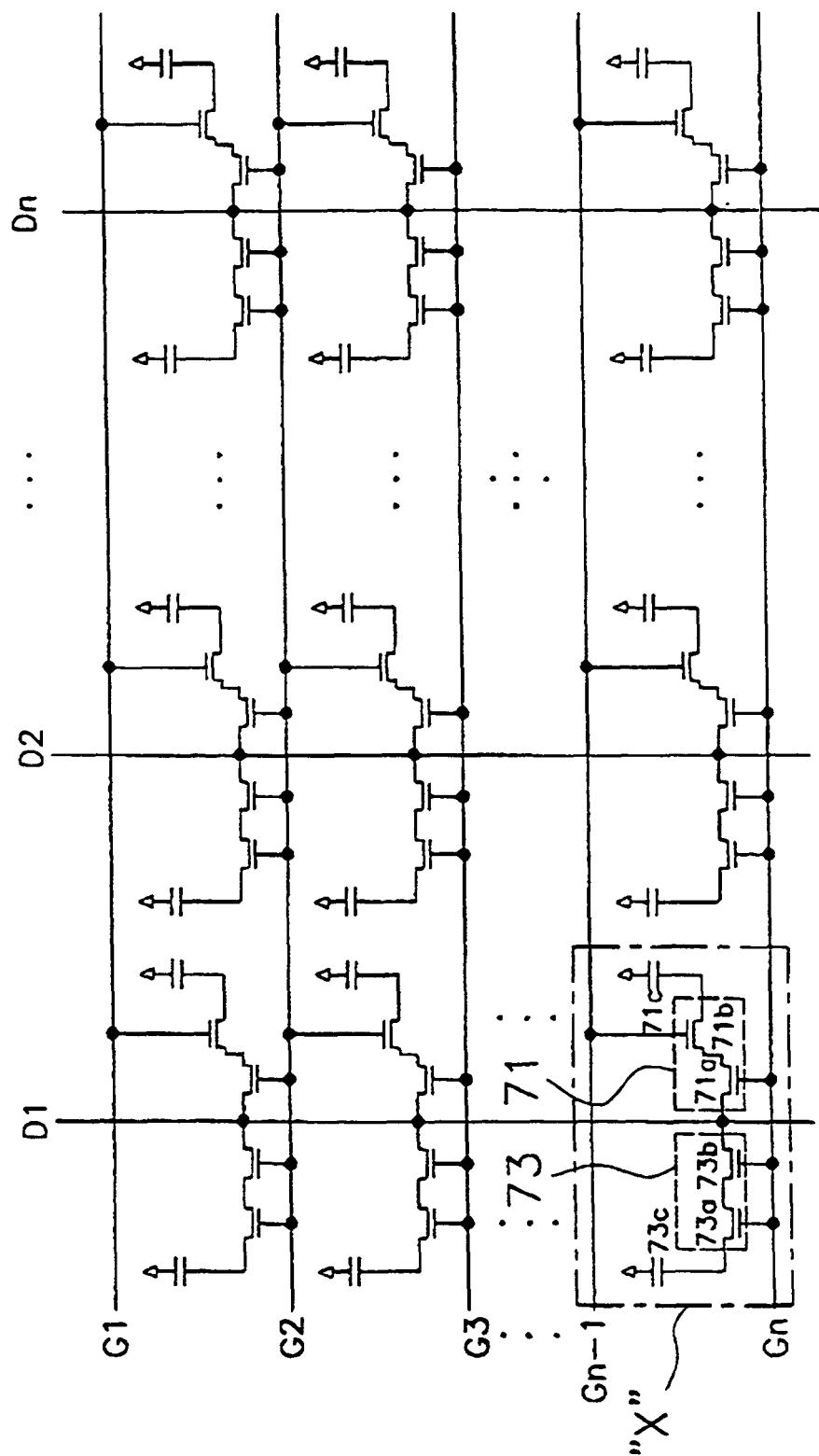


FIG. 1 3B

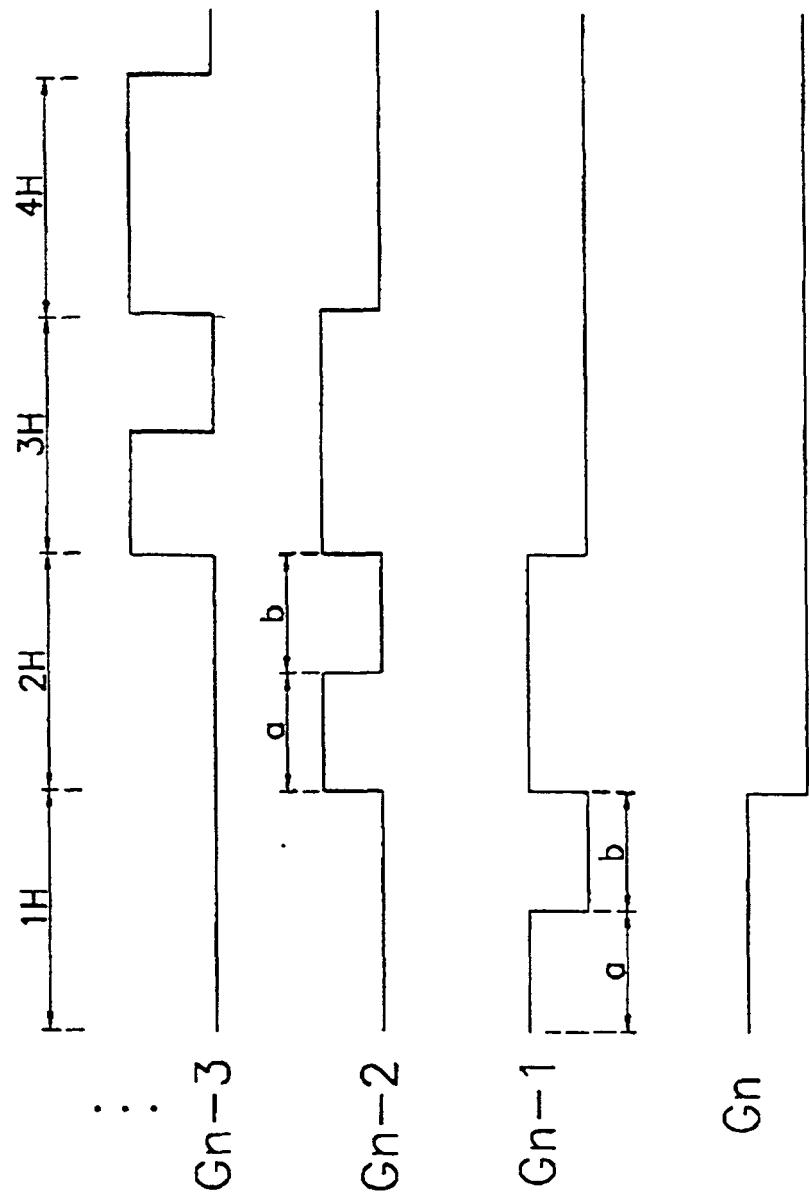


FIG. 14A

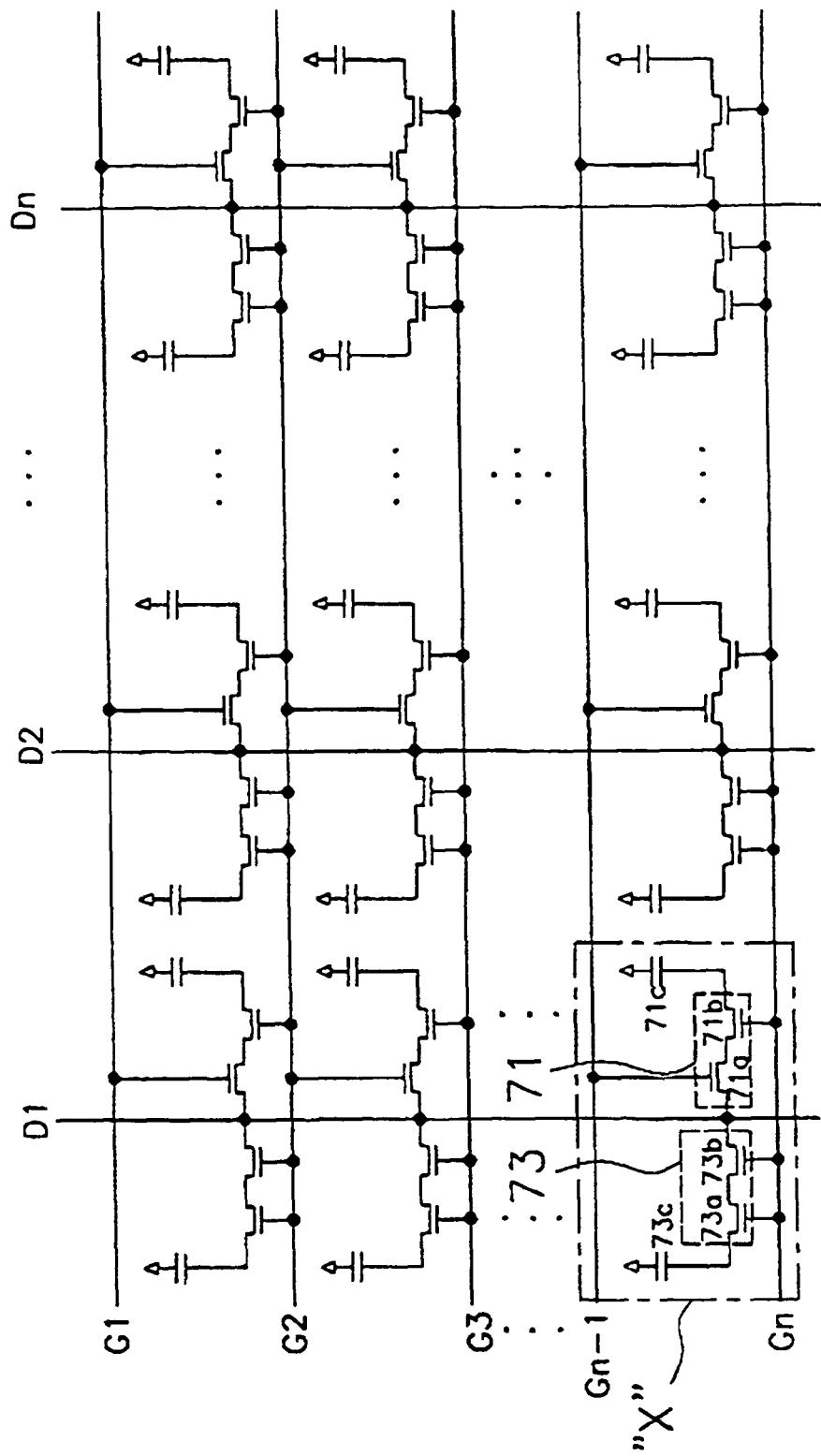


FIG. 14B

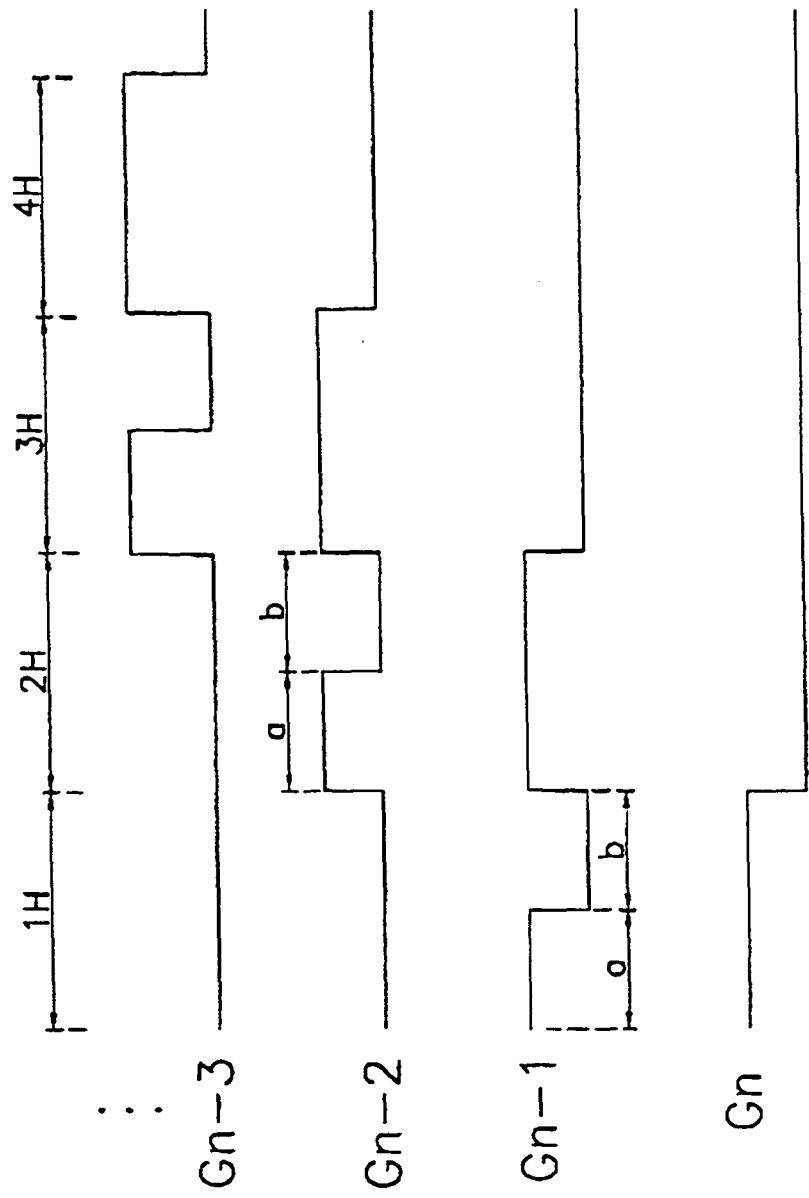


FIG.15A

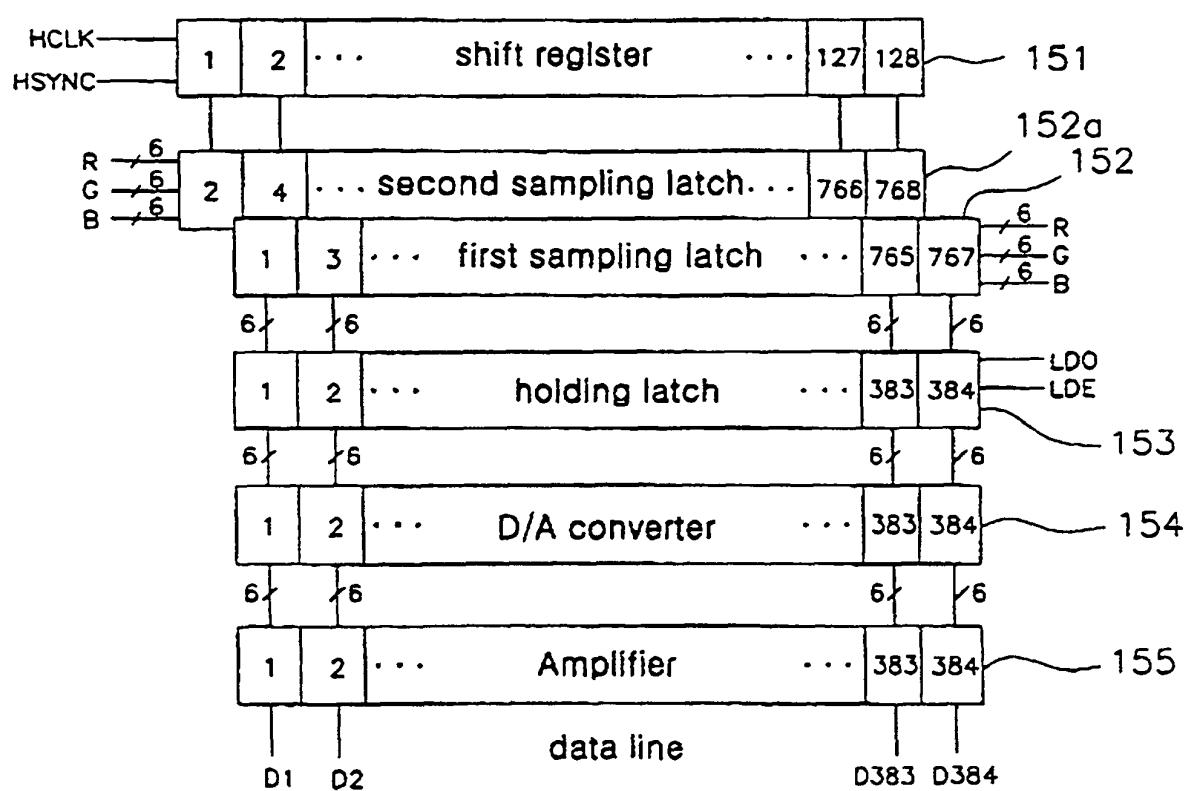


FIG. 15B

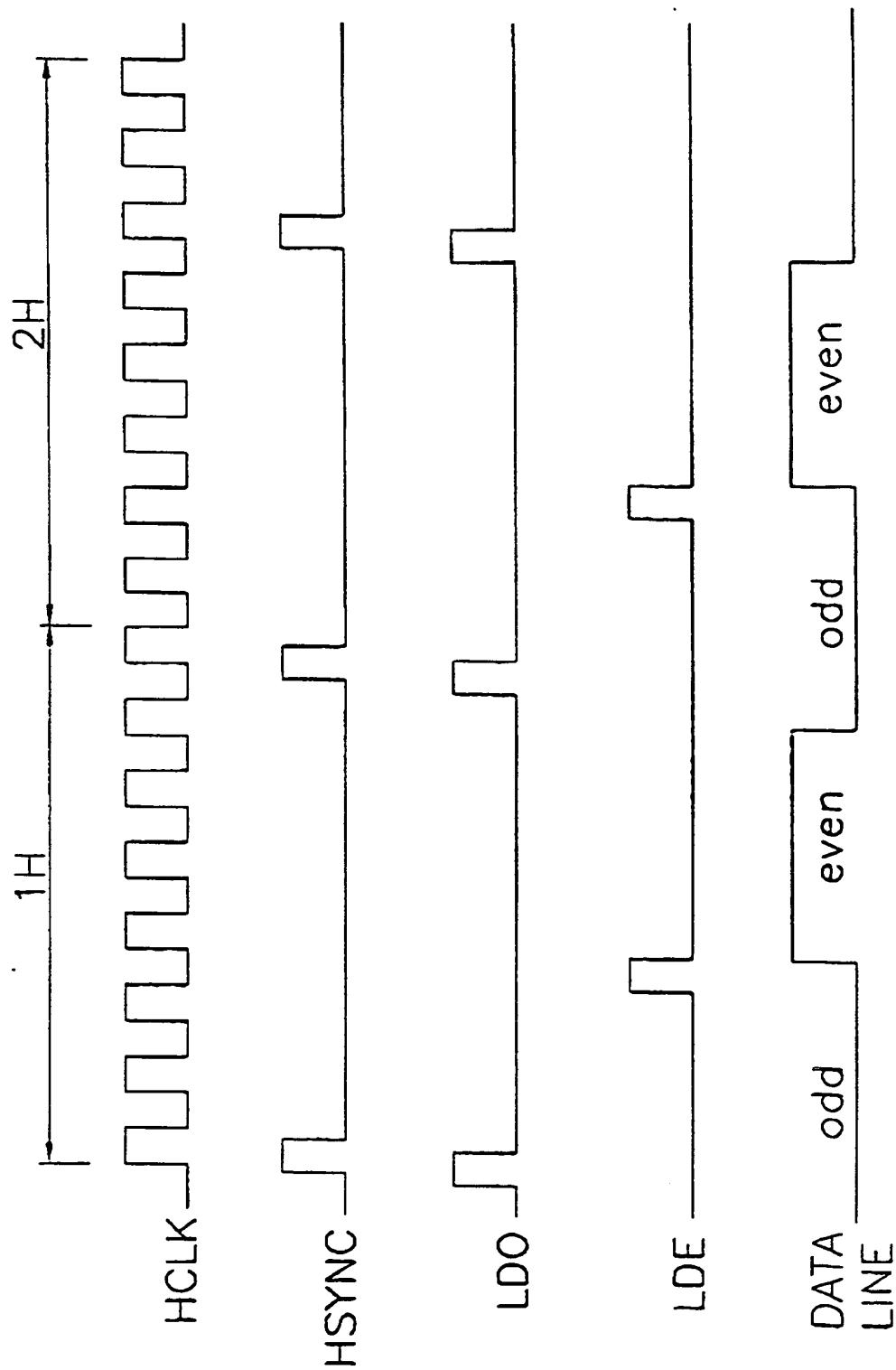


FIG.16A

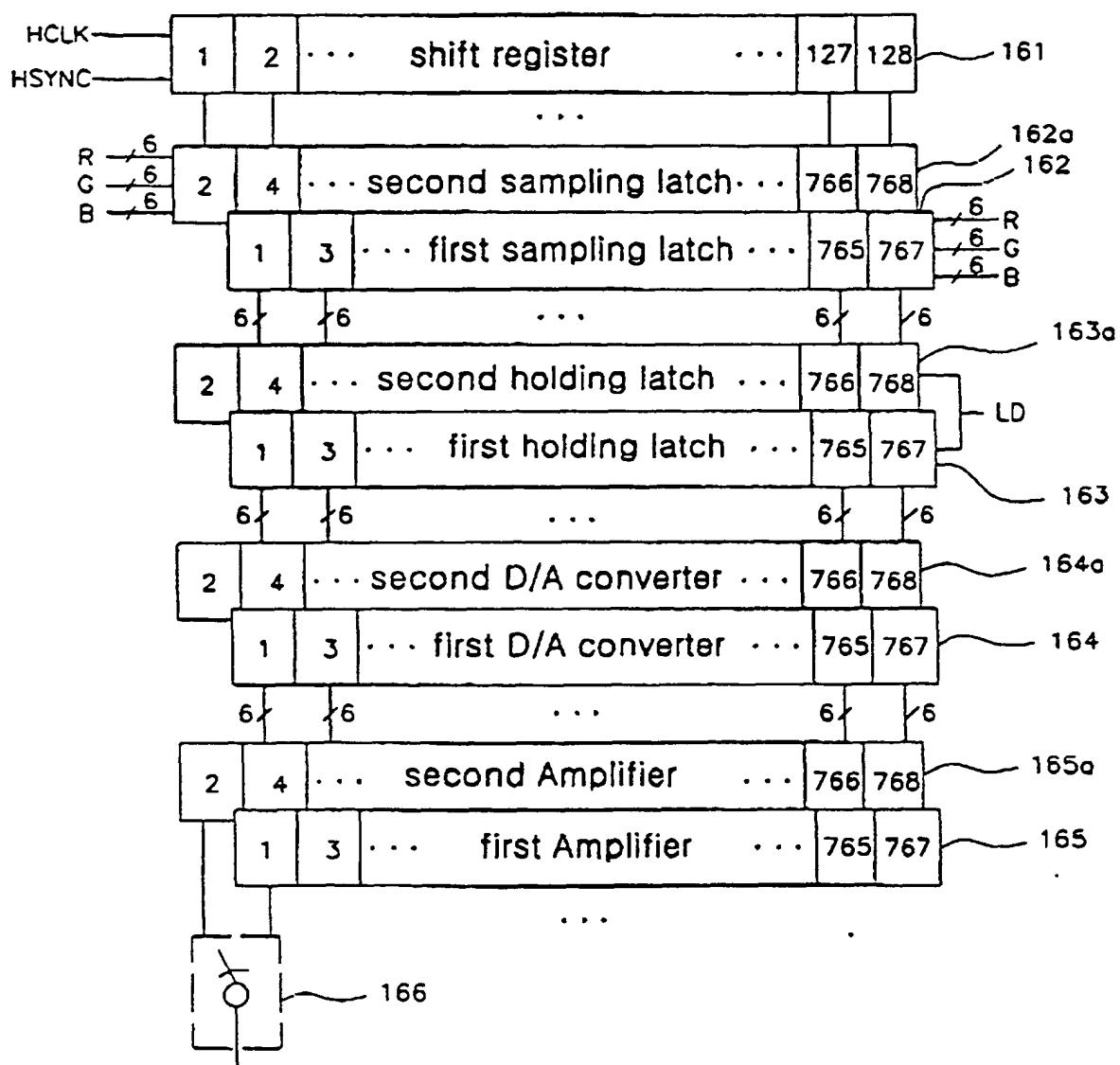


FIG. 16B

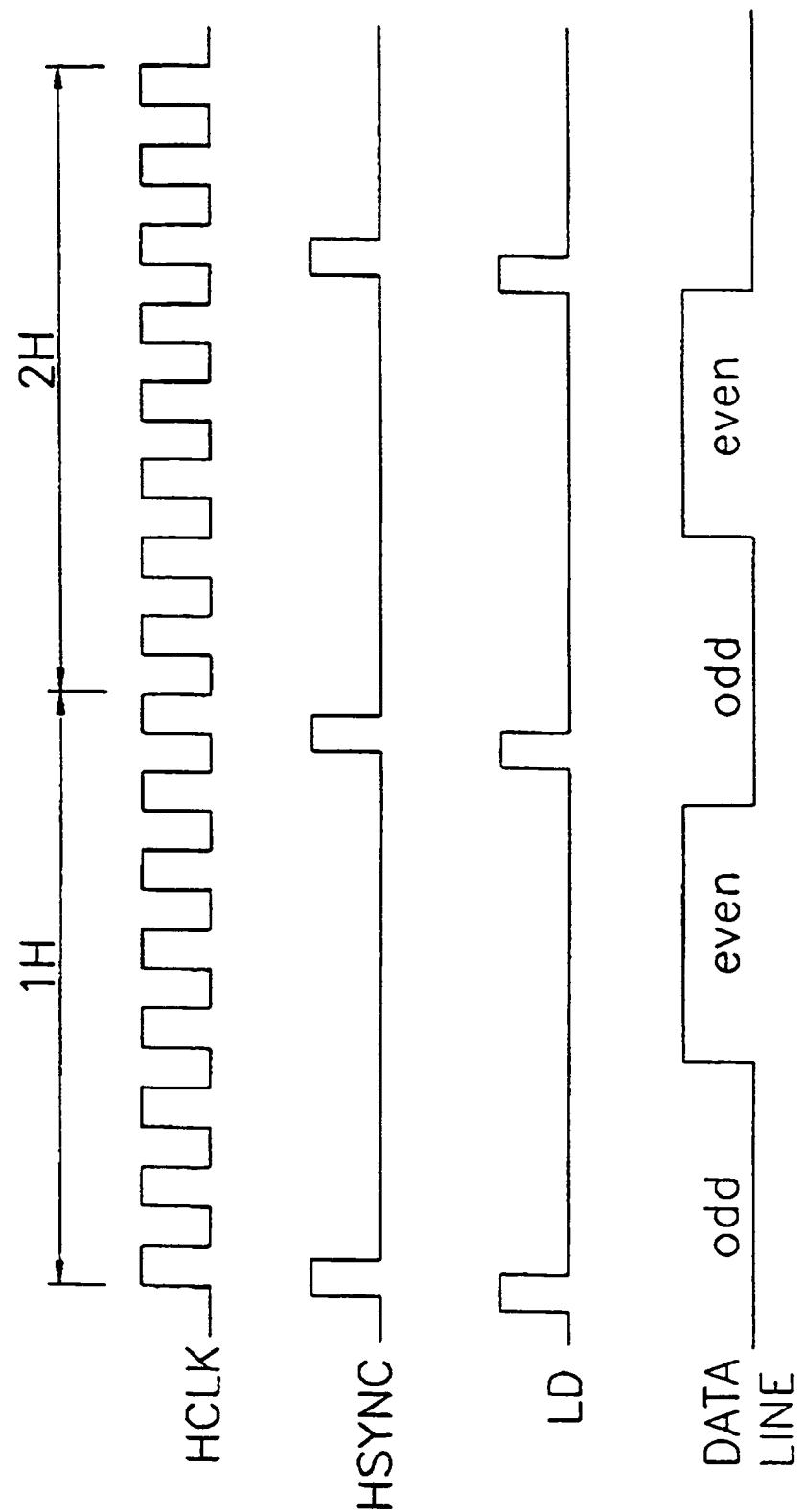


FIG.17A

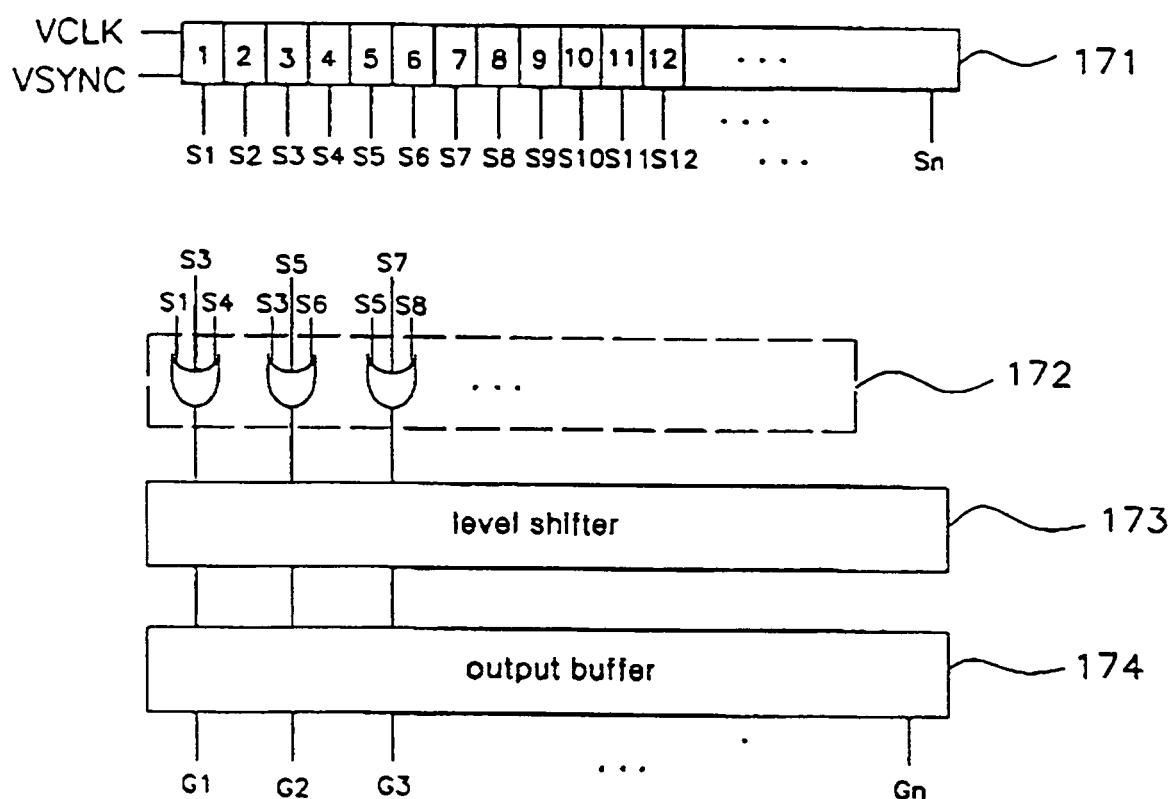


FIG.17B

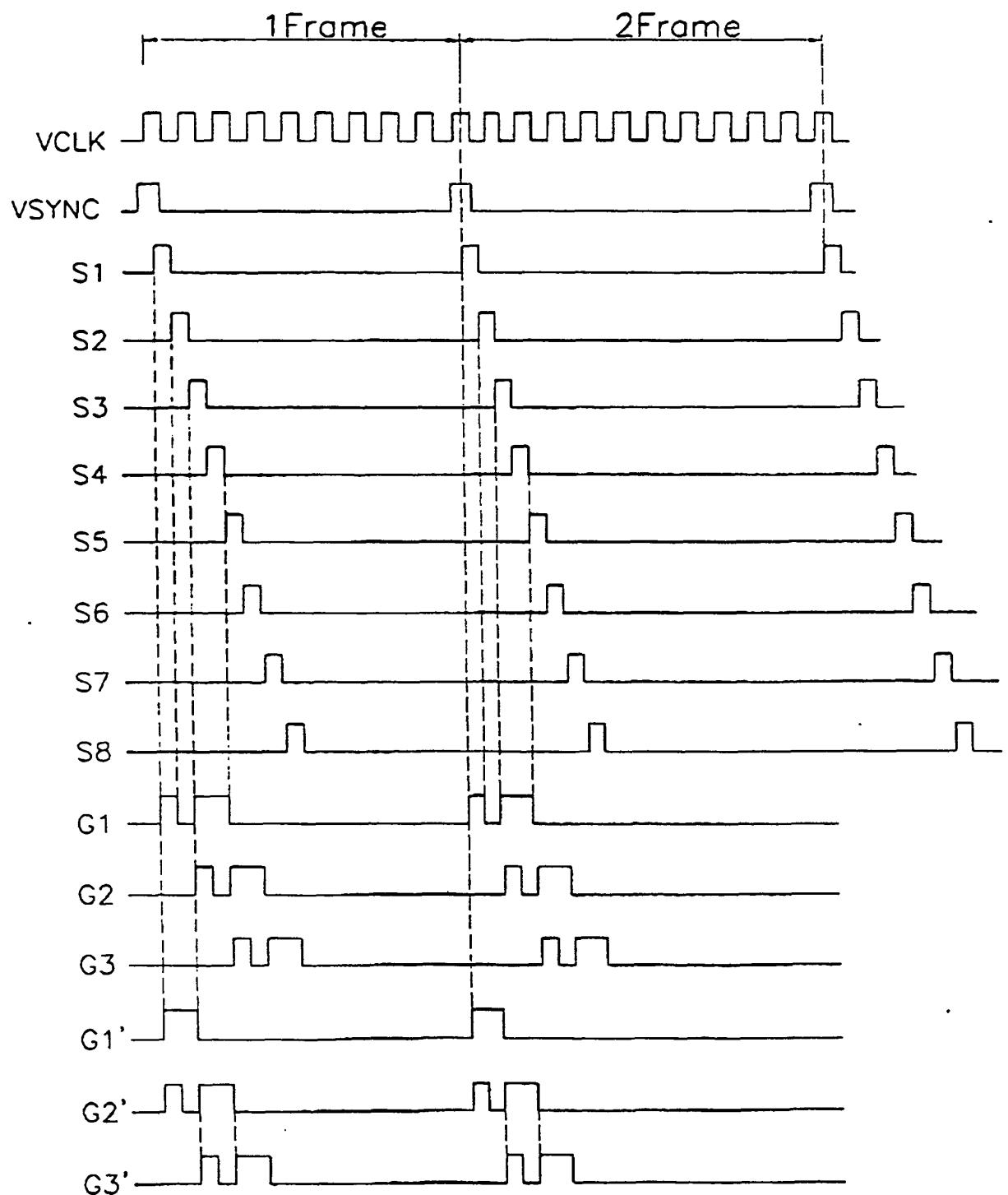


FIG.18

-	-	①+	②+	-	-
+	+	③-	④-	+	+
-	-	+	+	-	-
+	+	-	-	+	+

REFERENCES CITED IN THE DESCRIPTION

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