(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 058 317 B8**

(12) **CORRECTED EUROPEAN PATENT SPECIFICATION**

(15) Correction information:
Corrected version no 1 (W1 B1)
Corrections, see
Bibliography INID code(s) 73

(48) Corrigendum issued on:
04.11.2009 Bulletin 2009/45

(45) Date of publication and mention of the grant of the patent:
02.09.2009 Bulletin 2009/36

(21) Application number: **00401471.8**

(22) Date of filing: **25.05.2000**

(51) Int Cl.:
H01L 29/78 *(2006.01)* ***H01L 21/336*** *(2006.01)*
H01L 29/36 *(2006.01)* ***H01L 29/08*** *(2006.01)*

(54) Low voltage MOS device and corresponding manufacturing process

Niederspannungs-MOS-Anordnung und entsprechendes Herstellungsverfahren

Dispositif MOS faible tension et procédé de fabrication correspondant

(84) Designated Contracting States:
DE FR GB IT SE

(30) Priority: **03.06.1999 US 324553**

(43) Date of publication of application:
06.12.2000 Bulletin 2000/49

(73) Proprietor: **Fairchild Semiconductor Corporation**
South Portland, ME 04106 (US)

(72) Inventors:
- **Zeng, Jun**
  Mountaintop, PA 18707 (US)
- **Wheatley, Carl, Jr.**
  Drums, PA 18222 (US)

(74) Representative: **Bentz, Jean-Paul et al**
Novagraaf Technologies
122 Rue Edouard Vaillant
92593 Levallois-Perret Cedex (FR)

(56) References cited:
EP-A- 0 735 591 **US-A- 4 974 059**

- **PATENT ABSTRACTS OF JAPAN vol. 1998, no. 14, 31 December 1998 (1998-12-31) & JP 10 242458 A (TOSHIBA CORP), 11 September 1998 (1998-09-11)**

EP 1 058 317 B8