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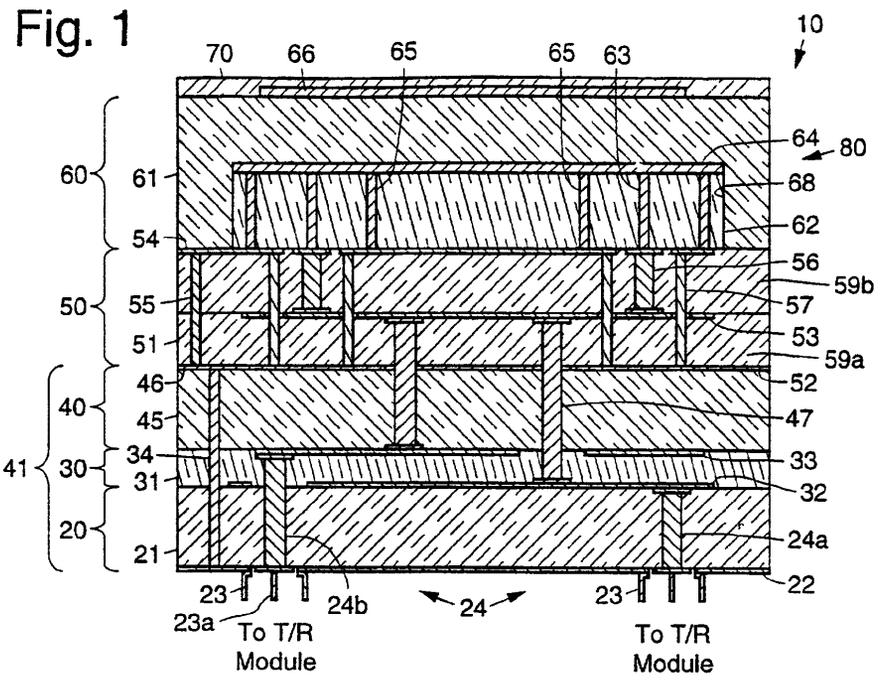
(54) Multiple stacked patch antenna

(57) A planar, low-profile, very wide frequency bandwidth, wide-scan, dual-linear or circular-polarized phased array antenna (90) using integrated stacked-disc radiator tiles (10). The stacked-disc radiator configuration comprises a lower active radiator (64) fed by a pair of probes (63) for each polarization state, and a parasitic radiator (66) separated from the active radiator by dielectric material (61). The stacked-disc radiator is integrated with its multi-layer feed circuits (41, 50) in a very compact package. The feed circuits include 90° hybrid coupler circuits (32, 33) and 180° hybrid coupler circuits (53) that couple dual linear or dual circular polarized energy to and from the disk radiators.

Fig. 1



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Description

BACKGROUND

[0001] The present invention relates generally to phased array antennas, and more particularly, to planar, low profile phased array antennas employing stacked disc radiators.

[0002] The assignee of the present invention has investigated the development of super high frequency phased array antennas for use in various radar and communication applications. Typical applications for such super high frequency phased array antennas include submarine communication systems, ground-based communication systems, radar systems, and satellite communication systems, and the like.

[0003] To this end, the assignee of the present invention has developed several phased array antennas using disc radiator apertures. U.S. Patent No. 5,745,079, entitled "Wide-Scan/Dual-Band stacked disc radiators on stacked dielectric posts phased array antenna", provides for an antenna that exhibits performance over an octave-bandwidth. U.S. Patent No. 5,880,694 entitled "Planar, Low Profile, Wide-Band, Wide Scan Phased Array Antenna Using a Stacked-Disc Radiator", provides for an antenna that exhibits excellent performance while maintaining a planar, low profile.

[0004] Papers have also been published that address prior developments leading up to the present invention. A publication in the 1996 IEEE AP-S International Symposium, Baltimore, Maryland, pp. 1150-1153, entitled "Low-Profile, Broadband, Wide-Scan, Circular-Polarized Phased Array Radiator", discusses the subject matter contained in U.S. Patent Application Serial No. 08/678,383. Another publication in the 1997 IEEE AP-S International Symposium, Montreal, Canada, pp. 702-704, entitled "Planar, Low Profile, Wideband, Wide-Scan Phased Array Antenna Using Stacked-Disc Radiator", discusses the subject matter contained in U.S. Patent No. 5,880,694. The present invention is an improvement to the invention disclosed in U.S. Patent No. 5,880,694. It would therefore be advantageous to have an improved antenna element that permits the construction of planar, low profile, wide-band, wide scan phased array antennas.

[0005] Accordingly, it is an objective of the present invention to provide for an improved antenna element that may be used to construct planar, low profile phased array antennas. It is a further objective of the present invention to provide for an improved antenna employing compact stacked disc radiator elements.

SUMMARY OF THE INVENTION

[0006] To meet the above and other objectives, the present invention provides for a versatile planar, low-profile, very wide frequency bandwidth, wide-scan, circular-polarized phased array antenna using integrated radiator tiles comprising stacked-disc radiators. The present invention comprises a stacked-disc radiator configuration where a lower active radiator is fed by a pair of probes for each linear polarization, and a parasitic radiator separated from the active radiator by dielectric material. The stacked-disc radiator is integrated with its feed circuits in a very compact and versatile package. The integration of the stacked disc radiator and its compact multilayer feed circuits are described herein. The feed circuits may include power combiners, 90° hybrid coupler circuits and 180° hybrid coupler circuits that couple dual linear or dual circular polarized energy to and from the disk radiators.

The present invention may be employed in ground-based, shipboard, airborne, and radar and satellite communication systems that operate using wide-band, wide scan phased array antennas with dual linear or dual circular polarization. The integrated stacked-disc radiator tiles are ideal for use in conformal phased array antenna applications. In addition to providing wide-band and wide scan performance, the integrated radiator tiles are planar, low profile, and light weight, can be produced inexpressively using printed circuit technology, and its form factor allows the arrays to be easily maintained. In general, the integrated radiator tile lends itsel well to many conformal applications and tile array architectures.

[0007] The present invention integrates the radiator (stacked-disc radiator) with its feed circuits. The resulting package, or integrated radiator tile, is very wideband (45% bandwidth) and provides a wide-scan and good axial ratio (circular polarization purity). The design of the integrated radiator tile provides for polarization diversity. Thus, changing feed circuits can provide, linear, dual-linear, and dual-circular polarization capability.

[0008] The packaging of the integrated radiator tile is compactly constructed using multilayer laminated printed circuit technology. Thus, the integrated radiator tiles can be inexpensively constructed. The dielectric materials that are laminated to produce the multilayer integrated radiator tile have comparable coefficients of thermal expansion. Furthermore, use of the integrated radiator tiles of the present invention greatly improves the assembly and maintainability of phased array antennas that employ them.

The feed circuits and number of circuit layers in the integrated radiator tile are a function of the application in which the tile is used. These aspects change depending on whether the tile has a linear or circular polarized configuration, whether the stacked disk radiator can be block-fed, whether the design requires an external coaxial connector, and so on. The stacked-disc radiator can provide an octave bandwidth. The feed circuits that drive the stacked-disc radiator provide a means to achieve this octave bandwidth. The integrated radiator tile uses wideband feed circuits that are compactly constructed and that are integrated with the stacked-disc radiator in an low-cost package. The bandwidth of the

feed circuits and vertical RF transitions essentially determine the overall bandwidth performance of the integrated radiator tile. Integrated radiator tiles have been constructed that can cover 45% bandwidth.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like structural elements, and in which

Fig. 1 shows an enlarged partial cross-sectional view of a portion of an integrated radiator tile in accordance with the principles of the present invention that illustrates its multi-layer construction;
Fig. 2a illustrates an enlarged top view of the integrated radiator tile of Fig. 1;
Fig. 2b illustrates an enlarged bottom view of the integrated radiator tile of Fig. 1;
Fig. 3 illustrates a feeding arrangement for achieving dual circular polarization using the integrated radiator tile of Fig. 1;
Fig. 4 illustrates an exploded view of the multilayer feed circuit structure used in the integrated radiator tile of Fig. 1;
Fig. 5 illustrates the stacked disc radiator feed layout used in the integrated radiator tile of Fig. 1, showing superimposed internal circuit layers;
Fig. 5a shows a plan view of the balun layer and modified ratrace 180° hybrid coupler circuit used in the integrated radiator tile of Fig. 1;
Fig. 6 shows a waveguide simulator measurement for the integrated radiator tile of Fig. 1;
Fig. 7 shows insertion loss resulting from the combined 90° and 180° hybrid circuits shown in Fig. 3;
Fig. 8 shows insertion phase resulting from the combined 90° and 180° hybrid 25 circuits shown in Fig. 3;
Fig. 9 shows the measured embedded element gain of the integrated radiator tile of Fig. 1;
Fig. 10a shows a 6 by 6 test antenna array constructed using a plurality of intehgrated radiator tiles; and
Fig. 10b shows the measured element pattern of a 6 by 6 integrated radiator tile test antenna array.

DETAILED DESCRIPTION

[0010] Referring to the drawing figures, Fig. 1 shows an enlarged partial cross-sectional view of a portion of an integrated radiator tile 10 in accordance with the principles of the present invention and which illustrates its multi-layer construction. The integrated radiator tile 10 includes a stripline circuit board 41 having a bottom dielectric layer 20 comprising dielectric material 21 having a dielectric constant of 3.27, for example, and having a conductive ground plane 22 disposed on an exposed surface thereof. First and second coaxial connectors 23 (such as commercial SSMP coaxial connectors 23, for example) are attached to the ground plane 22 by means of solder, for example, and have center pins 23a connected to conductive vias 24 formed trough the botton dielectric layer 20 that each comprise stripline to coaxial transitions 24 in the exemplary embodiment. Alternatively, a connectorless design is also possible by having a coax-like structure (including either fuzz-button or pin, with outer dielectric shell) coming from below and making direct contact to RF vias 24.

[0011] A 90° coupling circuit layer 30 is attached to the top of bottom dielectric layer 20. The coupling circuit layer 30 comprises bottom and top circuits 32, 33 formed on opposite sides of a dielectric layer 31. The bottom and top circuits 32, 33 comprise a middle layer of the 90° coupler circuit layer 31. A first vertical transitions 24a connects the bottom RF trace 32 to one coaxial connector 23 through the bottom dielectric layer 20. The other of the RF trace 33 connects to the other coaxial connector 23 through the bottom dielectric layer 20 and middle dielectric layer 31 by way of a second vertical RF transition 24b. The vertical transitions 24a, 24b are substantially perpendicular to the stripline circuit board 41, which helps to produce a compact low profile design.

[0012] The stripline circuit board 41 comprises an intermediate dielectric layer 40 made of dielectric material 45 having a dielectric constant of 3.4, for example, that is disposed between the coupling circuit layer 30 and a balun layer 50. The balun layer 50 has a lower ground plane 52 formed on a surface that is adjacent to the intermediate dielectric layer 40, and an upper ground plane 54 that is formed on its upper surface. The balun layer 50 is comprised of two dielectric boards. One of the dielectric boards 59a has the bottom ground plane 52. The other dielectric board 59b has the top ground plane 54. A plurality of grounding vias 55 are coupled between the lower and upper grottnd planes 52, 54 of the balun layer 50 and also around the RF vias (i.e., vias 24a, 47, 56, or 63). The plurality of grounding vias 55 function to provide a coax-like cross-section at the transition and to prevent the excitation of higher-order modes. A plurality of grounding vias 34 are also coupled between the lower ground plane 52 of the balun layer 50 and the bottom ground plane 22 disposed on the exposed surface of the bottom dielectric layer 20. The plurality of grounding vias 34 serve the same function as the vias 55 relative to layer 50. The locations of the grounding vias 55 are shown more clearly in Fig. 5a.

[0013] The balun layer 50 comprises 180° hybrid coupler circuits 53 that are implemented using modified retrace couplers 53a (Fig. 5). The balun layer 50 has an upper ground plane 54 formed adjacent to a surface. A plurality of RF transitions 47 are coupled between the balun layer 50 and the respective bottom and top strip-

line circuits 32, 33. The transitions 47 are in the form of vertical transitions which are perpendicular to the stripline circuit board. A plurality of RF transitions 56 are coupled between the 180° hybrid coupler circuits 53 and the upper surface of the balun layer 50. A plurality of ground vias 57 surround each of the radiator to RF transitions 56 that extend from the upper ground plane 54 to the lower ground plane 52.

[0014] An upper dielectric layer 60 comprising a relatively low dielectric constant material is disposed adjacent to the balun layer 50. The dielectric constant of the upper dielectric layer 60 is typically on the order of 1.7, for example. Emerson & Cuming Stycast material may be used as the upper dielectric layer 60. The upper dielectric layer 60 may be made of a low-dielectric constant foam material.

[0015] An a preferred embodiment, the upper dielectric layer 60 has a plurality of cylindrical recesses 68 formed therein into which a plurality of dielectric pucks 62 are disposed. The dielectric pucks 62 may be formed using Rogers TMM 3 dielectric material having a dielectric constant of 3.27, for example. Disposing the dielectric pucks 62 in the recesses 68 reduces the overall thickness of the integrated radiator tile 10. However, it is to be understood that the dielectric pucks 62 need not be disposed in the recesses 68 and surrounded by dielectric material, but may be surrounded entirely or partially by air dielectric for example.

[0016] The dielectric pucks 62 have an active radiator 64 formed on their upper surfaces. The plurality of probes 63, comprising metallized vias 63, formed through the dielectric pucks 62 are coupled at one end to the active radiator 64. The plurality of radiator to stripline transitions 56 are coupled between the 180° hybrid coupler circuits 53 and the probes 63. The dielectric puck 62 is surrounded by dielectric material 61 having a dielectric constant of about 1.70.

[0017] A parasitic radiator 66, or parasitic patch 66, is disposed on an upper surface of the upper dielectric layer 60. The parasitic radiator 66 is separated from the active radiator 64 by dielectric material 61. The active radiator 64, the parasitic radiator 66, the dielectric puck 62, and the low-dielectric constant upper dielectric layer 60 form a stacked-disc radiator 80. A radome layer 70 is disposed over the upper surface of the upper dielectric layer 60 and the parasitic radiator 66 to provide protection from the environment and improve the impedance match. A flat foam spacer may be disposed between dielectric puck 62 and the radome 70. A plurality of metallized vias 65 surround each of the probes 63 which function to control the radiating pattern of the stacked-disc radiator 80.

[0018] Thus, in the exemplary embodiment of the present invention, the stacked-disc radiator 80 is disposed over two laminated stripline circuit boards containing the 90° hybrid coupler circuits 30 and the 180° hybrid coupler circuits 53. The topmost stripline circuit board is the balun layer 50 containing the 180° hybrid coupler circuits 53 and the lower stripline circuit board is the coupling circuit layer 41 containing the 90° hybrid coupler circuits 32, 33. However, it is to be understood that more than two laminated stripline circuit boards may be employed, depending upon the application.

[0019] Fig. 2a illustrates an enlarged top view and Fig. 2b illustrates an enlarged bottom view of the integrated radiator tile 10 of Fig. 1, respectively. Fig. 2a shows the relative positions of each of the parasitic patches 66 covered by the radome layer 70. The locations of the coaxial connectors 23 on the bottom surface of the integrated radiator tile 10 is shown in Fig 2b. A central through hole 75 is disposed through the integrated radiator tile 10 that is used to secure the tile 10 and is shown in both Figs 2a and 2b. Invention is not limited to a 2x2 tile, could be any size.

[0020] Multiple feed circuits may also be implemented, as in the case where the radiators are block-fed. The figure shows a 2x2 tile. The plurality of radiators ion a tile depends on fabrication yield as well as specific application requirements. It is also possible to have designs without coaxial connectors 23.

[0021] Fig. 3 illustrates a feeding arrangement for achieving dual circular polarization using the integrated radiator tile 10 of Fig 1. Metallized vias 63 serve as the probes 63 for the stacked-disc radiator 80 and vias 24, 47, 56 (shown in Fig. 1) serve as vertical RF interconnects between the various feed layers.

[0022] The feeding arrangement produces both senses of circular polarization. The four probes 63 of each integrated radiator tile 10 are excited in phase sequence in the manner shown in Fig. 3. This may be achieved by feeding two orthogonal pairs of probes 63 using two 180° hybrid coupler circuits 53 and combining the outputs with a 90° hybrid coupler circuit 33.

[0023] More specifically, the 90° hybrid coupler circuit 33 receives left hand circularly polarized (LHCP) and right hand circularly polarized (RHCP) excitation 10 signals. In transmit mode, 0° and 90° outputs of the 90° hybrid coupler circuit 33 are coupled to first and second 180° hybrid coupler circuits 53, respectively. The 0° output of the 90° hybrid coupler circuit 33 feeds the first 180° hybrid coupler circuit 53, while the 90° output of the 90° hybrid coupler circuit 33 feeds the second 180° hybrid coupler circuit 53. 0° and 180° outputs of the first 180° hybrid coupler circuit 53 are coupled to probes 63 located at 0° and 180°, respectively. 0° and 180° outputs of the second 180° hybrid coupler circuit 53 are coupled to probes 63 located at 90° and 270°, respectively. Dual linear polarization can also be easily attained by removing the 90° hybrid coupler (hence layer 41) and taking the outputs signals of 57.

[0024] Fig. 4 shows an exploded view of the multilayer feed circuit structure used in the integrated radiator tile 10 of Fig. 1. Selected layers are shown without having apparent thickness and illustrate surface features thereof. Fig. 4 shows the radiator tile is constructed as a multilayer laminated structure. Its dielectric materials are

carefully chosen to have comparable coefficients of thermal expansion to ensure successful lamination of the boards.

[0025] Fig. 5, 5a illustrates the radiator feed layout for the stacked disc radiator 80 used in the integrated radiator tile 10 of Fig. 1. Fig. 5 contains superimposed internal circuit layers. The radiator feed layout has a plurality of transmit ports 81 and a plurality of receive ports 82 that are coupled to the coaxial connectors 23. The locations of the probes 63 below the active radiators 64 and parasitic patches 66 are shown. The configuration of the modified retrace 180° hybrid coupler circuit 53a is shown in Fig. 5. The configurations of the bottom and top stripline circuits 32, 33 of the coupling circuit layer 30 are shown in Fig. 5. The locations of 180° ratrace to 90° coupler transition comprising the metallized vias 47 are shown in Fig. 5. All circuits (180° hybrid, 90° coupler, and the vertical RF transitions) are designed for wideband performance. For clarity, Fig 5a shows a plan view of the balun layer 50 and modified ratrace 180° hybrid coupler circuit 53.

[0026] The integrated radiator tile 10 is configured as a 2 by 2 element subarray that is designed to interface directly with transmit/receive (T/R) module tiles. The overall thickness of the integrated radiator tile 10 is approximately 0.4" which also includes a mechanical support layer (not shown) behind the multi-layer stripline feed. The radiator layers make up about half (-0.2") of the overall thickness of the integrated radiator tile 10. Eight commercial SSMP coaxial connectors 23 are connected on the back side of the integrated radiator tile 10 that connect to outputs of the T/R module tiles (which also use mating SSMP connectors). There are two connectors 23 for each stacked-disc radiator 80 that provide for separate transmit and receive paths. The radome 70 seals the aperture from the environment.

[0027] The modified ratrace coupler 53a serves as a balun for stacked-disc radiator 80, providing the necessary 180° phase difference between the pair of probes 63. The modified ratrace couplers 53a are configured using additional traces that increase the overall bandwidth of the conventional ratrace coupler by about 150 percent. The modifcation involves adding an additional loop to the conventional ratrace ring hybrid geometry to increase bandwidth operation. Two of the 180° hybrid coupler circuits 53 are packaged on a single layer stripline board 50 under each stacked-disc radiator 80. Since the radiator tile contains four radiators, Figure 5a shows that the 180° layer 50 for the 2x2 tile has a total of 8 ratrace couplers. The two outputs of the 180° hybrid circuits transition to 90° hybrid circuits 32, 33 located on the lower coupler stripline circuit board 30.

[0028] Fig. 6 shows a waveguide simulator measurement for the integrated radiator tile 10 of Fig 1. A waveguide simulator was used to test the integrated radiator tile 10 and 180° hybrid coupler circuits 53, which produced the test results shown in Fig. 6. The two traces shown in Fig. 6 correspond to the two orthogonal orientations of the radiator tile 10. These results agree well with predicted performance. The best performance was obtained between 7 and 9 GHz (~15 dB return loss) with scan performance degrading at higher frequencies as designed due of the large lattice spacing selected for this application.

[0029] Fig. 7 shows insertion loss resulting from the combined 90° and 180° hybrid circuits 41, 50 shown in Fig 3. Fig. 8 shows the measured insertion phase resulting from the combined 90° and 180° hybrid circuits 41, 50 shown in Fig. 3. Both figures show 4 traces, which correspond to the four outputs of the combined circuit (assume input at one via 24a and output at four vias 56 of each radiator). The measured data show excellent performance-no worse than 6° from ideal over the entire frequency bandwidth except at the band edges, where it degrades to about 14°.

[0030] The combined circuits provided both senses of circular polarization. The four traces shown in Fig. 7 tracked each other very well. The two inputs of the combined circuits (same as the two outputs of the 90° hybrid circuit 30) match with the two outputs of the T/R module for each radiating element. The four outputs of the combined circuits (same as the four outputs of the 180° hybrid circuit) were transitioned to the stacked-disc radiator 80 through the four metal probes 63 (vertical RF interconnects). The measured 1.6 dB loss for the test circuits was close to expected considering that relatively hard, lossy material (Rogers R4003) was used for the stripline boards 30, 50, and there were three vertical RF transitions 24, 47, 56 in the multi-layer circuit.

[0031] Fig. 9 shows the measured element embedded gain of the integrated radiator tile of Fig. 1. The measured embedded element gain is consistent with predicted values except for the large ripples due to small aperture size. The measured gain was roughly 2 dB lower than area gain due to the mismatch and line loss.

[0032] A plurality of the integrated radiator tiles 10 described above may be readily secured together to form an antenna array. Fig. 10a shows an exemplary 6 by 6 test antenna array 90 constructed using a plurality of integrated radiator tiles 10. Fig. 10b shows the measured embedded element pattern of a 6 by 6 test antenna array 90 built using integrated radiator tiles 10 to validate aperture performances. The integrated radiator tiles 10 are designed to operate from 7 GHz to 11 GHz. The embedded element pattern held up well to 45° in all plane cuts up to nearly 9 GHz which is consistent with predictions. Thus, the predicted and measured performance of the planar, low-profile integrated radiator tile 10 of the present invention meet requirements of conformal phased array applications for radar and satellite communication systems such as those developed by the assignee of the present invention.

[0033] The parasitic radiator 66 is parasitically excited, and is not directly fed by the probes 63. In the presence of mutual coupling, the lower active radiator 64 is tuned to operate at a lower frequency band, while the

parasitic radiator 66 is tuned to higher frequencies. Consequently, the operational bandwidth of the integrated radiator tile 10 is extended to encompass the lower and higher frequency bands. The two pairs of probes 63 provide dual-linear polarization and circular polarization capability. More particularly, the polarization of the integrated radiator tile 10 may be single linear polarization, dual linear polarization, or circular polarization depending on whether a single pair or two pairs of probes 63 are excited.

[0034] Parameters for an exemplary embodiment of the integrated radiator tile are as follows. The spacing between each of the stacked-disc radiators 80 may be 0.78" in a rectangular lattice. The dielectric puck 62 may have a dielectric constant of 3.27, a diameter of 0.535", and thickness of 0.12". The dielectric material 61 may surround puck 62 and have a dielectric constant of about 1.70, and a thickness of 0.061" over puck 62. The lower active disc radiator 64 may have a diameter of 0.535"; and the upper parasitic radiator 66 may have a diameter of 0.320". The radome may have a average dielectric constant of 2.56, and a thickness of 0.060". The separation between each pair of probes 63 may be 0.330".

It is to be understood that the feed circuits and the number of circuit layers in the integrated radiator tile 10 may differ from the exemplary embodiment disclosed herein, depending on the application, i.e., whether it is linear or circular polarized, whether the stacked disk radiator 80 can be block-fed, or whether the design requires an external coaxial connector, for example. The stacked-disc radiator 80 used in the integrated radiator tile 10 can provide an octave bandwidth. The feed circuits disclosed herein that drive the stacked-disc radiator 80 provide the means to achieve this octave bandwidth. The integrated radiator tile 10 uses wideband feed circuits that are compactly constructed and that are integrated with the stacked-disc radiator 80 in a low-cost package. The bandwidth of the feed circuits and vertical RF transitions essentially determine the overall bandwidth performance of the integrated radiator tile 10. Integrated radiator tiles 10 have been constructed that can cover 45% bandwidth.

[0035] Thus, low profile integrated radiator tiles comprising stacked disc radiators for use in phased array antennas have been disclosed. It is to be understood that the described embodiment is merely illustrative of some of the many specific embodiments which represent applications of the principles of the present invention. Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.

Claims

1. An integrated radiator tile (10) for use in a phased array antenna, characterized by:

a bottom dielectric layer (20) having a ground plane (22) disposed on an exposed surface, and having first and second via transitions (24a, 24b) formed through the bottom dielectric layer;

a coupling circuit layer (30) adjacent to the bottom dielectric layer comprising 90° hybrid coupler circuits (32, 33) respectively coupled to the first and second via transitions;

a balun layer (50) adjacent to the coupling circuit layer comprising lower and upper ground planes (52, 54) formed on opposite surfaces, 180° hybrid coupler circuits (53), a plurality of RF transitions (47) selectively connected between the 180° hybrid coupler circuits and the 90° hybrid coupler circuits, and a plurality of radiator to RF transitions (56) coupled to the 180° hybrid coupler circuits;

a plurality of grounding vias (55) interconnecting the lower and upper ground planes of the balun layer, plurality of grounding vias (34) interconnecting the lower ground plane of the balun layer rod the ground plane of the bottom dielectric layer, and a plurality of grounding vias (57) surrounding each of the radiator to RF transitions and

a stacked disk radiator (80) adjacent to the balun layer comprising a dielectric puck (62) having an active radiator (64) formed on an upper surface, an upper dielectric layer (60) adjacent to the active radiator, a parasitic radiator (66) adjacent to the upper dielectric layer, and a pair of excitation probes (63) coupled between the radiator to RF transitions and the active radiator.

2. The tile of claim 1 characterized by a radome covering the parasitic radiator (66) and the upper dielectric layer (60).

3. The tile of claim 1 or 2, characterized by first and second coaxial connectors (23) coupled to the ground plane (22) and having center pins (23a) coupled to the first and second transitions (24a, 24b).

4. The tile of claim 1 or 2, characterized by connectorless coax-like structures coupled to the ground plane (22) and to the first and second transitions (24a, 24b).

5. The tile of any of claims 1 to 4, characterized in that the 180° hybrid coupler circuits (53) comprise modified ratrace couplers (53a).

6. The tile of any of claims 1 to 5, characterized by a plurality of grounding vias (34) coupled between the lower ground plane (52) of the balun layer (50) and the ground plane (22) disposed on the exposed surface of the bottom dielectric layer (20), a plurality of

grounding vias (55) coupled between the lower and upper ground planes (52, 54) of the balun layer, and a plurality of grounding vias disposed around the RF vias.

7. The tile of any of claims 1 to 6, characterized in that the upper dielectric layer (60) surrounds the dielectric puck (62), and the dielectric puck is disposed in a recess (68) formed in the upper dielectric layer.

8. The tile of any of claims 1 to 7, characterized by a flat foam spacer disposed between dielectric puck (62) and the radome (70).

9. The tile of claim 7 characterized in that the upper dielectric layer (60) surrounding the dielectric puck (62) comprises a dielectric material having a dielectric constant that is equal to that of the dielectric puck.

10. The tile of any of claims 1 to 9 characterized in that the dielectric puck (62) is fully surrounded by air dielectric.

11. The tile of any of claims 1 to 9, characterized in that the dielectric puck (62) is partially surrounded by air dielectric.

12. The tile of any claims 1 to 11, characterized in that the coupling circuit layer (30) and the balun layer (50) produce both senses of circular polarization.

13. The tile of any of claims 1 to 11, characterized in that the coupling circuit layer (30) and the balun layer (50) produce dual-linear polarization.

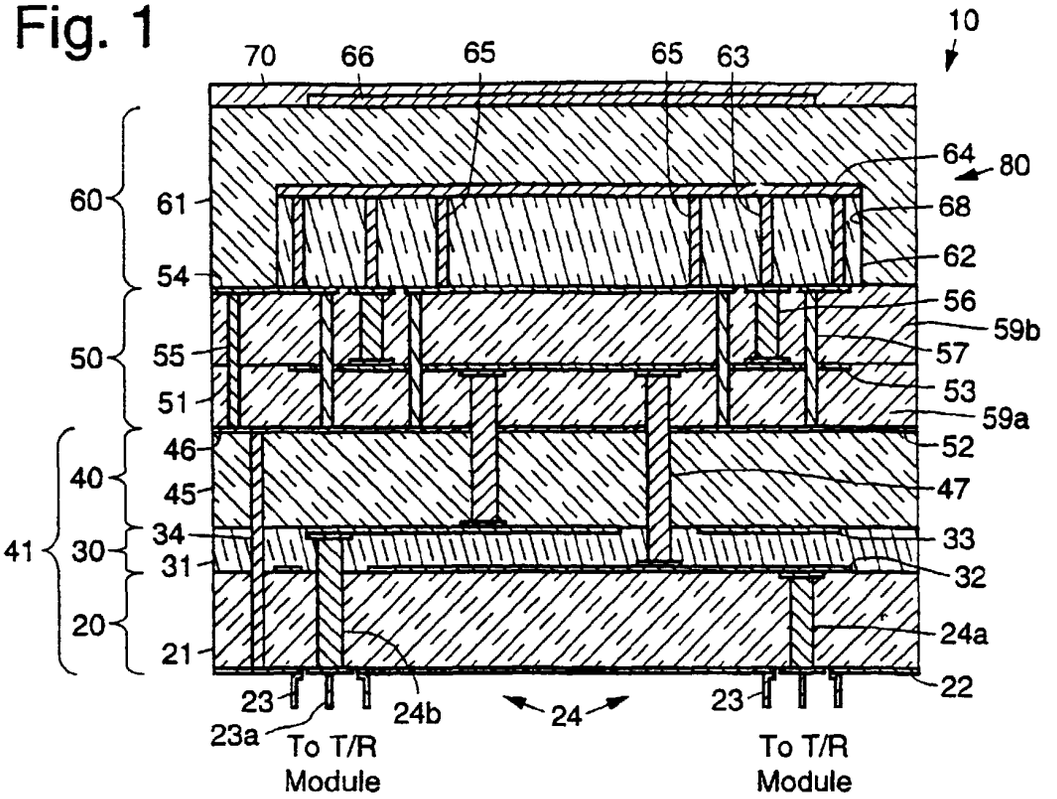
14. The tile of any of claims 1 to 11, characterized in that the coupling circuit layer (30) and the balun layer (50) selectively produce both senses of circular polarization or dual-linear polarization.

15. The tile of any of claims 1 to 14, characterized in that the upper dielectric layer (60) comprises a relatively low dielectric constant material relative to the dielectric constant of the balun layer (50).

16. The tile of any of claims 1 to 15, characterized in that the dielectric materials comprising the dielectric puck (62), the balun layer (50), and the 90° coupling circuit layer (41) have similar coefficients of thermal expansion.

17. An antenna (90) having a plurality of integrated radiator tiles (10) abutting each other that form an array, characterized in that each integrated radiator tile is an integrated radiator tile according to any of claims 1 to 16.

Fig. 1



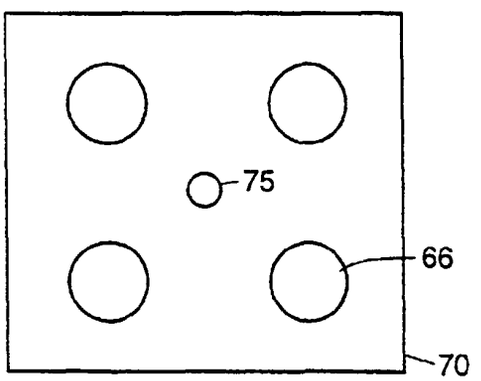


Fig. 2a

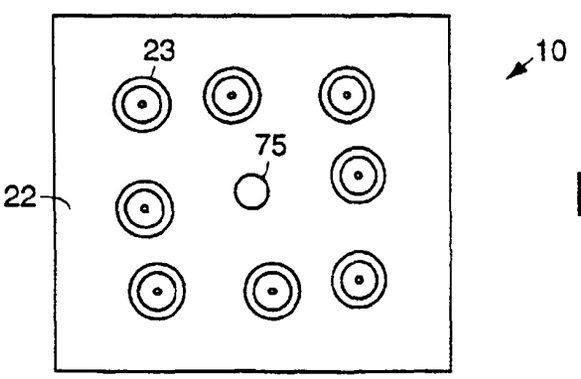


Fig. 2b

Fig. 4

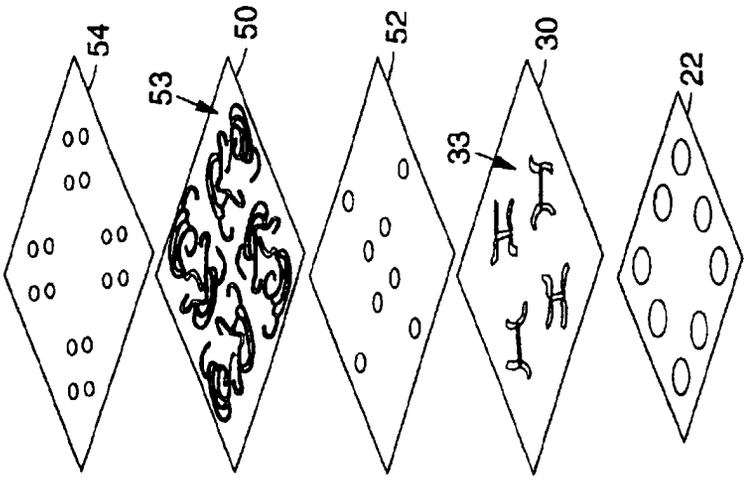
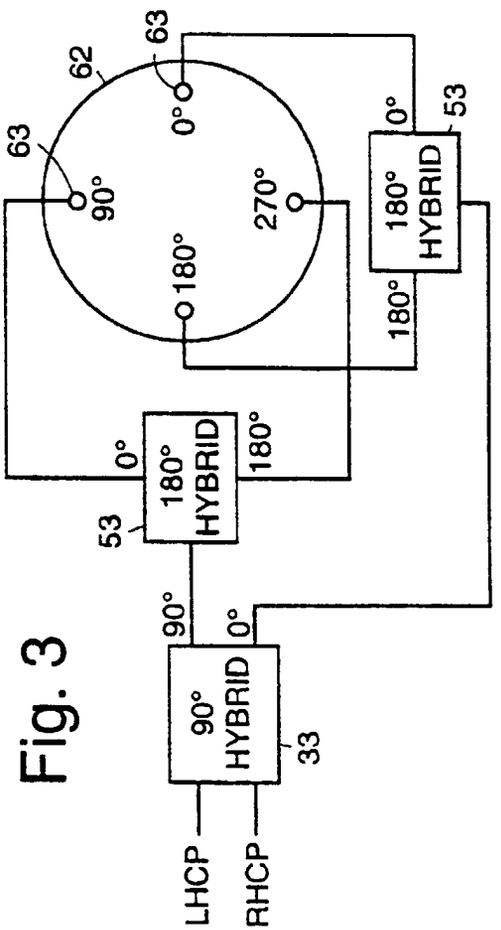

10
54
53
50
52
33
30
22

Fig. 3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0°
90°
270°
180°
180° HYBRID
0°
53
180°
180° HYBRID
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180°
53
90° HYBRID
90°
0°
33
LHCP
RHCP

Fig. 5

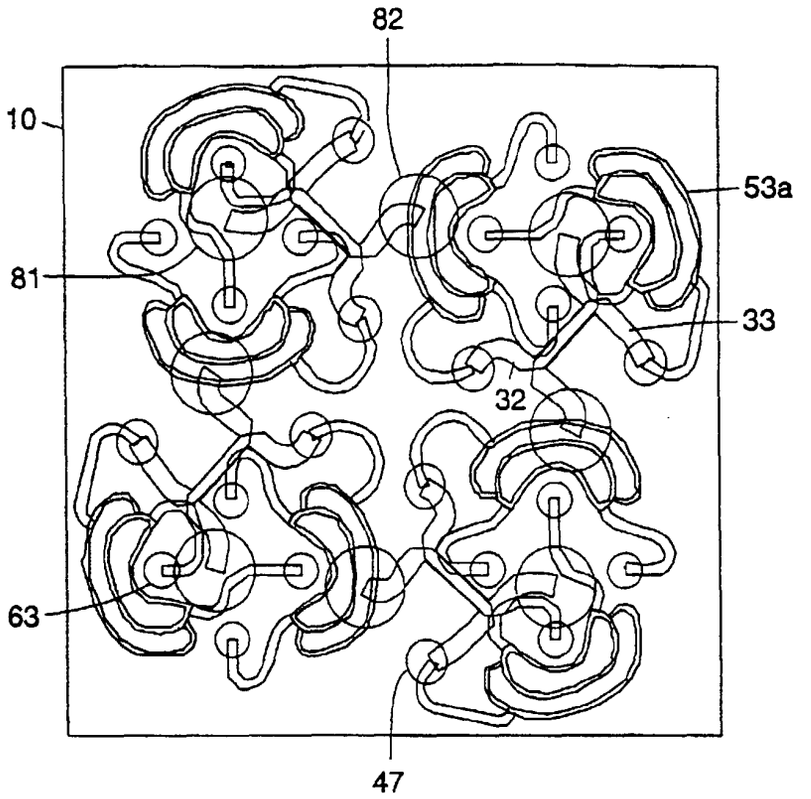

82
10
53a
81
33
32
63
47

Fig. 6

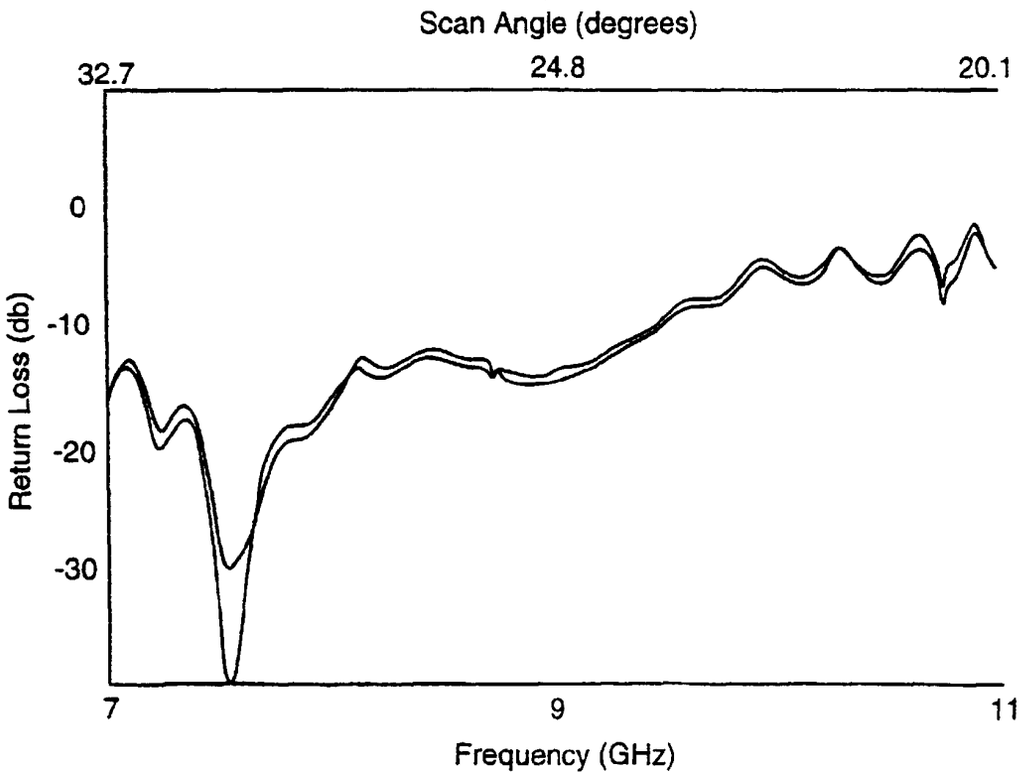
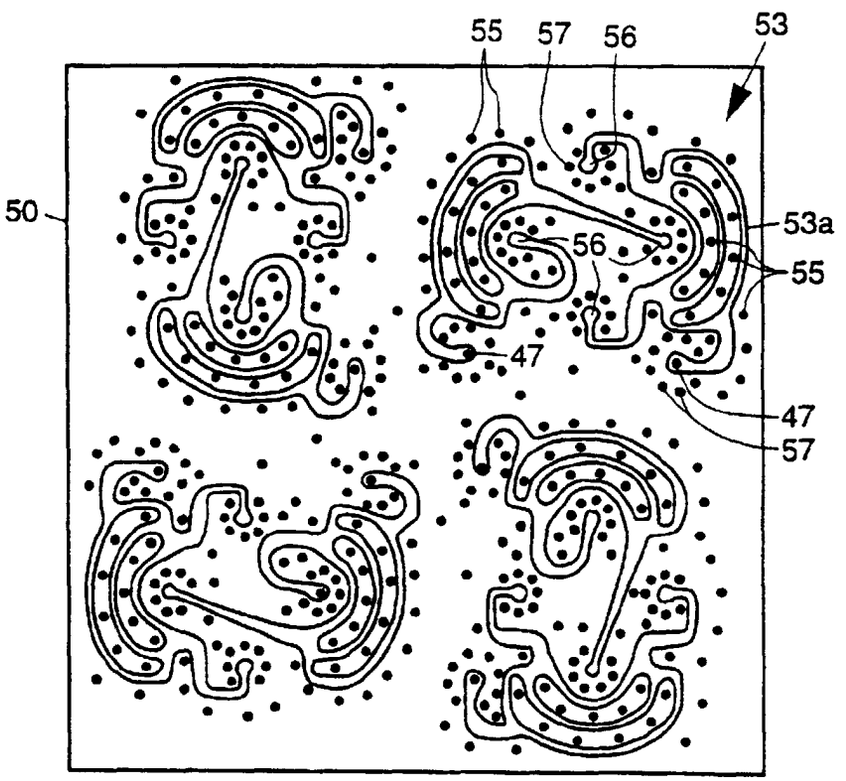

Scan Angle (degrees)
32.7
24.8
20.1
0
-10
-20
-30
Return Loss (db)
7
9
11
Frequency (GHz)

Fig. 5a



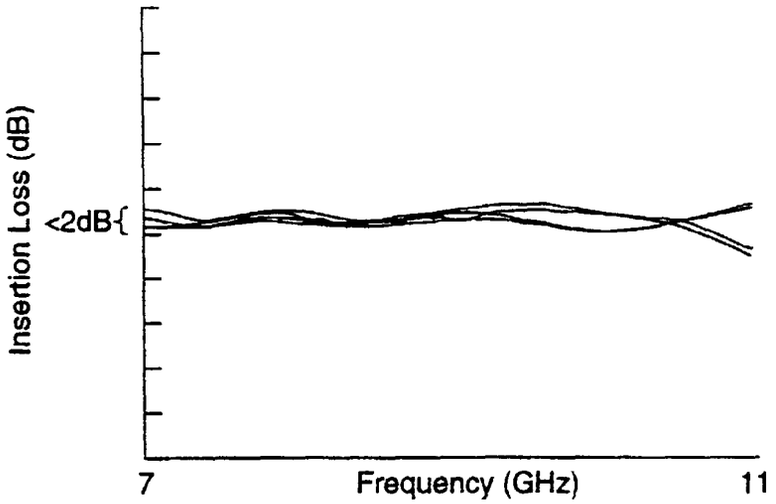


Fig. 7

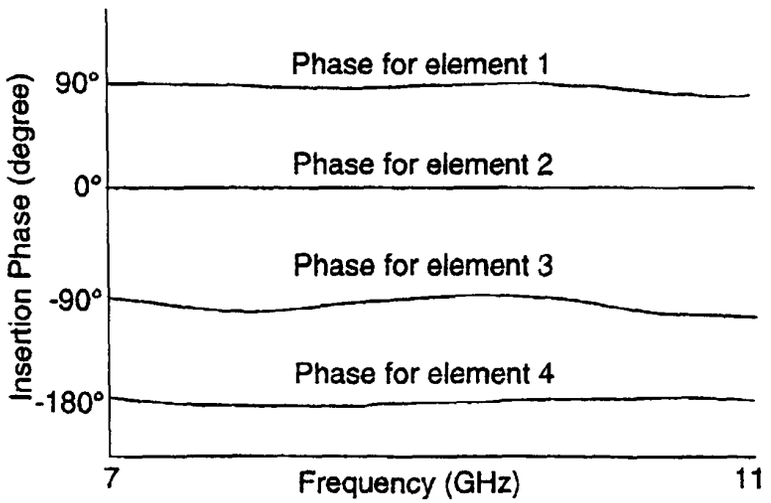


Fig. 8

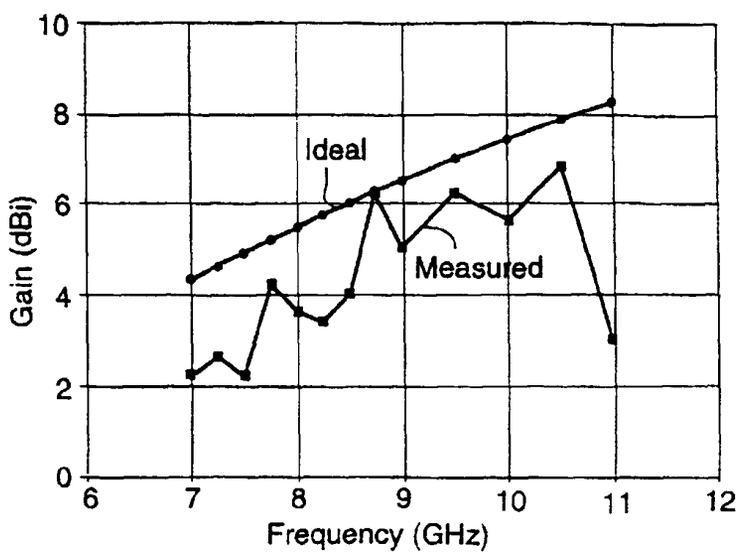


Fig. 9

Fig. 10a

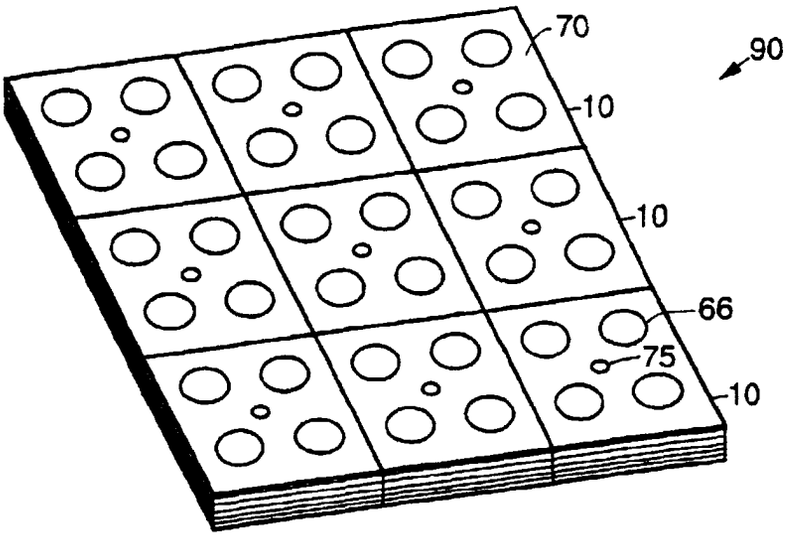
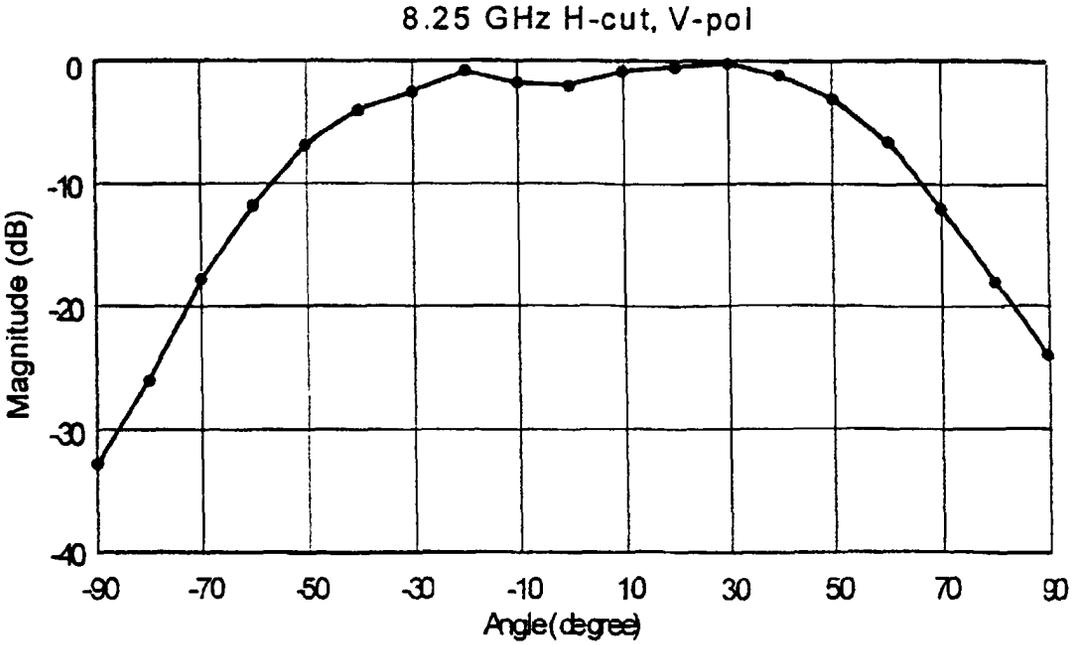


Fig. 10b



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EUROPEAN SEARCH REPORT

Application Number
EP 99 11 4034

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	21 October 1999	Villafuerte Abrego

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