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(54) Programmable digital signal processor for demodulating digital television signals

(57) A phase-lock loop circuit in a demodulator includes a timing recovery block and a carrier recovery block. The demodulator for demodulates a digital signal including symbols. The phase-lock loop includes an in-

tegrator processing a block of N samples to produce an average of the N symbols, and means for supplying the average of the N symbols to the timing recovery block and the carrier recovery block every NT period, where T is a sample time interval.

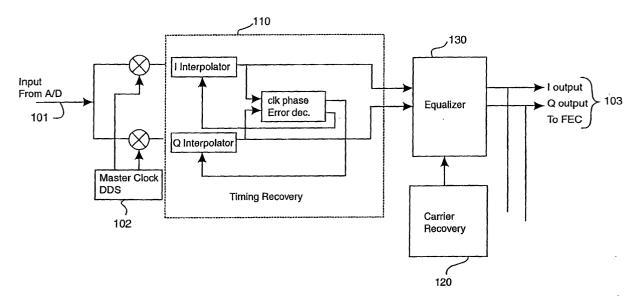


FIG. 1



EUROPEAN SEARCH REPORT

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EP 00 11 4882

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