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(54) **Dynamic type memory**

(57) A DRAM includes memory blocks (10) in a form of division of shared sense amplifier configuration in which sub arrays (11) and sense amplifiers (12) serving as cache memories are alternately arranged in the X direction of a memory chip. The memory blocks are arranged in the Y direction. Data lines are formed in parallel with the Y direction for the corresponding sub arrays, for transferring data held in the sense amplifiers corresponding to the sub arrays. I/O pads (16) are arranged in parallel with the X direction, for inputting/outputting data to/from the corresponding sub arrays via the data lines. When the shared sense amplifier configuration and sense amplifier cache system are achieved in a small area of the DRAM, the hit rate of the cache memories is increased, and data can be transferred at high speed by shortening data paths formed in the memory chip.

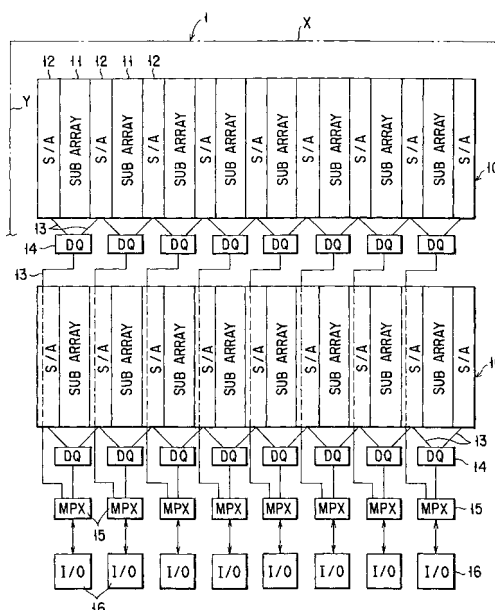


FIG. 1



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 12 4224

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The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		28 February 2008	Nielsen, Ole
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
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