(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 083 659 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
14.03.2001 Bulletin 2001/11

(51) Int. Cl.[7]: **H03K 19/003**, H03K 19/00, H03K 19/0185

(21) Application number: **00307665.0**

(22) Date of filing: **05.09.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **09.09.1999 GB 9921367**

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(54) Level shifter

(57) A level shifter uses a current mirror as a current switch connected to the drains of two oppositely-driven FETs. A switch selectively connects the current mirror to its power supply so that no quiescent DC current flows.

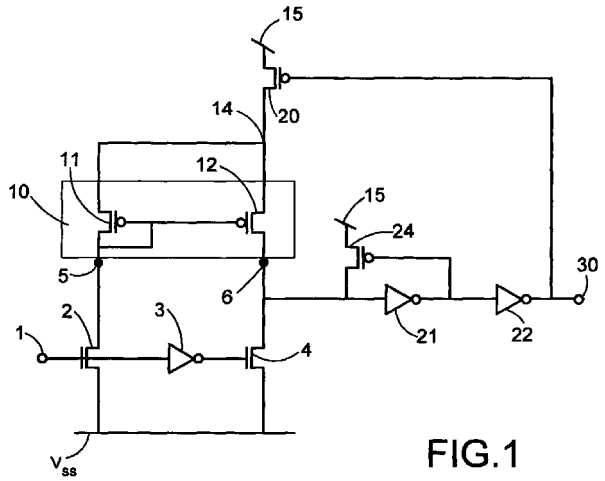


FIG.1

EP 1 083 659 A1

Description

[0001] The present invention relates to a level shifter and more particularly to a CMOS level shifter.

[0002] Level shifters are well known in logic circuitry. Some prior art level shifters require current to flow between the positive and negative supply rails in one or both of the logic states. This can be avoided by use of CMOS technology but there then may be a problem in that the relative current sourcing/sinking ability of the NMOS and PMOS transistors may have to be balanced. This is problematical because of process tolerances.

[0003] It is accordingly an object of the present invention to at least partially mitigate the above-mentioned difficulties.

[0004] According to the present invention there is provided a level shifter comprising a current mirror having a circuit node for receiving a current controlled by a control current applied at a control node thereof, said current mirror being selectively connected to a supply terminal via a supply switch, the level shifter further comprising a first switch connected to said control node for selectively applying said control current in response to an input logic signal at an input node, a second switch for selectively pulling down said circuit node in response to said input logic signal and connecting circuitry connecting said circuit node to a control terminal of said supply switch.

[0005] Preferably supply switch is implemented in PMOS technology and said first and second switches are NMOS transistors.

[0006] Advantageously said current mirror comprises first and second p transistors having common drain/source terminals, the first transistor having a source/drain terminal in common with its gate terminal as said control node, and the second transistor having a gate terminal in common with the gate terminal of the first transistor and a source/drain terminal as said circuit node.

[0007] Preferably said connecting circuitry includes pull-up circuitry connected to said circuit node for maintaining said circuit node potential when said supply switch disconnects said current mirror from said supply node.

[0008] Preferably said pull-up circuitry comprises a p FET.

[0009] In one embodiment said connecting circuitry further comprises a direct connection between said circuit node and a control node of said supply switch.

[0010] Alternatively said connecting circuitry comprises a first inverter connected between said circuit node and a gate of said pull-up FET and a second inverter connected between said gate of said pull-up FET and the control terminal of said supply switch.

[0011] Preferably said level shifter further comprises an input inverter connected between a control node of said first switch and a control node of said second switch.

[0012] An embodiment of the invention will now be described with reference to the accompanying drawings in which:-

Figure 1 shows a first embodiment of a level shifter in accordance with the present invention;

Figure 2 shows a simplified level shifter in accordance with the present invention:

Figure 3 shows a partial schematic view of an alternative level shifter realizing a first logic function; and

Figure 4 shows a partial schematic view of a second alternative level shifter realizing a second logic function.

[0013] In the various figures like reference numerals refer to like parts.

[0014] Referring first to Figure 1 a level shifter has an input terminal 1 connected to a first PMOS FET 2 and, via an inverter 3 to a second PMOS FET 4. The first and second FETs 2 and 4 have their sources connected to a negative supply VSS. The drain of the first FET 2 is connected to the control node 5 of a current mirror 10. The second FET 4 has its drain connected to a circuit node 6 of the current mirror 10. The current mirror 10 consists of two p FETS 11, 12, of which the first p FET 11 has a commoned gate and source/drain electrode connected as the control node 5. The second p FET 12 has a gate electrode connected to the gate electrode of the first p FET 11 and a drain/source terminal 6 as the circuit node. The two p FETs have a common source/drain terminal 14 which is selectively connected to a supply terminal 15, in use receiving the positive supply VDD, via a supply switch 20. The supply switch is PMOS FET and, in this embodiment, the control electrode of the supply switch 20 is connected to the circuit node 6 via the series arrangement of two inverters 21, 22. The circuit node 6 is further connected to the positive supply terminal 15 via a pull-up transistor 24 whose control electrode is connected to the output of the first inverter 21. The pull-up transistor 24 is weak by comparison with the second switch 4.

[0015] In the present embodiment, the circuit output is derived from the output of the second inverter 22; it will of course be understood that it could be derived from a further inverter connected to the circuit node 6, if appropriate. The use of such an inverter to provide the output allows for separate optimization of the data propagation delays and the control for enabling the supply.

[0016] To consider the operation of the circuit it is necessary to consider the two transistors 20 and 24. If the circuit node 6 is at a high potential then the inverter 21 produces an output of low potential which is applied to the gate of the pull-up switch 24 to cause the circuit

node 6 to remain at high potential.

[0017] The second inverter 22 produces a low potential at its output, thus effectively turning off the supply transistor 20.

[0018] If at this time a logic 1 is applied to the input terminal 1, the first switch 2 will be rendered conductive but the open circuit afforded by the supply switch 20 prevents any current from flowing from node 5. The result is that no change in the circuit occurs and no current flows between the supply terminal 15 and the reference node VSS.

[0019] If a logic 0 is applied to input terminal 1, then the first switch 2 will be turned off and the inverter 3 will produce a high output to the second switch 4. The second switch 4, because it is an NMOS FET will conduct and will pull-down the circuit node 6 to a low potential. The current mirror 10 is turned off - i.e.: the off-state of the first switch 2 does not apply current to the controlling p FET 11, and so no current flows through the controlled p FET 12. Pulling down the circuit node 6 causes the output of the first inverter 21 to go high, thus turning off the pull-up switch 24 and, via the second inverter 22, turning on the supply switch 20. Although the supply switch is turned on, there is no DC path because the current mirror 10 is off.

[0020] However, if at this time the input terminal is again supplied with a logic 1, then the first switch 2 will turn on thus sinking current from the control node 5 of the current mirror which in turn causes current to flow from the supply switch 20 through the second PMOS FET 12 of the current mirror causing the circuit node 6 to be pulled high. Because in this situation the second switch 4 is off, there is again no DC path present.

[0021] It will be seen therefore that the level shifter as described is to a certain extent bistable.

[0022] A simplified arrangement is shown in Figure 2 in which the control gate of the supply switch 20 is connected directly to the circuit node 6.

[0023] A constraint on both of the embodiments described is that the current sourcing ability of the pull-up transistor is less than the pull-down ability of the second switch 4. There is no requirement to balance the drain/source currents of NMOS and PMOS FETs. As has been discussed above, there is no static current flow in either logic state.

[0024] It will be clear to those skilled in the art that the inverters 21 and 22 shown in Figure 1 have a propagation delay. The particular circuit shown therefore operates successfully provided the time between input transitions to the input terminal 1 is greater than this propagation delay. If this is not the case, then other alternative circuits may be necessary to rapidly disconnect the remainder of the circuit from the positive supply when required.

[0025] The particular configuration of current mirror is that of a simple current mirror. Other switching circuits for current comparators could be substituted, and specifically different current mirror circuits could be used.

[0026] Finally, the circuits disclosed has only a single input terminal. It would be clear to those skilled in the art that, instead of the single NMOS FETS 2 and 4, alternative circuits could be used to selectively connect the nodes 5 and 6 to the reference node VSS.

[0027] Two examples of such alternative connections are shown in Figures 3 and 4.

[0028] In Figure 3 it will be seen that the first FET 2 has been replaced by two parallel FETs 200, 201 and the second FET 4 by two parallel FETs 400, 401. Each of the first pair 200, 201 has its source connected to the reference node VSS and its drain connected to the control node 5 of the current mirror. Similarly, the second pair, 400, 401 each has a source connected to the reference node VSS and a drain connected to the circuit node 6 of the current mirror. The control gate of the first transistor 201 of the first pair is connected to the control gate of the first transistor 400 of the second pair via an inverter 300 and likewise the gate of the second transistor 201 of the first pair is connected to that of the second transistor of the second pair via an inverter 301. The control gate of the first transistor 200 is connected to a first input terminal 100 and that of the second transistor 201 to a second input terminal 101.

[0029] It will be clear to those skilled in the art that the circuit of Figure 3 provides an OR gating function.

[0030] A second alternative arrangement is shown in Figure 4.

[0031] In this case each of the first and second FETs 2 and 4 of Figure 1 are replaced by the series connection of a first pair 203, 204 and a second pair 403, 404 of NMOS FETs with gates interconnected by inverters 303, 304. Respective input terminals 103, 104 are connected to the control gates of the first pair 203, 204. It will be clear to those skilled in the art that this connection provides an AND gating function.

[0032] It will be clear to those skilled in the art that other logic gating functions can be achieved by suitable modification of the input transistors.

Claims

1. A level shifter comprising a current mirror (10) having a circuit node (6) for receiving a current controlled by a control current applied at a control node (5) of said current mirror, said current mirror being selectively connected to a supply terminal (15) via a supply switch (20), the level shifter further comprising a first switch (2) connected to said control node for selectively applying said control current in response to an input logic signal at an input node, a second switch (4) for selectively pulling down said circuit node in response to said input logic signal arid connecting circuitry (21,22,24) connecting said circuit node (6) to a control terminal of said supply switch.

2. A level shifter as claimed in claim 1 wherein said

supply switch (20) is implemented in PMOS technology and said first and second switches (2,4) are NMOS transistors.

3. A level shifter as claimed in claim 1 or 2 wherein said current mirror (10) comprises first (11) and second (12) transistors having common drain/source terminals, the first transistor (11) having a source/drain terminal in common with its gate terminal as said control node (5), and the second transistor (12) having a gate terminal in common with the gate terminal of the first transistor and a source/drain terminal as said circuit node.

4. A level shifter as claimed in claim 3 wherein said first (2) and second (4) transistors are p FETs.

5. A level shifter as claimed in any preceding claim wherein said connecting circuitry includes pull-up circuitry (21,24) connected to said circuit node for maintaining said circuit node potential when said supply switch disconnects said current mirror from said supply node.

6. A level shifter as claimed in claim 5 wherein said pull-up circuitry comprises a p FET (24).

7. A level shifter as claimed in any preceding claim wherein said connecting circuitry further comprises a direct connection between said circuit node (6) and a control node of said supply switch (20).

8. A level shifter as claimed in claim 6 wherein said connecting circuitry (21) comprises a first inverter connected between said circuit node (6) and a gate of said pull-up FET and a second inverter (22) connected between said gate of said pull-up FET and a control terminal of said supply switch.

9. A level shifter as claimed in any preceding claim and further comprising an input inverter connected between a control node of said first switch and a control node of said second switch.

10. A level shifter as claimed in any preceding claim further comprising a further first switch and a further second switch connected to said first switch and said second switch respectively to realize therewith a logic function.

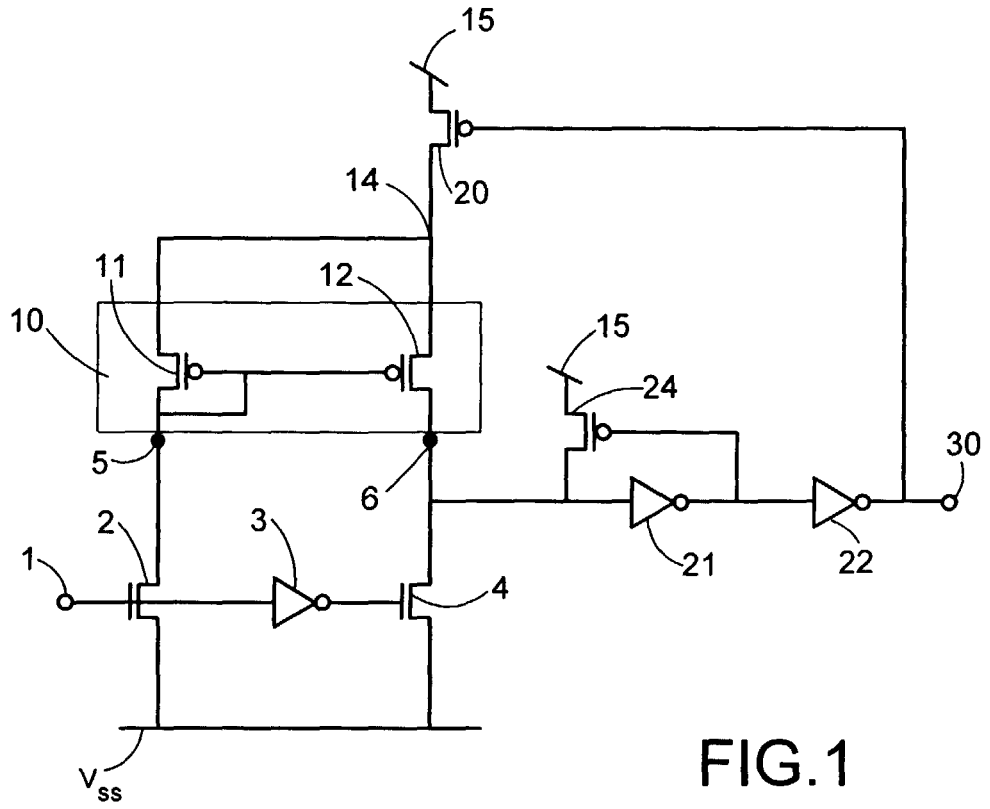


FIG.1

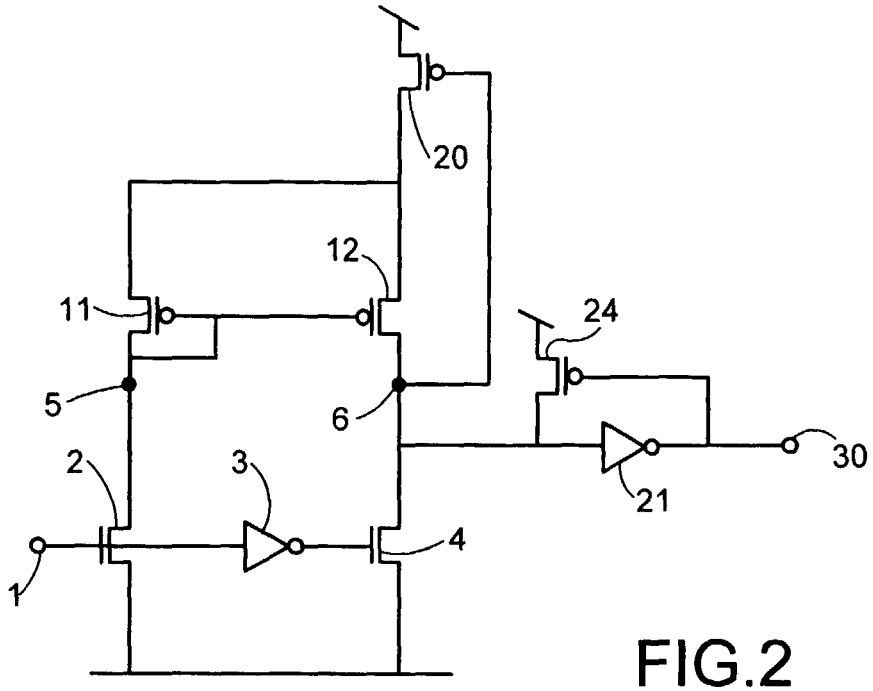
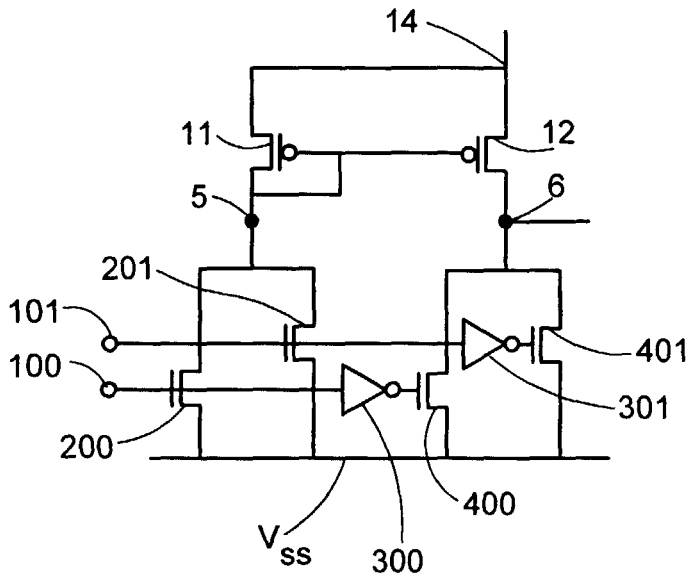


FIG.2


14
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12
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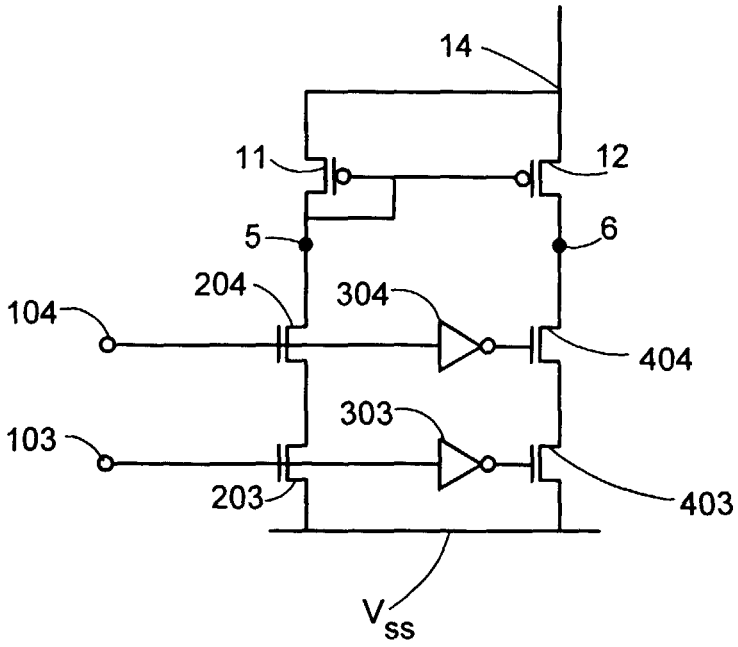
201
101
100
200
401
301
400
V_{ss}
300

FIG.3


14
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204
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104
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303
103
203
403
V_{ss}

FIG.4

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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 7665

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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A	US 5 268 872 A (FUJII SHINJI ET AL) 7 December 1993 (1993-12-07) * figure 14 *	1-10	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 December 2000	Jepsen, J

CATEGORY OF CITED DOCUMENTS

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