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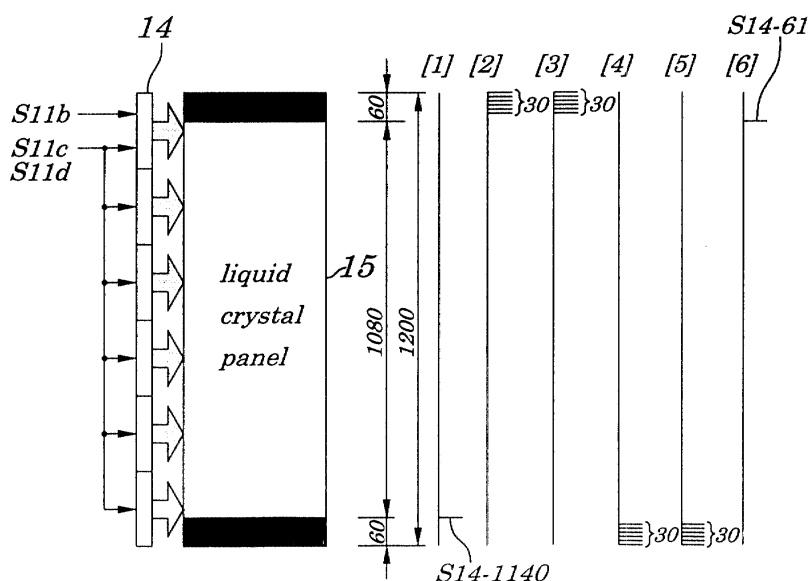
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(54) Liquid crystal display and driving method for liquid crystal display

(57) For an image display area, a scanning signal circuit (14) sequentially outputs scanning signals (S14-61 to S14-1140) once for one horizontal period of an image input signal (lin), and pixel data signals (S13-1 to S13-m) are input from a display signal circuit (13) to a liquid crystal panel (15). For a blanking area, a plurality of input pulses (S11b) are input to the scanning signal circuit (14) synchronously with a high speed clock signal (S11c), and the input pulses (S11b) transfer to the blanking area. After writing blanking lines to thirty odd lines

at an upper side of the liquid crystal panel (15) at a same time, blanking lines are written into thirty even lines at the upper side at a same time. Similarly, after writing blanking lines to thirty odd lines at a lower side of the liquid crystal panel (15) at a same time, blanking lines are written into thirty even lines at the lower side at a same time. With this operation, when a number of scanning signal lines (X1 to Xn) of the liquid crystal panel (15) is larger than a number of scanning lines of one vertical period of the image input signal (lin), the blanking area is made completely.

FIG.2B



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Description

Field of the Invention

[0001] The present invention relates to a display using a liquid crystal panel and more particularly to the liquid crystal display and a driving method for the liquid crystal display carrying out a complete blanking display in a blanking area (blanking period) in which no image is displayed at an upper side and a lower side of a screen.

[0002] The present application claims priority of Japanese Patent Application No. Hei 11-335170 filed on November 25, 1999, which is hereby incorporated by reference.

Description of the Related Art

[0003] A conventional liquid crystal display, as shown in Fig. 5, is provided with a controller 1 and an oscillating circuit 2. The controller 1 receives an image input signal *lin* supplied from outside and a clock signal *S2* supplied from an oscillating circuit 2. The controller 1 generates an image data signal *S1a* and a input pulse *S1b*, a clock signal *S1c* and an output enable signal *S1d* for generating a scanning signal and outputs them. The controller 1 is connected to a display signal circuit 3 and a scanning signal circuit 4. The display signal circuit 3 receives the image data signal *S1a*, generates pixel (picture element) data signal *S3-1* to pixel data signal *S3-m* and outputs pixel data signal *S3-1* to the pixel data signal *S3-m* to a liquid crystal panel 5. The scanning signal circuit 4 is provided with a shift register (not shown) for receiving the input pulse *S1b* and for shifting synchronously with the clock signal *S1c* and outputs the input pulse *S1b* as scanning signal *S4-1* to scanning signal *S4-m* to the liquid crystal panel 5 when receiving the output enable signal *S1d*. An output side of the display signal circuit 3 is connected to data signal line *Y1* to data signal line *Ym* of the liquid crystal panel 5. An output side of the scanning signal circuit 4 is connected to scanning signal line *X1* to scanning signal line *Xn* of the liquid crystal panel 5. The liquid crystal panel 5 is provided with a plurality of pixel areas at intersection points of the data signal line *Y1* to data signal line *Ym* and scanning signal line *X1* to scanning signal line *Xn* and displays an image by supplying pixel data signal *S3-1* to the pixel data signal *S3-m* to pixel areas selected by scanning signal *S4-1* to scanning signal *S4-n* among all the pixel areas.

[0004] The operation of the conventional liquid crystal display will be explained with reference to the timing chart shown in Fig. 6.

[0005] The image input signal *lin* and the clock signal *S2* are input into the controller 1. Then, the image data signal *S1a*, the input pulse *S1b*, the clock signal *S1c* and the enable signal *S1d* are output from the controller 1. The image data signal *S1a* is input into the display signal circuit 3 and then pixel data signal *S3-1* to pixel

data signal *S3-m* are output from the display signal circuit 3. The input pulse *S1b*, the clock signal *S1c* and the output enable signal *S1d* are input into the scanning signal circuit 4. In the scanning signal circuit 4, the input pulse *S1b* shifts synchronously with the clock signal *S1c*, and scanning signal *S4-1* to scanning signal *S4-n* are output when the output enable signal *S1d* is in a active mode, namely, a high level (hereinafter referred to as H level). No scanning signal *S4-1* to no scanning signal *S4-n* are output when the output enable signal *S1d* is in a non-active mode, namely, a low level (hereinafter referred to as L level). The pixel data signal *S3-1* to pixel data signal *S3-m* and the scanning signal *S4-1* to scanning signal *S4-n* are input into the liquid crystal panel 5. In the liquid crystal panel 5, pixel data signal *S3-1* to pixel data signal *S3-m* are supplied to pixel areas selected by scanning signal *S4-1* to scanning signal *S4-n* and then an image corresponding to pixel data signal *S3-1* to pixel data signal *S3-m* which are selected is displayed.

[0006] However, there are the following problems in the conventional liquid crystal display.

[0007] Figure 7 is a view explaining an operation of the conventional liquid crystal display when a number of scanning signal *X1* to scanning signal *Xn* is 1200, a number of scanning lines for an image display area (image display period) of the image input signal *lin* is 1080 and a total of scanning lines is 1125.

[0008] As shown in Fig. 7, a state [1] shows scanning signal *S4-1* when pixel data signal *S3-1* to pixel data signal *S3-m* of a first line for the image display area (image display period) is firstly written in the liquid crystal panel 5. The output enable signal *S1d* is always in active mode. Then, the input pulse *S1b* is shifted synchronously with the clock signal *S1c*, and pixel data signal *S3-1* to pixel data signal *S3-m* of a second line are written in the liquid crystal panel 5. In this way, pixel data signal *S3-1* to pixel data signal *S3-m* of the first line through a 1080th line are written in the liquid crystal panel 5. A state [2] shows a scanning signal *S4-1080* when pixel data signal *S3-1* to pixel data signal *S3-m* of the 1080th line are written in the liquid crystal panel 5.

[0009] Then, a blanking area (black belt) is written when the clock signal *S1c* is received. The blanking area (blanking period) includes forty-five lines and the liquid crystal panel 5 becomes black in the blanking area. A state [3] shows the scanning signal *S4-1* of the first line and a scanning signal *S4-1126* of an 1126th line when a next line is the 1126th line, namely, the next is returned to the first line. Therefore, concerning the 1126th line and following lines, pixel data signal *S3-1* to pixel data signal *S3-m* are written similarly to a fifth line to an 1125th line. A state [4] shows an example of the liquid crystal panel 5 displaying a state in that a start of the blanking area is taken as a start of an image display area. In the state [4], black parts show a blanking area 5a and blanking area 5c and a white part is an image display area 5b. As shown in the state [4], the blanking area 5a and the

blanking area 5c are written at an upper side and a lower side of the image display area 5b, and another image display area 5d is displayed under the blanking area 5c at the lower side. Therefore, there is a problem in that it is impossible to write complete blanking areas at the upper side and at the lower side of the image display area.

[0010] To solve this problem, a technique is used in which a digital signal process is applied to the image input signal lin when a number of scanning signal line X1 to scanning signal line Xn is larger than a total of the scanning lines in a vertical period. For example, when the number of the scanning signal line X1 to scanning signal line Xn of the liquid crystal panel 5 is 1200, the number of scanning lines of the image input signal lin in the image display area is 1080 and the total of the scanning lines is 1125, the image input signal lin is stored in a frame memory and a process for preparing blanking areas. With this operation, the liquid crystal panel is carried out in which the total of scanning lines is 1200 while the number of scanning lines in the image display area is kept to 1080. However, when the total of scanning lines is increased by executing a such a digital process, there is a problem in that parts such as a frame memory and a frame memory controller increase and a configuration becomes complicated and large.

[0011] Further, Japanese Patent Publication No. 2820061 discloses a liquid crystal panel using a polysilicon technique in which a complicated scanning signal circuit is configured in a liquid crystal panel, a plurality of scanning signals are made in active modes and thereby complete blanking areas are written in the upper side and the lower side of the image display area. However, in a liquid crystal panel using an amorphous silicon technique, which is mainly used in recent years, an electron mobility is remarkably delayed compared with the liquid crystal panel using the polysilicon technique, and therefore, there is no practical use though the complicated scanning signal circuit is configured in the liquid crystal panel. That is, since the scanning signal circuit is a shift register of a simple configuration, it is impossible to make the plurality of scanning signals in the active mode at a same time by the conventional driving method shown in Fig. 6.

SUMMARY OF THE INVENTION

[0012] In view of the above, it is an object of the present invention to provide a liquid crystal display capable of writing complete blanking at an upper side and a lower side of an image display area in a liquid crystal panel using an amorphous technique while keeping conventional configuration of a scanning signal circuit, when number of scanning signal lines is larger than total of scanning lines of image signal for one vertical period.

[0013] According to a first aspect of the present invention, there is provided a liquid crystal display including:

a liquid crystal panel provided with a plurality of data

signal lines for inputting image data signals, a plurality of scanning signal lines for inputting scanning signals and a plurality of pixel areas arranged at intersection points of the data signal lines and the scanning signal lines and for displaying an image corresponding to the image data signals by supplying the image data signals to selected pixel areas selected by scanning signals among the pixel areas;

a display signal circuit for sending the image data signals to the data signal lines in accordance with image input signals;

a scanning signal circuit for inputting an input pulse used to generate the scanning signals, for moving synchronously with a clock signal and for sending the input pulse to the scanning signal lines as the scanning signals when an output instruction signal is input; and

a controller for inputting the image input signals and for outputting the input pulse, the clock signal and the output instruction signal to the scanning signal circuit; the controller, when a number of the scanning signal lines is larger than a number of scanning lines of the image input signals for a vertical period, for outputting the input pulse, the clock signal and the output instruction signal in a first operation mode for an image display area in a vertical direction of a screen of the liquid crystal panel and for outputting the input pulse, the clock signal and the output instruction signal in a second operation mode for a blanking area in which no image is displayed at an upper side and a lower side of the screen in the vertical direction.

[0014] In the foregoing, a preferable mode is one wherein in the first operation mode, the scanning signal circuit outputs the scanning signal once for one horizontal period of the image input signal and in the second operation mode, the scanning signal circuit outputs the plurality of the scanning signals for the blanking area at the same time.

[0015] Also, a preferable mode is one wherein in the first operation mode, the scanning signal circuit outputs the scanning signals plural times for one horizontal period of the image input signal in order to enlarge the image and in the second operation mode, the scanning signal circuit outputs the plurality of the scanning signals for the blanking area at the same time.

[0016] Also, a preferable mode is one wherein in the second operation mode, the scanning signal circuit outputs the plurality of the scanning signals into an odd line and an even line separated from the scanning signal lines.

[0017] Also, a preferable mode one wherein in the second operation mode, the scanning signal circuit inverts polarities of the scanning signals for the odd line and the even line.

[0018] Furthermore, a preferable mode one wherein

the liquid crystal panel is an active matrix liquid crystal panel using a thin film transistor of amorphous silicon as an active element.

[0019] According to a second aspect of the present invention, there is provided a driving method for a liquid crystal display including:

a step, when a number of scanning signal lines of a liquid crystal panel is larger than a number of scanning lines of image input signals for a vertical period, of outputting a scanning signal for one horizontal period of image input signal for an image display area in a vertical direction of a screen of the liquid crystal panel and of outputting a plurality of scanning signals at a same time for a blanking area in which no image is displayed at an upper side and a lower side of the screen in the vertical direction.

[0020] According to a third aspect of the present invention, there is provided a driving method for a liquid crystal display including:

a step, when a number of scanning signal lines of a liquid crystal panel is larger than a number of scanning lines of image input signals for a vertical period, of outputting scanning signals plural times for one horizontal period of image input signal in order to enlarge an image for an image display area in a vertical direction of a screen of the liquid crystal panel and of outputting a plurality of scanning signals at a same time for a blanking area in which no image is displayed at an upper side and a lower side of the screen in the vertical direction.

[0021] In the foregoing, a preferable mode wherein the plurality of the scanning signals are output separately into odd lines and even lines for a blanking area in which no image is displayed at the upper side and the lower side of the screen in the vertical direction.

[0022] Also, a preferable mode one wherein polarities of the scanning signals are inverted for the odd lines and the even lines.

[0023] With the above-mentioned configurations, when the number of scanning signal lines of the liquid crystal panel equals the number of scanning lines of one vertical period of the image input signal, the controller outputs the input pulse, the clock signal and the output instruction signal in the first operation mode for the image display area of the screen of the liquid crystal panel in the vertical direction and outputs the input pulse, the clock signal and the output instruction signal in the second operation mode for the blanking area of the screen displaying no image at the upper side and the lower side of the screen in the vertical direction, therefore, it is possible to write complete blanking at the upper side and lower side of the image display area without a digital signal process using a frame memory or a like in spite of a relatively simple liquid crystal panel using the amorphous silicon technique. Further, when the controller receives an image input signal of which a number of pixels is half or less than a number of scanning pixels of the liquid crystal panel, the controller outputs the clock signal plural times and the scanning signal circuit outputs

scanning signals synchronously with the clock signals plural times, therefore, it is possible to enlarge the image.

5 BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The above and other objects, advantages, and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing an electrical configuration of a liquid crystal display according to a first embodiment;

Fig. 2A is a timing chart and Fig. 2B is a view for explaining an operation of the liquid crystal display in Fig. 1;

Fig. 3 is a block diagram showing an electrical configuration of a liquid crystal display according to a second embodiment;

Fig. 4 is a timing chart for explaining an operation of the liquid crystal display in Fig. 3;

Fig. 5 is a block diagram showing an electrical configuration of a conventional liquid crystal display;

Fig. 6 is a timing chart for explaining an operation of the conventional liquid crystal display shown in Fig. 5; and

Fig. 7 is a view for explaining the operation of the conventional liquid crystal display shown in Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] Best modes for carrying out the present invention will be described in further detail using various embodiments with reference to the accompanying drawings.

First Embodiment

[0026] Figure 1 is a block diagram showing an electrical configuration of a liquid crystal display according to the first embodiment of the present invention.

[0027] The liquid crystal display according to the first embodiment, as shown in Fig. 1, is provided with a controller 11 and an oscillating circuit 12. The controller 11 includes a plurality of logic circuits and a like, receives an image input signal *Iin* supplied from outside and a clock signal *S12* supplied from the oscillating circuit 12 and generates an image data signal *S11a* and an input pulse *S11b*, a clock signal *S11c* and an output instruction signal, such as an output enable signal *S11d*, for scanning signal generation in order to output them. Further, the controller 11, when number of scanning signal lines of a liquid crystal panel 15 in the liquid crystal display is larger than number of the image input signal *Iin* for one vertical period, outputs the input pulse *S11b*, the clock signal *S11c* and the output enable signal *S11d* in

a first operation mode for an image display area of the liquid crystal panel 15 in a vertical direction and outputs the input pulse S11b, the clock signal S11c and the output enable signal S11d and outputs the input pulse S11b, the clock signal S11c and the output enable signal S11d in a second operation mode for a blanking area in which no image is displayed at an upper side and a lower side of the liquid crystal panel 15 in the vertical direction.

[0028] The controller 11 is connected to a display signal circuit 13 and a scanning signal circuit 14. The display signal circuit 13 receives the image data signal S11a, generates pixel data signal S13-1 to pixel data signal S13-m and outputs them. The scanning signal circuit 14 includes a shift register for receiving the input pulse S11b and shifting synchronously with the clock signal S11c and a like and outputs the input pulse S11b as scanning signal S14-1 to scanning signal S14-n when receiving the output enable signal S11d. An output side of the display signal circuit 13 is connected to data signal line Y1 to data signal line Ym of the liquid crystal panel 15 and an output side of the scanning signal circuit 14 is connected to scanning signal line X1 to scanning signal line Xn. The liquid crystal panel 15 includes a plurality of pixel areas provided at intersection points of data signal line Y1 to data signal line Ym and scanning signal line X1 to scanning signal line Xn and displays an image by supplying pixel data signal S13-1 to pixel data signal S13-m to image areas selected by scanning signal S14-1 to scanning signal S14-n among all the image areas. The liquid crystal panel 15 is an active-matrix type, and includes active elements of a TFT (Thin Film Transistor) using amorphous silicon and memory cells for storing pixel data signal S13-1 to pixel data signal S13-m as the pixel areas.

[0029] In the liquid crystal display, the image input signal lin and the clock signal S12 are input into the controller 11, and the image data signal S11a, the input pulse S11b, the clock signal S11c and the output enable signal S11d are output from the controller 11. The image data signal S11a is input into the display signal circuit 13 and pixel data signal S13-1 to pixel data signal S13-n are output from the display signal circuit 13. The input pulse S11b, the clock signal S11c and the output enable signal S11d are input into the scanning signal circuit 14. In the scanning signal circuit 14, the input pulse S11b shifts synchronously with the clock signal S11c, and scanning signal S14-1 to scanning signal S14-n are output when the output enable signal S11d is an H level. The pixel data signal S13-1 to pixel data signal S13-m and scanning signal S14-1 to scanning signal S14-n are input into the liquid crystal panel 15. In the liquid crystal panel 15, pixel data signal S13-1 to pixel data signal S13-m are supplied to the pixel areas selected by scanning signal S14-1 to scanning signal S14-n, and the display corresponding to pixel data signal S13-1 to pixel data signal S13-m is displayed.

[0030] Figure 2A is a timing chart and Fig. 2B is a view for explaining an operation of the liquid crystal display

according to the first embodiment when number of scanning signal line X1 to scanning signal line Xn is larger than total of scanning lines of the image input signal lin. Figure 2A and Fig. 2B show an operation of the liquid crystal display when number of scanning signal line X1 to scanning signal line Xn is 1200, number of the image input signal lin for the image display area is 1080 and total of scanning lines is 1125.

[0031] Explanations will be given of the liquid crystal display with reference to Fig. 2A and Fig. 2B.

[0032] As shown in Fig. 2A and Fig. 2B, in a state [1], the output enable signal S11d becomes the H level, a scanning signal S14-1140 is output from the scanning signal circuit 14 and last pixel data signal S13-1 to last pixel data signal S13-m in the image display area for 1080 lines are input from the display signal circuit 13 to the liquid crystal panel 15. A transition period from the state [1] to state [2] in Fig. 2A and Fig. 2B, the output enable signal S11d becomes an L level and the scanning signal S14-1140 in the state [1] becomes in a non-active state. At this time, thirty pulses inverting per one pulse of the clock signal S11c are input to the scanning signal circuit 14 and transfer in the scanning signal circuit 14 synchronously with the clock signal S11c.

[0033] In the state [2] shown in Fig. 2A and Fig. 2B, the controller 11 executes an operation in the second operation mode. The output enable signal S11d becomes the H level and thirty odd lines are output from among sixty lines of scanning signal S14-1 to scanning signal S14-60 in the blanking area of the upper side from the scanning signal circuit 14 at a same time. As a result, blanking lines are written in thirty odd lines of the upper side in the liquid crystal panel 15 at a same time. In a state [3] shown in Fig. 2A and Fig. 2B, the controller 11 executes an operation in the second operation mode. The output enable signal S11d becomes the H level, thirty input pulses S11b transfer in the scanning circuit 14 synchronously with one clock signal S11c and thirty even scanning signals are output from among sixty signals of scanning signal S14-1 to scanning signal S14-60 in the blanking area of the upper side from the scanning signal circuit 14 at a same time. As a result, blanking lines are written in thirty even lines of the upper side in the liquid crystal panel 15 at a same time. Polarities of these scanning signals are inverse to those of the thirty odd scanning signals in the state [2]. In the state [2] and the state [3] shown in Fig. 2A and Fig. 2B, to match an image display period for the image display area with a writing time, the clock signal of a period similar to the image display period is input to the scanning signal circuit 14. Periods in the state [2] and the state [3] may be longer or shorter than a horizontal period, if only the blanking areas are written in the liquid crystal panel 15. In a transition period from the state [3] to a state [4] in Fig. 2A and Fig. 2B, the output enable signal S11d becomes the L level and the scanning signal becomes a non-active mode. At this time, one clock signal S11c is input to the scanning signal circuit 14 and thirty input

pulses S11b transfer of synchronously with one clock signal S11c to the blanking area at the lower side.

[0034] Then, in the state [4] shown in Fig. 2A and Fig. 2B, the output enable signal S11d becomes the H level and thirty odd scanning signals are output among sixty signals of scanning signal S14-1141 to scanning signal S14-1200 of the blanking area at the lower side. As a result, blanking lines are written in thirty odd lines of the liquid crystal panel 15 at the lower side at a same time. In a state [5] shown in Fig. 2A and Fig. 2B, the output enable signal S11d becomes the H level, thirty input pulses S11b transfer in the scanning signal circuit 14 synchronously with one clock signal S11c, and thirty even scanning signals among sixty of the scanning signal S14-1141 to scanning signal S14-1200 of the blanking area at the lower side. As a result, blanking lines are written in the thirty even lines of the liquid crystal panel 15 at the lower side. In the state [4] and the state [5] in Fig. 2A and Fig. 2B, in order to match image display period with writing time, clock signals S11c with period equal to that of the image display area is input to the scanning signal circuit 14. Period of the state [4] and the state [5] may be longer or shorter than the horizontal period only if the blanking is written.

[0035] After the state [5] in Fig 2A and Fig. 2B, as shown in Fig. 2A, the input pulse S11b of the H level is input for one clock signal S11c. In a transition period from the state [5] to a state [6], one clock signal S11c is input into the scanning signal circuit 14. Then, thirty input pulses S11b become non-active modes and one input pulse S11b transfers to a start of the image display area. In the state [6] in Fig. 2A and Fig. 2B, the controller 11 executes the first operation mode, the output enable signal S11d becomes the H level, scanning signal S14-61 is output from the scanning signal circuit 14, and pixel data signal S13-1 to pixel data signal S13-m of the first line in image display area having 1080 lines are input from the display signal circuit 13 to the liquid crystal panel 15. Similarly, scanning signal S14-62 to scanning signal S14-1140 are sequentially output from the display signal circuit 13 to the liquid crystal panel 15 per one horizontal period of the image input signal lin. Thus, pixel data signal S13-1 to pixel data signal S13-m of the corresponding line are input from the display signal circuit 13 to the liquid crystal panel 15.

[0036] As described above, according to the first embodiment, when number of scanning signal lines of the liquid crystal panel 15 is larger than number of scanning lines of one vertical period of the image input signal lin, the controller 11, for the image display area in the vertical direction of the liquid crystal panel 15, outputs the input pulse S11b, clock signal S11c and the output enable signal S11d in the first operation mode and, for the blanking area at the upper side and the lower side of the screen in the vertical direction, outputs the input pulse S11b, the clock signal S11c and the output enable signal S11d in the second operation mode, therefore, though the liquid crystal panel 15 of relatively simple configura-

tion using the amorphous silicon technique is used, complete blanks can be written at the upper side and the lower side.

5 Second Embodiment

[0037] Further, a second embodiment according to the present invention will be described.

[0038] Figure 3 is a block diagram showing an electrical configuration of a liquid crystal display according to a second embodiment of the present invention, and same numerals are applied to same elements in Fig. 1.

[0039] The liquid crystal display is provided with a controller 21 different from a controller 11 in Fig. 1. The controller 21 receives image signal inH such as an interlace signal of an HDTV [High Definition Television] signal in which a scanning line for one vertical period is half or less than a scanning signal of a liquid crystal panel 15 and outputs an input pulse S21b, the clock signal S21c and the output enable signal S21d in a first operation mode for an image display area in a vertical direction of a screen of the liquid crystal panel 15. In the first operation mode, a scanning signal circuit 14 receives the input pulse S21b, the clock signal S21c and the output enable signal S21d and outputs a plurality of scanning signals for one horizontal period of the image input signal inH.

[0040] Figure 4 is a timing chart of each section for explaining operation of the liquid crystal display, a vertical axis shows a logic level and a horizontal axis shows a time. Figure 4 shows an operation when an interlace signal of the HDTV in which a number of the scanning lines is 1080 for the image display area is 1080, a total of scanning lines is 1125 is written as the image input signal inH.

[0041] The following shows differences the operation of the second embodiment and operation in the first embodiment.

[0042] That is, in the image display area, the controller 21 outputs the clock signal S21c two times to an pixel data signal S13-1 to pixel data signal S13-m of one line and the scanning signal circuit 14 outputs sequentially a scanning signal S14-k and a scanning signal S14-(k+1) synchronously with the clock signal S21c. As a result, same pixel data signal S13-1 to pixel data signal S13-m are written into the liquid crystal panel 15 of two lines and an image is enlarged. At this time, the output enable signal S21d is not always in active mode, a pulse width is made narrow and pulse widths for a first writing time and a second writing time of pixel data signal S13-1 to pixel data signal S13-m are similar. Thus, it is avoided that a rising of pixel data signal S13-1 to pixel data signal S13-m input into data signal line Yl to data signal line Ym becomes slow, and thereby no luminance difference occurs in pixel data signal S13-1 to pixel data signal S13-m. Other operations are similar to those of the first embodiment.

[0043] As above described, according to the second

embodiment, when the controller 21 receives the image input signal inH in which the scanning line of one vertical period is half or less of the scanning signal line of the liquid crystal panel 15, the controller 21 outputs the clock signal S21c two times and the scanning signal circuit 14 outputs sequentially the scanning signal S14-k and the scanning signal S14- (K+1) synchronously with the clock signal S21c, therefore, the image is enlarged and blanking lines area written at an upper side and a lower side of an image display area with relatively simple configuration.

[0044] It is apparent that the present invention is not limited to the above embodiments but may be changed and modified without departing from the scope and spirit of the invention.

[0045] For example, the liquid crystal panel is not limited to the active-matrix type and a passive-matrix type may be used. Also, it is possible to increase or decrease a number of scanning lines of the image input scanning signal, a number of scanning lines for the blanking area, a number of scanning lines in the image display area and a number of scanning lines of the liquid crystal panel 15 in accordance with necessity. In the second embodiment, pixel data signal S13-1 to pixel data signal S13-m may be written three or more times in accordance with the number of the scanning signals of the liquid crystal panel 15, not limited to twice. The display signal circuit 13 shown in Fig. 1 and Fig. 3 may directly receive an image input signal in and output pixel data signal S13-1 to pixel data signal S13-m. Further, the present invention may be applied to all apparatuses for displaying an image by supplying pixel data to pixel areas selected by a scanning signal image, for example, a PDP (Plasma Display Panel).

Claims

1. A liquid crystal display characterized by comprising: a liquid crystal panel (15) provided with a plurality of data signal lines (Y1 to Ym) for inputting pixel data signals (S13-1 to S13-m), a plurality of scanning signal lines (X1 to Xn) for inputting scanning signals (S14-1 to S14-n) and a plurality of pixel areas arranged at intersection points of said data signal lines (Y1 to Ym) and said scanning signal lines (X1 to Xn) and for displaying an image corresponding to said pixel data signals (S13-1 to S13-m) by supplying said pixel data signals (S13-1 to S13-m) to selected pixel areas selected by said scanning signals (S14-1 to S14-n) among said pixel areas;

a display signal circuit (13) for sending said pixel data signals (S13-1 to S13-m) to said data signal lines (Y1 to Ym) in accordance with image input signals (lin);

a scanning signal circuit (14) for inputting an input pulse (S11b) used to generate said scan-

ning signals (S14-1 to S14-n), moving synchronously with a clock signal (S11c) and for sending said input pulse (S11b) to said scanning signal lines (X1 to Xn) as said scanning signals (S14-1 to S14-n) when an output instruction signal (S11d) is input; and

a controller (11, 21) for inputting said image input signals (lin) and for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) to said scanning signal circuit (14); said controller (11, 21), when a number of said scanning signal lines (X1 to Xn) is larger than a number of scanning lines of said image input signals (lin) for a vertical period, for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) in a first operation mode for an image display area in a vertical direction of a screen of said liquid crystal panel (15) and for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) in a second operation mode for a blanking area in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.

2. The liquid crystal display according to Claim 1, characterized in that in said first operation mode, said scanning signal circuit (14) outputs said scanning signal (S14-61 to S14-S14-1140) once for one horizontal period of said image input signal (lin) and in said second operation mode, said scanning signal circuit (14) outputs a plurality of said scanning signals for said blanking area at a same time.
3. The liquid crystal display according to Claim 1, characterized in that in said first operation mode, said scanning signal circuit (14) outputs said scanning signals plural times for one horizontal period of said image input signal (lin) in order to enlarge said image and in said second operation mode, said scanning signal circuit (14) outputs a plurality of said scanning signals for said blanking area at a same time.
4. The liquid crystal display according Claim 1, characterized in that in said second operation mode, said scanning signal circuit (14) outputs said plurality of said scanning signals into an odd line and an even line separated from each of said scanning signal lines (X1 to Xn).
5. The liquid crystal display according to Claim 4, characterized in that in said second operation mode, said scanning signal circuit (14) inverts polarities of said scanning signals for said odd line and said even line.

6. The liquid crystal display according to Claim 1, characterized in that said liquid crystal panel (15) is an active matrix liquid crystal panel (15) using a thin film transistor of amorphous silicon as an active element.
7. A driving method for a liquid crystal display characterized by comprising:
a step, when a number of scanning signal lines (X1 to Xn) of a liquid crystal panel (15) is larger than a number of scanning lines of image input signals (lin) for a vertical period, of outputting a scanning signal for one horizontal period of image input signal (lin) for an image display area in a vertical direction of a screen of said liquid crystal panel (15) and of outputting a plurality of scanning signals at a same time for a blanking area in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.
8. The driving method for the liquid crystal display according to Claim 7, characterized in that said plurality of said scanning signals are output separately into odd lines and even lines for said blanking area in which no image is displayed at said upper side and said lower side of said screen in said vertical direction.
9. The driving method for the liquid crystal display according to Claim 8, characterized in that polarities of said scanning signals are inverted for said odd lines and said even lines of said scanning signal lines (X1 to Xn).
10. A driving method for a liquid crystal display characterized by comprising:
a step, when a number of scanning signal lines (X1 to Xn) of a liquid crystal panel (15) is larger than a number of scanning lines of image input signals (lin) for a vertical period, of outputting scanning signals plural times for one horizontal period of image input signal (lin) in order to enlarge an image for an image display area in a vertical direction of a screen of said liquid crystal panel (15) and of outputting a plurality of scanning signals at a same time for a blanking area in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.
11. The driving method for the liquid crystal display according to Claim 10, characterized in that said plurality of said scanning signals are output separately into odd lines and even lines for said blanking area in which no image is displayed at said upper side and said lower side of said screen in said vertical direction.
12. The driving method for the liquid crystal display according to Claim 11, characterized in that polarities of said scanning signals are inverted for said odd lines and said even lines of said scanning signal lines (X1 to Xn).
13. A liquid crystal display characterized by comprising:
a liquid crystal panel (15) provided with a plurality of data signal lines (Y1 to Ym) for inputting pixel data signals (S13-1 to S13-m), a plurality of scanning signal lines (X1 to Xn) for inputting scanning signals and a plurality of pixel areas arranged at intersection points of said data signal lines (Y1 to Ym) and said scanning signal lines (X1 to Xn) and for displaying an image corresponding to said pixel data signals (S13-1 to S13-m) by supplying said pixel data signals (S13-1 to S13-m) to selected pixel areas selected by said scanning signals among said pixel areas;
a display signal circuit (13) for sending said pixel data signals (S13-1 to S13-m) to said data signal lines (Y1 to Ym) in accordance with image input signals (lin);
a scanning signal circuit (14) for inputting an input pulse (S11b) used to generate said scanning signals, moving synchronously with a clock signal (S11c) and for sending said input pulse (S11b) to said scanning signal lines (X1 to Xn) as said scanning signals when an output instruction signal (S11d) is input; and
a controller (11, 21) for inputting said image input signals (lin) and for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) to said scanning signal circuit (14); said controller (11, 21), when a number of said scanning signal lines (X1 to Xn) is larger than a number of scanning lines of said image input signals (lin) for a vertical period, for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) in a first operation mode for an image display period in a vertical direction of a screen of said liquid crystal panel (15) and for outputting said input pulse (S11b), said clock signal (S11c) and said output instruction signal (S11d) in a second operation mode for a blanking period in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.
14. The liquid crystal display according to Claim 13, characterized in that in said first operation mode, said scanning signal circuit (14) outputs said scanning signal once for one horizontal period of said image input signal (lin) and in said second operation mode, said scanning signal circuit (14) outputs a plurality of said scanning signals for said blanking period at a same time.

15. The liquid crystal display according to Claim 13, characterized in that in said first operation mode, said scanning signal circuit (14) outputs said scanning signals plural times for one horizontal period of said image input signal (lin) in order to enlarge said image and in said second operation mode, said scanning signal circuit (14) outputs a plurality of said scanning signals for said blanking period at a same time.
16. A driving method for a liquid crystal display characterized by comprising:
a step, when a number of scanning signal lines (X1 to Xn) of a liquid crystal panel (15) is larger than a number of scanning lines of image input signals (lin) for a vertical period, of outputting a scanning signal for one horizontal period of image input signal (lin) for an image display period in a vertical direction of a screen of said liquid crystal panel (15) and of outputting a plurality of scanning signals at a same time for a blanking period in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.
17. A driving method for a liquid crystal display characterized by comprising:
a step, when a number of scanning signal lines (X1 to Xn) of a liquid crystal panel (15) is larger than a number of scanning lines of image input signals (lin) for a vertical period, of outputting scanning signals plural times for one horizontal period of image input signal (lin) in order to enlarge an image for an image display period in a vertical direction of a screen of said liquid crystal panel (15) and of outputting a plurality of scanning signals at a same time for a blanking period in which no image is displayed at an upper side and a lower side of said screen in said vertical direction.

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FIG. 1

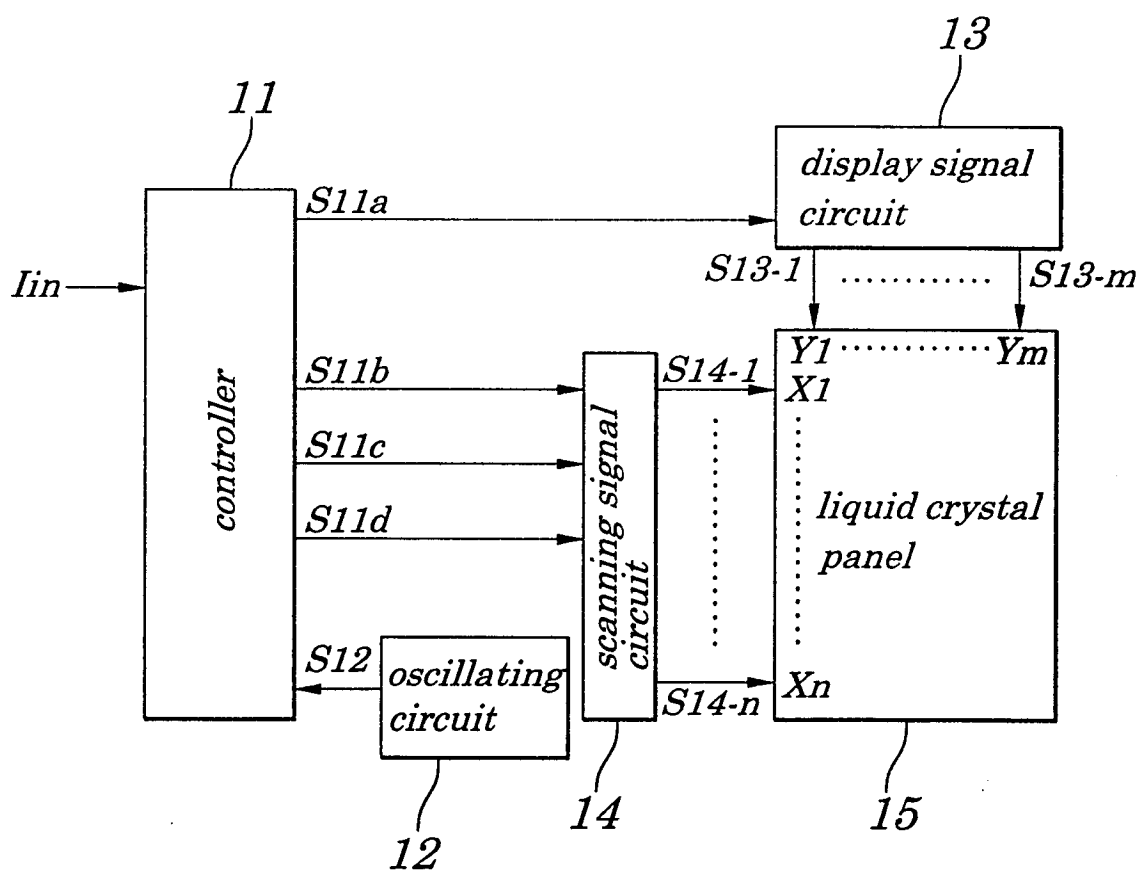


FIG.2A

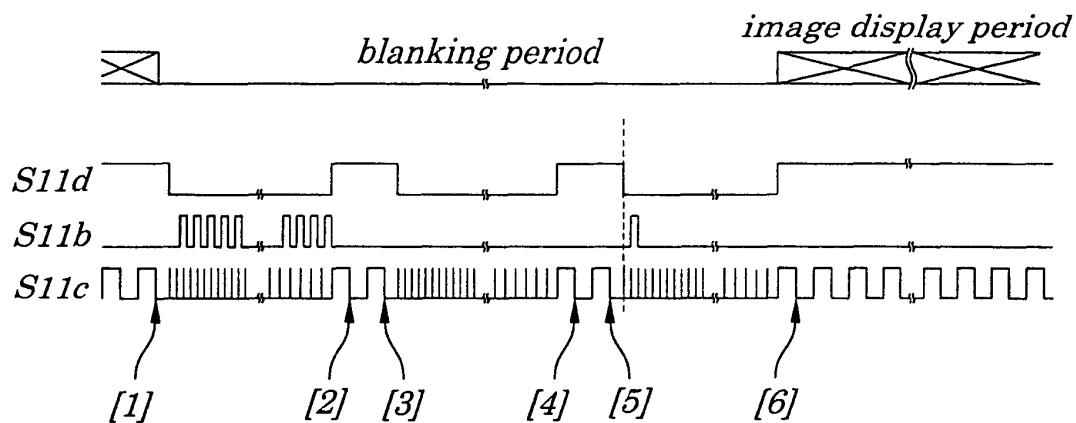


FIG.2B

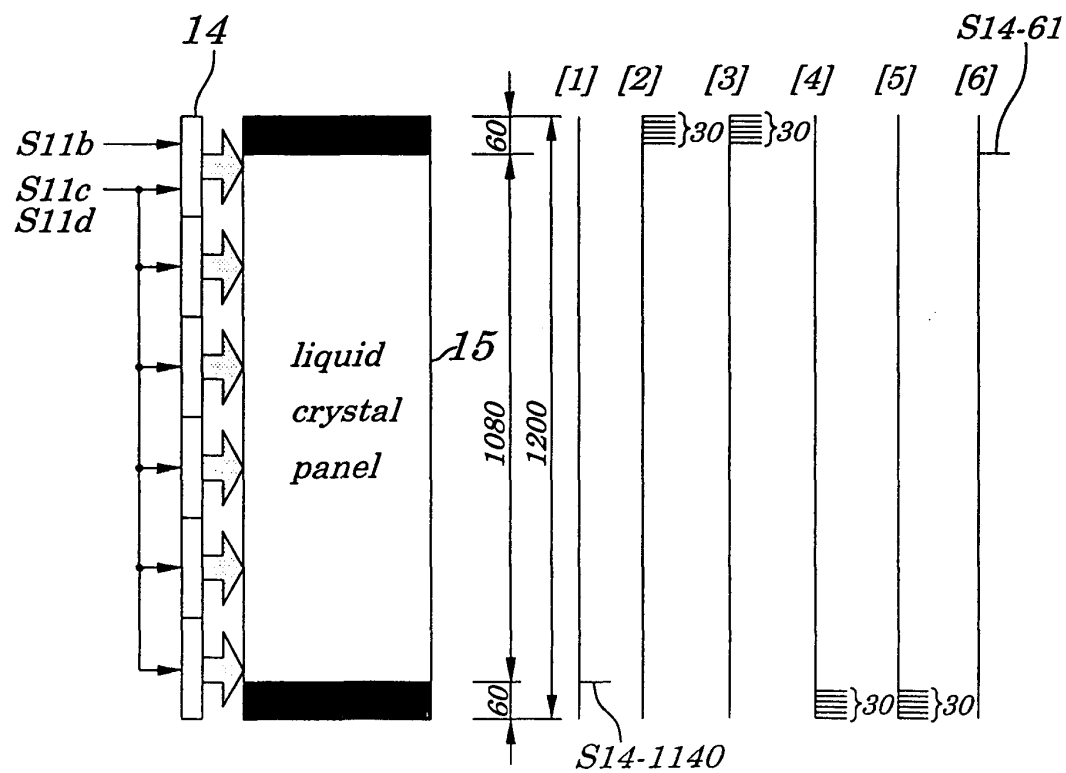


FIG. 3

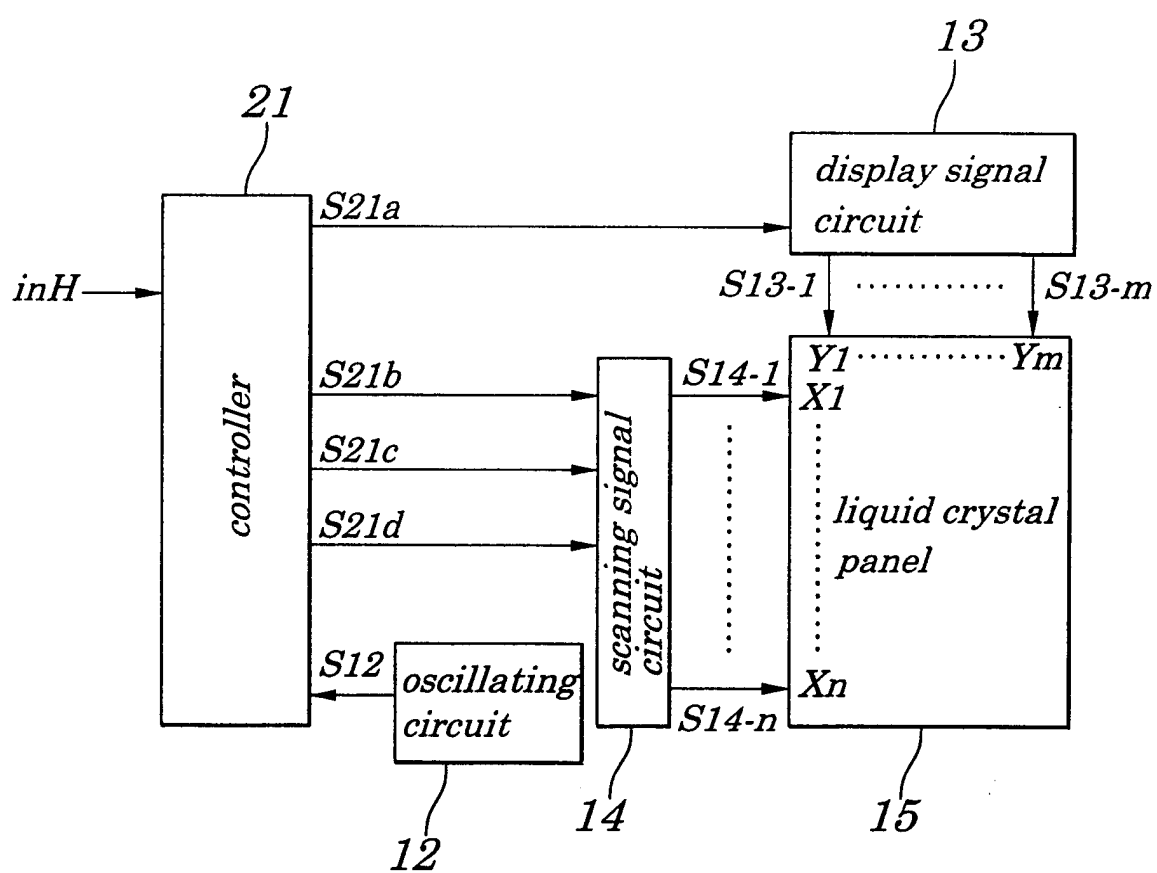


FIG.4

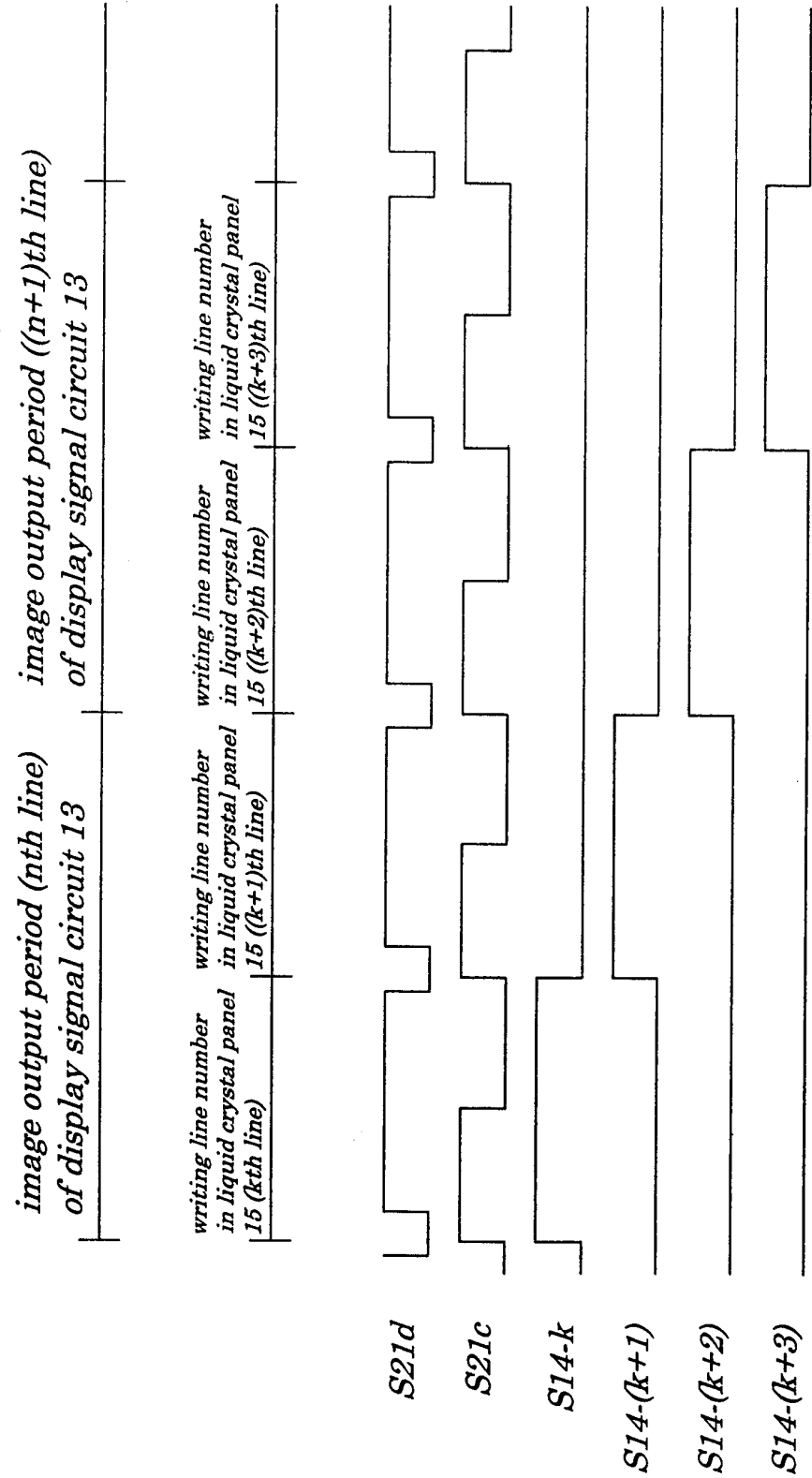


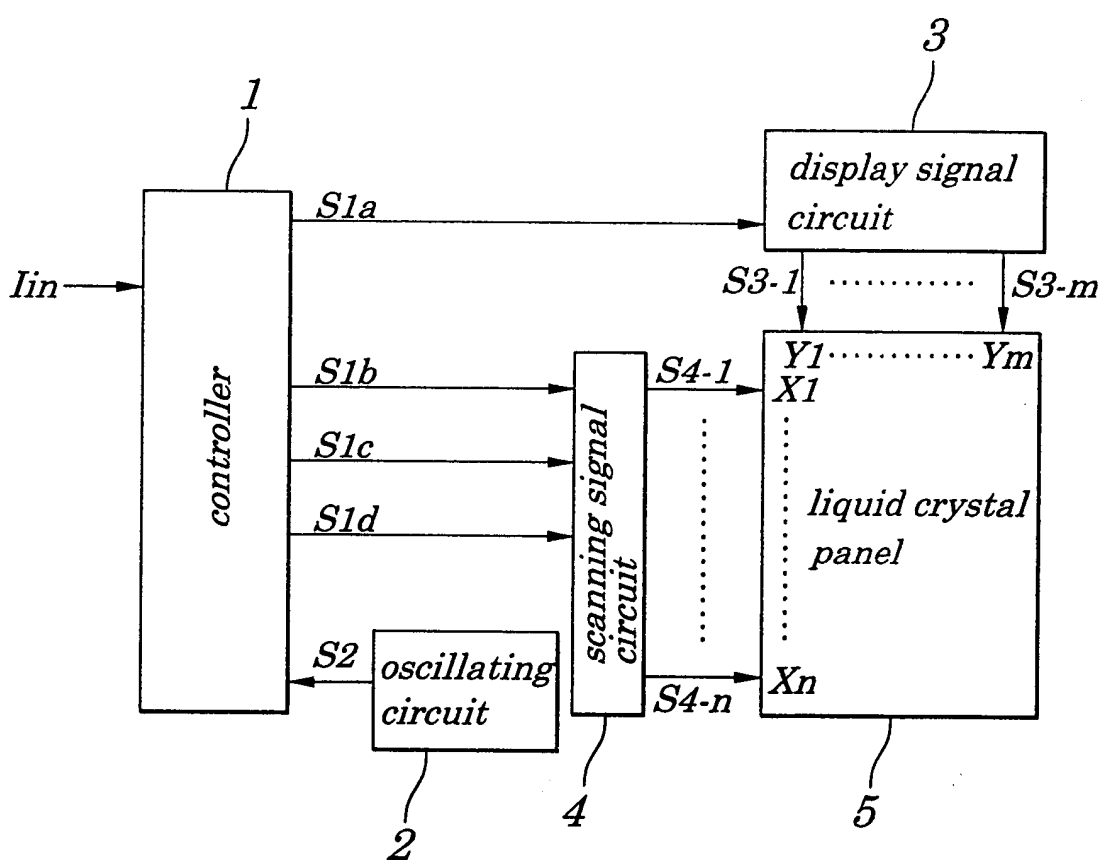
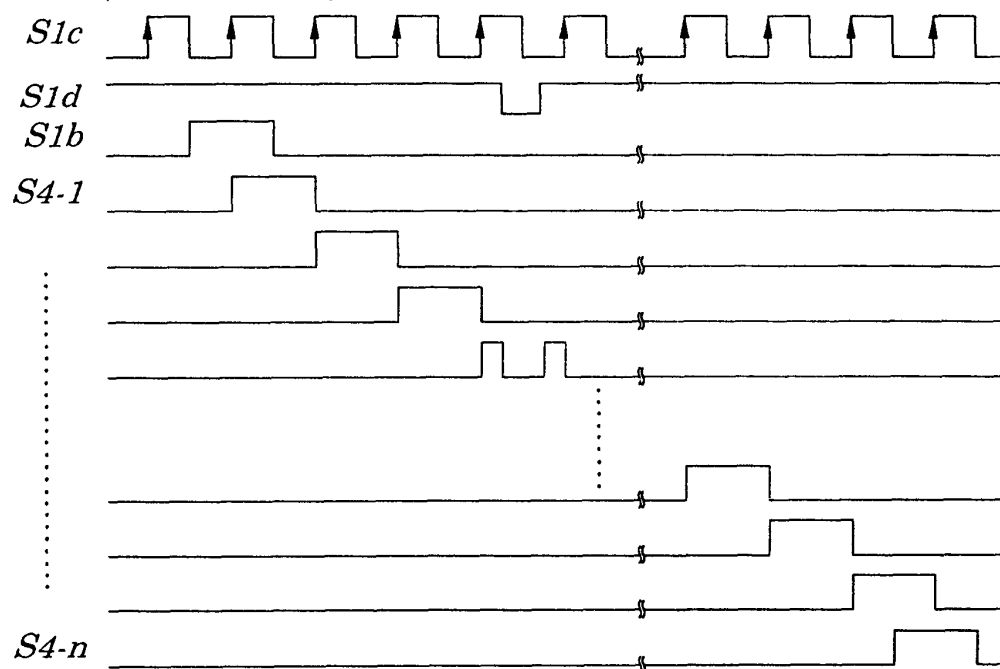
FIG. 5 (PRIOR ART)

FIG. 6 (PRIOR ART)**FIG. 7 (PRIOR ART)**