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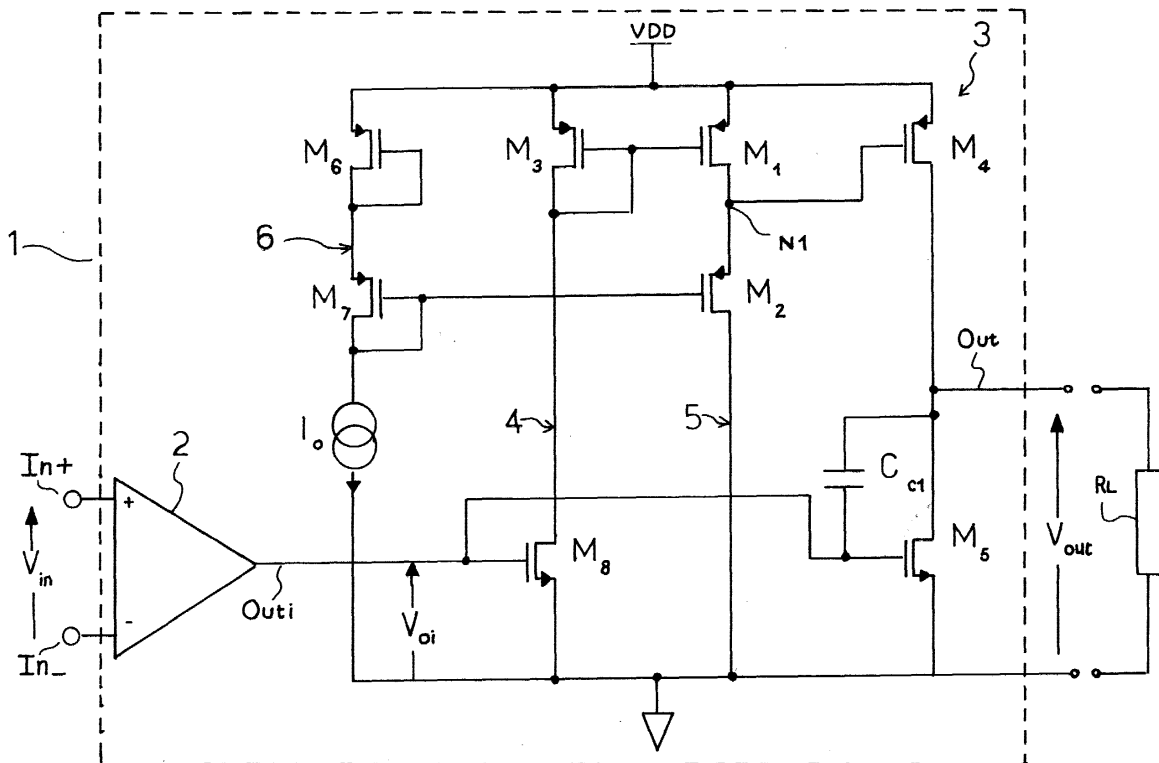
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(54) **An operational amplifier with high gain and symmetrical output-current capability**

(57) An operational amplifier comprises a first stage (2) and a second stage (3) with an input connected to an output (V_{oi}) of the first stage (2) and an output (Out) connectible to a load (RL), the second stage (3) comprising, between its input and its output, a first signal path (M_5) for driving the load (RL) in a first direction, and

a second signal path (M_8, M_3, M_1, M_2, M_4) for driving the load (RL) in the opposite direction. The first and second signal paths have substantially equal gains for small signals, substantially equal output impedances for small and large signals, and substantially equal output-current capabilities.



Description

[0001] The present invention relates to an operational amplifier.

[0002] Operational amplifiers are used in various applications in analogue electronics.

[0003] As is well known, an operational amplifier is a circuit characterized by having: two inputs, that is, an inverting or negative input and a non-inverting or positive input, an output (a "single-ended" amplifier) or two outputs (a "double-ended" amplifier, also known as a "fully differential" amplifier), theoretically infinite differential input impedance (in practice, operational amplifiers have a very high differential input impedance), theoretically infinite gain (in practice, very high gain), voltage-driven output voltage, theoretically infinite output-current capability which is also symmetrical in the two cases of a leading edge and of a trailing edge of the output signal, and a theoretically infinite rate of variation ("slew rate") of the output current over time.

[0004] In practice, operational amplifiers which are symmetrical from the point of view of their output-current capabilities but which have a single amplification stage and hence low overall gain, are known.

[0005] Other known operational amplifiers in practice comprise two amplification stages in cascade and thus have a sufficiently high overall gain. However, these operational amplifiers are not symmetrical with regard to their output-current capabilities.

[0006] Operational amplifiers with more than two stages are critical from the stability point of view. In fact it is known that operational amplifiers are normally used with a feedback network between input and output. To ensure the stability of the feedback loop in which the operational amplifier is connected, it is necessary to provide compensation capacitors within the amplifier. This increases the area occupied by the amplifier and reduces the slew rate.

[0007] In view of the prior art described, an object of the present invention is to provide an operational amplifier with sufficiently high gain which is not critical from the stability point of view, and which at the same time is symmetrical from the point of view of its output-current capability.

[0008] According to the present invention, this object is achieved by an operational amplifier comprising a first stage and a second stage with an input connected to an output of the first stage and an output connectible to a load, the second stage comprising, between its input and its output, a first signal path for driving the load in a first direction and a second signal path for driving the load in the opposite direction, characterized in that the first and second signal paths have substantially equal gains for small signals, substantially equal output impedances for small and large signals, and substantially equal output-current capabilities.

[0009] The characteristics and the advantages of the present invention will be made clearer by the following

detailed description of a possible practical embodiment thereof, shown purely by way of non-limiting example, in the single drawing given on the appended drawing sheet.

5 **[0010]** This drawing shows the circuit diagram of an operational amplifier according to a possible practical embodiment of the present invention.

[0011] The operational amplifier, generally indicated 1, comprises a first amplification stage 2, or input stage. The first amplification stage 2 has two inputs, that is, a positive or non-inverting input $In+$ and a negative or inverting input $In-$, between which an input signal V_{in} can be applied.

10 **[0012]** The first, "single-ended" amplification stage 2 has an output Out_i . The output Out_i of the first amplification stage 2 is supplied to a second amplification stage, generally indicated 3.

[0013] The second amplification stage 3 comprises a final stage M_4, M_5 which constitutes a Class B push-pull output stage. The output stage is formed by a p-channel MOSFET M_4 and by an n-channel MOSFET M_5 connected in series between a supply voltage VDD and a reference voltage, that is, the ground in the embodiment shown. In particular, the MOSFET M_4 has its source electrode connected to the supply voltage and its drain electrode connected to the drain electrode of the MOSFET M_5 the source electrode of which is connected to ground. The common node between the MOSFETs M_4 and M_5 forms an output Out of the operational amplifier.

20 **[0014]** The second amplification stage 3 comprises two signal paths. A first signal path or "n-path" is constituted by the path which goes from the output Out_i of the first amplification stage 1 to the output Out of the operational amplifier, passing through the n-channel MOSFET M_5 of the final stage. A second signal path or "p-path" is constituted by the path which goes from the output Out_i of the first amplification stage 1 to the output Out of the operational amplifier, passing through the p-channel MOSFET M_4 of the final stage. The first signal path or "n-path" serves for driving the load, indicated RL in the drawing, in a first direction, particularly towards the ground. The second signal path or "p-path" serves for driving the load in the opposite direction, in particular, towards the supply voltage VDD.

25 **[0015]** The n-channel MOSFET M_5 has its gate electrode connected to the output Out_i of the first amplification stage 2. The MOSFET M_5 of the output stage is therefore driven directly by the output Out_i of the first amplification stage 2. A compensation capacitor C_{c1} is also connected between the gate electrode and the drain electrode of the MOSFET M_5 .

30 **[0016]** For driving the p-channel MOSFET M_4 , however, the second stage 3 comprises a pair of circuit branches 4, 5. The branch 4 comprises a p-channel MOSFET M_3 and an n-channel MOSFET M_8 connected in series between the supply voltage VDD and the ground. The MOSFET M_3 is connected in a diode configuration, that is, it has its gate electrode short-circuited

to its drain electrode. The MOSFET M_8 has its gate electrode connected to the output Out_i , that is, it is driven by the first amplification stage 2.

[0017] The branch 5 comprises two p-channel MOSFETs M_1 and M_2 , connected in series between the supply voltage VDD and the ground. The MOSFET M_1 , which has its source electrode connected to the supply voltage VDD, has its gate electrode connected to the gate electrode of the MOSFET M_3 . The drain electrode of the MOSFET M_1 , which is also the source electrode of the MOSFET M_2 , is connected to the gate electrode of the MOSFET M_4 of the final stage.

[0018] Owing to the way in which the MOSFETs M_3 and M_1 are connected to one another, the two circuit branches 4 and 5 form a current mirror. This current mirror also acts substantially as a level translator for the MOSFET M_4 .

[0019] The operational amplifier 1 also comprises a biasing circuit for the MOSFET M_2 . The biasing circuit comprises a circuit branch 6 with a pair of p-channel MOSFETs M_6 , M_7 , connected as diodes and connected in series between the supply voltage VDD and a current generator I_o . In practice, the current generator I_o may also be formed by transistors in accordance with one of the known solutions, so that the current I_o has a value which is substantially constant with variations in the supply voltage VDD, with a high output impedance.

[0020] The dimensions of the MOSFETs M_1 , M_2 , M_3 , M_4 , M_5 and M_8 of the second amplification stage 3 may be selected in accordance with the following considerations.

[0021] First of all, the n-channel MOSFET M_5 of the final stage will have to be relatively highly conductive so as to be able to absorb a relatively high current from the load.

[0022] If the ratio between the transconductance g_{mN5} of the n-channel M_5 of the final stage and the transconductance g_{mN8} of the n-channel MOSFET M_8 is K, that is:

$$g_{mN5}/g_{mN8} = K,$$

the dimensions of the remaining MOSFETs M_1 , M_2 , M_3 , and M_4 of the second stage will be such that their transconductances g_{mP1} , g_{mP2} , g_{mP3} and g_{mP4} satisfy the equation:

$$(g_{mP1}/g_{mP3}) * (g_{mP4}/g_{mP2}) = K.$$

[0023] As is clear to an expert in the art, this can easily be achieved by means of the W/L ratios (where W and L are the channel width and length of the MOSFET, respectively) of the individual MOSFETs.

[0024] Preferably, since:

- the p-channel MOSFET M_4 in the final stage will

have to have dimensions such as to be relatively highly conductive so as to be able to supply a relatively high current to the load, and

- the ratio between the transconductance g_{mP1} of the MOSFET M_1 and the transconductance g_{mP3} of the MOSFET M_3 of the current mirror will have to be kept as close as possible to unity in order not to reduce excessively the pass-band of the current mirror for a small signal, the two p-channel MOSFETs M_3 and M_1 of the current mirror have dimensions such that the ratio between their transconductances is substantially equal to 1 (mirroring ratio equal to approximately 1), whereas the p-channel MOSFET M_4 of the final stage and the p-channel MOSFET M_2 have dimensions such that the former has a transconductance value approximately K times greater than the transconductance of the MOSFET M_2 .

[0025] The MOSFETs M_6 , M_7 of the biasing circuit 6 preferably have dimensions such that the ratio between their transconductance values and the transconductance of the MOSFETs M_1 , M_2 , M_3 is substantially equal to 1.

[0026] The operational amplifier described operates in the following manner.

[0027] First of all, the biasing circuit 6 sets the working voltage at the gate of the MOSFET M_2 at a value such that the current which flows in the final stage 3 at rest, that is, in the absence of a signal V_{in} at the input of the operational amplifier 1, is approximately equal to K times the current I_o , where, as explained above, K is the ratio between the transconductance g_{mP4} of the p-channel MOSFET M_4 and the transconductance g_{mP2} of the p-channel MOSFET M_2 .

[0028] It is important to note that, in the second signal path or p-path, the node N1 connected to the gate of the p-channel MOSFET M_4 of the final stage is a low-impedance node. This node is in fact connected to the source electrode of the p-channel MOSFET M_2 which is itself a low-impedance node; moreover, since the drain of the MOSFET M_2 is connected to ground, the impedance seen by the node N2 is further reduced. By virtue of the fact that the node N1 has low impedance, it is not necessary to provide for its compensation.

[0029] It is assumed that a load of impedance equal to R_L is applied to the output Out of the operational amplifier 1 and a low-frequency (voltage) signal V_{in} is applied between the inputs $In+$ and $In-$. It is also assumed that the first amplification stage 2 has a gain of A_1 , so that the signal V_{oi} which is present at the output Out_i of the first amplification stage 2 is

$$V_{oi} = V_{in} * A_1$$

[0030] The first signal path or "n-path" will be considered. If g_{mN5} is the transconductance of the MOSFET

M₅,

$$V_{out} = -V_{oi} * g_{mN5} * RL.$$

[0031] The gain (in absolute value) of the second amplification stage 3 along the n-path is therefore:

$$A2 = (V_{out}/V_{oi}) = g_{mN5} * RL$$

and the overall gain of the operational amplifier along the n-path is:

$$A = A1 * A2 = A1 * g_{mN5} * RL.$$

[0032] The second signal path or p-path will now be considered. Assuming that g_{mN8} , g_{mP3} , g_{mP1} , g_{mP2} and g_{mP4} are the respective transconductances of the MOSFETs M₈, M₃, M₁, M₂ and M₄, in this case:

$$V_{out} = V_{oi} * g_{mN8} * (g_{mP1}/g_{mP3}) * (g_{mP4}/g_{mP2}) * RL$$

[0033] With the dimensions of the MOSFETs described above:

$$(g_{mP1}/g_{mP3}) = 1$$

and

$$(g_{mP4}/g_{mP2}) = K$$

[0034] Therefore, for the p-path:

$$V_{out} = V_{oi} * g_{mN8} * K * RL$$

but, again on the basis of the dimensions of the MOSFETs described above,

$$g_{mN8} * K = g_{mN5}$$

the gain A2 of the second amplification stage 3 along the p-path is equal to the gain of the second amplification stage 3 along the n-path.

[0035] The operational amplifier 1 therefore has perfect symmetry between the p-path and the n-path, since the gain along the two paths is equal, except for mismatch between the components. However, any asymmetry resulting from mismatch between the components would certainly be of a lower order than asymmetry resulting from different circuit topology of the p-path and the n-path.

[0036] Clearly, variants and/or additions to the embodiment described and illustrated above may be provided.

[0037] For example, although, in the embodiment shown and described, reference was made to MOS field-effect transistors, naturally this should not be considered a limitation of the invention since transistors of other types may in fact also be used.

[0038] Although the dimensions of the transistors given in the embodiment described are preferred, these are in no way limiting. An expert in the art can easily design alternative dimensions for the transistors without the resulting circuit thereby being considered not to be included within the scope of the protection of the present invention defined in the appended claims.

[0039] Moreover, the voltage for biasing the MOSFET M₂ which, in the embodiment described, is generated by a biasing circuit 6 forming part of the operational amplifier, may be generated outside the operational amplifier by a biasing circuit, for example, similar to the biasing circuit described, which may even be common to several operational amplifiers.

25 Claims

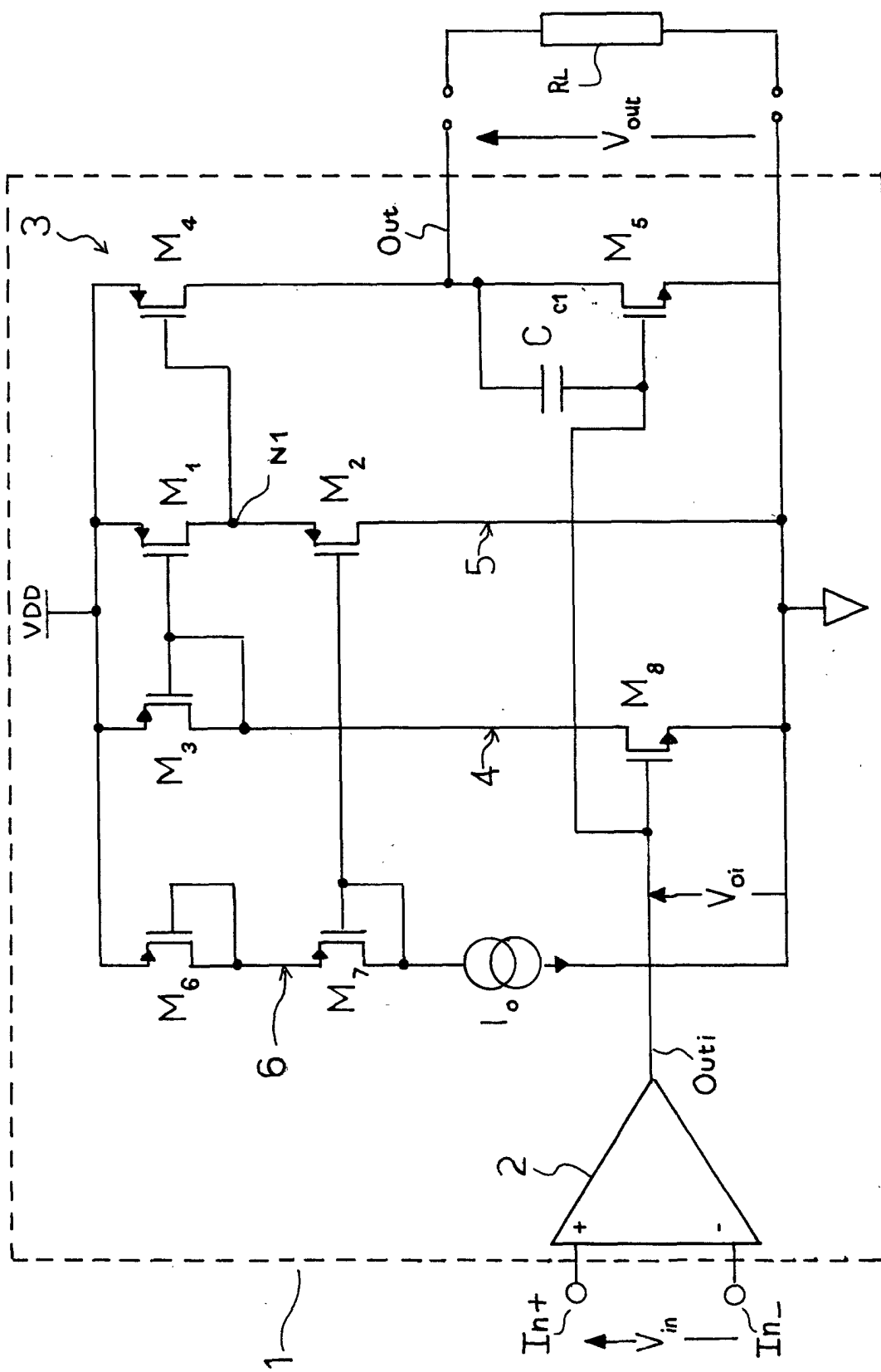
1. An operational amplifier comprising a first stage (2) and a second stage (3) with an input connected to an output (V_{oi}) of the first stage (2) and an output (Out) connectible to a load (RL), the second stage (3) comprising, between its input and its output, a first signal path (M₅) for driving the load (RL) in a first direction, and a second signal path (M₈, M₃, M₁, M₂, M₄) for driving the load (RL) in the opposite direction, characterized in that the first and second signal paths have substantially equal gains for small signals, substantially equal output impedances for small and large signals, and substantially equal output-current capabilities.
2. An operational amplifier according to Claim 1, in which the second stage (3) comprises a final push-pull stage (M₄, M₅) with a first transistor (M₅) and a second transistor (M₄) belonging to the first signal path and to the second signal path, respectively, for driving the load (RL) in the first direction and in the second direction, respectively.
3. An operational amplifier according to Claim 2, in which the first transistor (M₅) of the final stage (M₄, M₅) is driven directly by the output (V_{oi}) of the first stage (2), and the second transistor (M₄) of the final stage (M₄, M₅) is driven by the output (V_{oi}) of the first stage (2) via a signal-level translation circuit (M₈, M₃, M₁, M₂).
4. An operational amplifier according to Claim 3, in which a control electrode of the second transistor

(M₄) of the final stage (M₄, M₅) is driven by a low-impedance output node (N1) of the level-translation circuit (M₈, M₃, M₁, M₂).

5. An operational amplifier according to Claim 4, characterized in that the level-translation circuit (M₈, M₃, M₁, M₂) comprises a pair of circuit branches (4, 5) connected as a current mirror, a first branch (4) of the pair comprising a first transistor (M₈) driven by the output (Out_i) of the first stage (2), in series with a second transistor (M₃) which is connected as a diode and the control electrode of which is connected to the control electrode of a first transistor (M₁) of the second branch (5) of the pair of circuit branches (4, 5), the first transistor (M₁) of the second branch (5) being connected in series with a second transistor (M₂) of the second branch (5), the common node (N1) between the first and second transistors (M₁, M₂) of the second branch being the low-impedance node which drives the second transistor (M₄) of the final stage (M₄, M₅). 5
6. An operational amplifier according to Claim 5, further comprising a circuit (M₆, M₇, I_o) for biasing the second transistor (M₂) of the second branch (5) of the pair of branches (4, 5). 10
7. An operational amplifier according to Claim 6, in which the dimensions of the transistors are such that the ratio between the transconductance of the second transistor (M₄) of the final stage (M₄, M₅) and the transconductance of the second transistor (M₂) of the second branch (5), multiplied by the ratio between the transconductance of the first transistor (M₁) of the second branch (5) and the transconductance of the second transistor (M₃) of the first branch (4), is substantially equal to the ratio between the transconductance of the first transistor (M₅) of the final stage (M₄, M₅) and the transconductance of the first transistor (M₈) of the first branch. 15
8. An operational amplifier according to Claim 7, in which the dimensions of the second transistor (M₃) of the first branch (4) and of the first transistor (M₁) of the second branch (5) are such that the ratio between their transconductances is substantially equal to 1, and the dimensions of the second transistor (M₂) of the second branch (5) are such that the ratio between the transconductance of the second transistor (M₄) of the final stage (M₄, M₅) and the transconductance of the second transistor (M₂) of the second branch (5) is substantially equal to the ratio between the transconductance of the first transistor (M₅) of the final stage (M₄, M₅) and the transconductance of the first transistor (M₈) of the first branch. 20
9. An operational amplifier according to Claim 8, in 25

which the transistors (M₁, M₂, M₃, M₄, M₅, M₈) are MOSFETs.

10. An operational amplifier according to Claim 9, in which the first transistor (M₅) of the final stage (M₄, M₅) and the first transistor (M₈) of the first branch (4) are n-channel MOSFETs, and the second transistor (M₄) of the final stage (M₄, M₅), the second transistor (M₃) of the first branch (4), and the transistors (M₁, M₂) of the second branch (5) are p-channel MOSFETs. 30





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0091

DOCUMENTS CONSIDERED TO BE RELEVANT			
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A	* page 232; figure 4 *	5,6,9,10	

The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22 June 2000	Examiner Tyberghien, G
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 00 83 0091

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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