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(54) **Semiconductor memory devices**

(57) A method is provided for refreshing memory cells in semiconductor memories. The method includes the steps of providing a semiconductor memory having memory cells and redundancy memory cells in at least one memory array and an associated redundancy memory array, respectively (1002). The memory cells and the redundancy memory cells are independently refreshed, using addresses generated by a row address counter and a redundancy address counter, respectively (1008). The method optionally includes the step of disabling redundancy wordlines coupled to unused redundancy memory cells, using a master fuse signal corresponding to a master fuse of the semiconductor memory (1004).

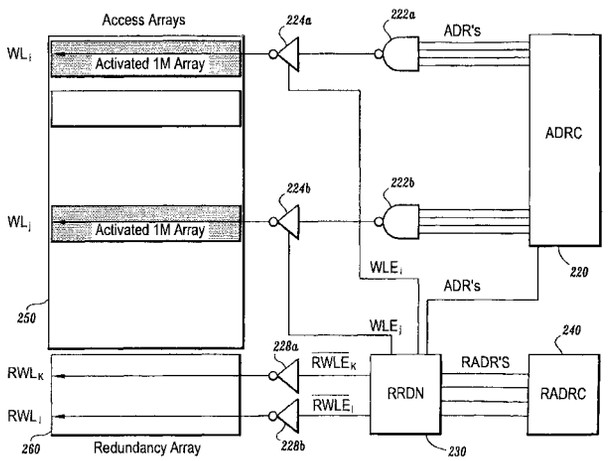

FIG. 2

EP 1 137 010 A8