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(11) **EP 1 152 431 A8**

(12) **CORRECTED EUROPEAN PATENT APPLICATION**

Note: Bibliography reflects the latest situation

(15) Correction information:

**Corrected version no 1 (W1 A2)**  
**Corrected Kind of Document code A2**  
**Previously published as A1**

(51) Int Cl.7: **G11C 11/406**, G11C 11/407,  
G11C 5/14, G11C 11/4074

(48) Corrigendum issued on:

**30.01.2002 Bulletin 2002/05**

(43) Date of publication:

**07.11.2001 Bulletin 2001/45**

(21) Application number: **01118907.3**

(22) Date of filing: **20.04.2000**

(84) Designated Contracting States:

**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE**

Designated Extension States:

**AL LT LV MK RO SI**

(30) Priority: **05.08.1999 JP 22260599**

(62) Document number(s) of the earlier application(s) in  
accordance with Art. 76 EPC:

**00108653.7 / 1 074 993**

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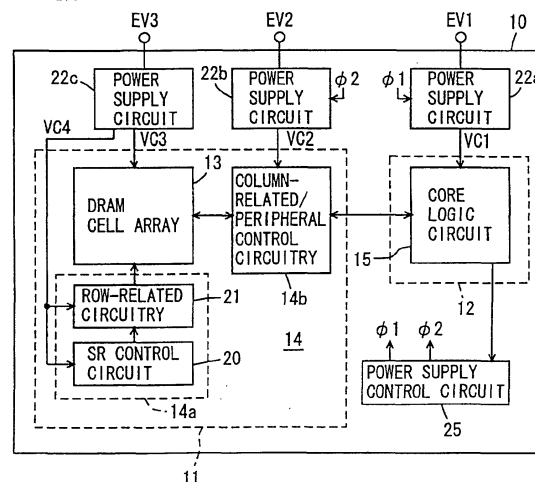
Remarks:

This application was filed on 03 - 08 - 2001 as a  
divisional application to the application mentioned  
under INID code 62.

(54) **Semiconductor memory device with reduced current consumption in data hold mode**

(57) A power supply circuit (22c) generating a power supply voltage for refresh-related circuitry (14a) and a power supply circuit (22b) for column-related/peripheral control circuitry (14b) are controlled by a power supply control circuit (25) to be put in different power supply voltage supplying states in a self refresh mode. In the self refresh mode, only self refresh-related circuitry receives a power supply voltage to perform refresh operation. A reduced current consumption can be achieved in the self refresh mode while fast access operation is not deteriorated.

F I G. 2



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