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(54) **Image sensor pixel for configurable output**

(57) A pixel design for CMOS image sensors that has a high frame rate potential and motion capture capabilities. The pixel architecture provides for a CMOS based, active pixel image sensor comprising an array of pixels formed in rows and columns, with each of the pixels containing at least one active circuit element. There are a plurality of output channels formed such that each

of the output channels are operatively connected to a subset of pixels wherein each of the pixel have an attribute that is the same. The pixel architecture also provides an output gate region and a shutter gate region that are symmetric about the center of the pixel. By arranging the shutter and transfer gates, a symmetric manner about the center of the pixel, a more efficient transfer of electrons to these gates is provided.

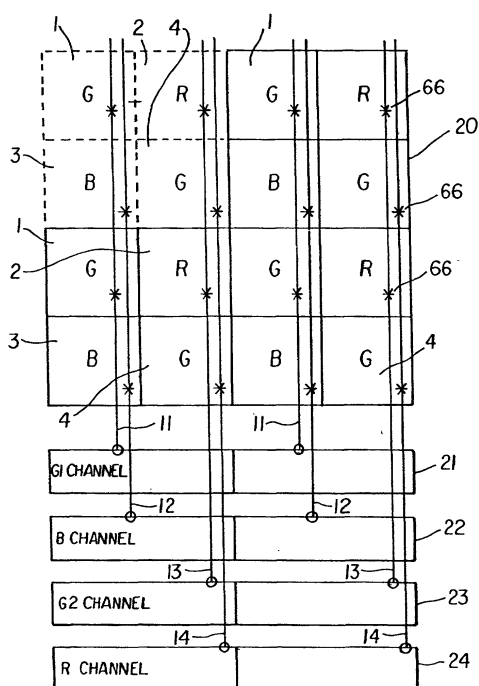


FIG. 2a



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 01 20 1359

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X	US 4 504 854 A (MASUDA MICHIO) 12 March 1985 (1985-03-12) * abstract * * column 1, line 36 - column 2, line 10 * * column 2, line 30 - column 7, line 30 * * figure 6 *	1-10	
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The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 18 February 2004	Examiner Bernabé Prieto, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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