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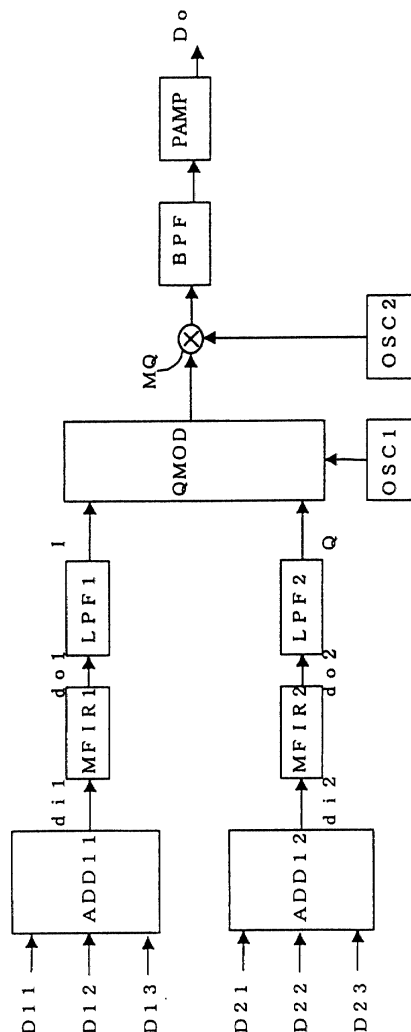
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Small-scale and low-power consumption multipliers and filter circuits

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A multiplication of digital data by small-scale and low-power consumption circuits. ANDs of all combinations of the respective bits of first digital data and the respective bits of second digital data are generated. A capacitive coupling is configured by a plurality of capacitances each having a capacity proportional to the sum of weights of pair of bits corresponding to each AND, an output of the capacitive coupling is connected to an inverting amplifier, and a multiplication result is output as analog data.

FIG. 1



Description

BACKGROUND OF THE INVENTION

5 Field of the Invention

[0001] The present invention relates to multipliers and filters circuit based on the conception of the multiplier, and particularly relates to multipliers and filter circuits for outputting a mutual multiplication of digital data as analog data.

10 Description of the Related Art

[0002] For example, in spread-spectrum communications for mobile communications, a high-speed correlation operation should be executed. For this purpose, a SAW filter, a sliding correlator, or a matched filter has been used. Among these correlation operating means, because the means has a high initial synchronization capture rate, the matched filter is favorable in view of communication performance. However, there is a problem that circuit scale and power consumption grow larger when the matched filter is composed of digital circuits. Moreover, in a transmitting section of a mobile communication terminal, a Nyquist filter is required, and the scale of an arithmetic circuit for the sum and the products of digital data and filter coefficient data is large, so that the output data must be further converted to analog signals.

[0003] In order to solve such a problem, the applicant of the present invention has developed and proposed a large number of arithmetic circuits and filter circuits executing a digital/analog mixed calculation. This proposal is described in Unexamined Japanese Patent Publication Nos. 09-46231, 09-193434, 09-46173, 09-46174, 09-83486, 09-83488, 09-83483, 09-135231, 09-116522, 09-116523, 09-130365, 09-200179, 09-223986, 09-181645, 09-181701, 09-200085, 09-298490, 09-284252, 09-321667, and 10-56442.

[0004] Analog voltage signals for both an input and an output are used in the proposals, therefore the advent of a small-scale and low-power consumption circuit for processing digital signals has been looking forwarded to. Particularly, an arithmetic accuracy was largely influenced by an output accuracy of a sample and hold circuit that holds data in time series, resulting in the arithmetic accuracy was not easily ensured.

30 SUMMARY OF THE INVENTION

[0005] The present invention has been made in consideration of the above-mentioned problem. An object of the present invention is to provide multipliers and filter circuits, which are small scale, and low power consumption as well as suitable for digital multiplication.

[0006] The multiplier according to the present invention generates ANDs (logical products) of all combinations of the respective bits of first digital data and those of second digital data. The multiplier performs a weighted addition by use of a plurality of capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to each AND circuit, or resistances each having a resistance value, which is indirectly proportional to the weight, an amplifier to which outputs of these capacitances or resistances are combined and connected, and a negative feedback capacitance or resistance, which is connected to the amplifier, thereby outputting a multiplication result as an analog voltage.

[0007] Also, the filter circuit according to the present invention is one that adopts the multipliers of the present invention in calculating the sum of products of a plurality of time series digital data and digital multipliers corresponding to these digital data.

[0008] The details of one or more embodiments of the present invention set forth in the description and the accompanying drawings below. Other features, and advantages of the present invention will be apparent from the description, drawings, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

50 **[0009]**

FIG. 1 is a block diagram of a transmitter incorporating filter circuits according to the present invention;

FIG. 2 is a block diagram of the filter circuits shown in FIG. 1;

FIG. 3 is a circuit diagram of AND circuits of the filter circuits shown in FIG. 1;

FIG. 4 is a circuit diagram of adders of the filter circuit shown in FIG. 1;

FIG. 5 is a circuit diagram of the adders shown in FIG. 4;

FIG. 6 is a circuit diagram of selectors of the adders shown in FIG. 5;

FIG. 7 is a circuit diagram of adders incorporated in the filter circuits according to a second embodiment;
 FIG. 8 is a circuit diagram of adders shown in FIG. 7;
 FIG. 9 is a circuit diagram of a multiplier according to a first embodiment of the present invention; and
 FIG. 10 is a circuit diagram of a second embodiment of a multiplier according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] Embodiments of the filter circuits according to the present invention will be specifically explained with reference to drawings accompanying herewith.

[0011] Fig. 1 shows a DS-CDMA (Direct-Sequence-Code-Division-Multiple-Access) transmitter using filter circuits according to the present invention as transmission filters MFIR 1 and MFIR 2. In the transmitter, data of a plurality of lines (three lines in this figure) is input to adders ADD 11 to ADD 12 as in-phase components D11 to D13 and quadrature components D21 to D23. In these adders, the signals of the plurality of lines are combined and added, and the added resultants are output as digital data di1, di2. Digital data di1 and di2 are input to transmission filters MFIR1 and MFIR2, respectively, and multiplied by a coefficient of Nyquist filters. Outputs dol and do2 are input to low-pass filters LPF1 and LPF2, respectively, to remove harmonic noise components therefrom. Outputs I (in-phase components) and Q (quadrature components) of LPF1 and LPF2 are modulated by a quadrature modulator QMOD, and are mixed with carrier waves by a mixer MQ. Thereafter, noise is removed from the modulated resultant by a bandpass filter BPF, and is amplified by a power amplifier PAMP.

[0012] FIG. 2 shows the aforementioned transmission filter MFIR 1. In Fig. 2, data di1 is input to a shift register SR, and stored as time series digital data di11, di12, ..., di1n. Time series digital data is input to taps (multiplier) T1, T2, ..., Tn, calculating ADDs of the predetermined digital multipliers m1, m2, ..., mn. Outputs of the respective taps T1 to Tn are input to an adder TADD to calculate the sum Do. The transmission filter MFIR 2 has the same configuration as that of MFIR1 and therefore the explanation thereof is omitted.

[0013] FIG. 3 shows the aforementioned tap T1, which is composed of AND circuits G1 to GP corresponding to a number (P) of all combinations of data di11 and the respective bits of multiplier m1. In Fig. 3, the number of bits of data di11 and that of bits of m1 are set to s. In this case, there is a relationship between p and s as $p = s^2$. The respective AND circuits G1 to Gp generate outputs M1, 00, M1, 10 ..., M1, s, s. Also, i-th tap Ti generates outputs Mi, 00, mi, 10 ..., Mi, s, s, and AND outputs of all taps are added by TADD. Therefore, each of output signals M1, M2, ..., Mn from the respective taps of FIG. 2 is a signal that includes AND output of s^2 . For the sake of simplicity, assume that the number of input data and that of the multipliers are the same of FIG. 3, however, AND calculation with the different number of bits can be made in the similar way.

[0014] FIG. 4 shows the aforementioned adder TADD. The TDD is composed of a plurality of adders ADD4, 1 to ADD4, (2s-1). The adder ADD4, 1 calculates the sum of ANDs of the least significant bits of data di1k (k = 1 to n) and those of multipliers mk (k = 1 to n) in connection with all taps. Here, AND of the least significant bits is adding data of weight of 2^0 . Similarly, data of weight of 2^{i-1} is added by i-th adder ADD 4, i, and data of the maximum weight of $2^{(2s-1)-1}$ is added by adder ADD 4, (2s - 1). Here, n ANDs A1, 1 to A1 n are added by ADD 4, 1, n(s-s-i) data is added by i-th adder ADD 4, i, and n data is added by ADD 4, (2s-1).

[0015] The outputs of adders ADD 4, 1 to ADD 4, (2s-1) are connected to capacitances C4, 1 to C4, (2s-1), respectively. The outputs of these capacitances are combined with each other and connected to an inverting input of an operational amplifier AMP 4. These capacitances are set to the capacities corresponding to bit weights of input data, and then the appropriate sum can be obtained at a final output Vo4. The inverting input and output of the operational amplifier AMP 4 are connected to each other through a switch SW 41, and further a capacitance C4F is connected to the inverting input at its one terminal. The other terminal of C4F is connected to a switch SW 42 by which connection to the output of AMP 4 or to the non-inverting input thereof is switched.

[0016] A refresh signal REF is fed to adders ADD 4, 1 to ADD, (2s-1) and switches SW 41, SW 42. When the refresh signal is in a high-level, the adders are refreshed, the switch SW 41 is closed to refresh capacitances and switch SW 42 is closed to connect to the non-inverting input. In a normal operational state, SW 41 is opened and SW 42 is connected to the output of the operational amplifier. At this time, suppose that the outputs of adders ADD 4, 1 to ADD 4, (2s-1) are expressed by V(A4, 1) to V(A4, (2s-1)), the output Vo4 of AMP 4 is given by equation (1). where Vref is a reference voltage to be input to AMP 4.

$$Vo4 - V_{ref} = - \frac{\sum_{j=1}^{2s-1} V(A4, j) \cdot C4, j - V_{ref} \left(\sum_{j=1}^{2s-1} C4, j \right)}{C4F} \quad (Eq.1)$$

From equation (1), it is shown that Vo4 represents the sum of inputs.

[0017] In addition, when the refresh signal is set to a high-level, Vref is output from the adders ADD 4, 1 to ADD 4, (2s-1), and then Vref is also input to the output side of C4F. In this state, charges of all capacitances are reset.

[0018] FIG. 5 shows a configuration of the adder ADD 4, 1 with an odd number of taps. The adder ADD 4, 1 has a multiplexer MUX 51 to which A1, 1 is input, and (n-1)/2 selectors SEL 5, 1 to SEL 5, (n-1)/2 to which two data, that is, (A1, 2, A1, 3), ..., (A1, n-1, A1, n) is input, respectively. A first reference voltage VH and a second reference voltage VL are input to the multiplexer 51, and the outputs therefrom are input to a second multiplexer MUX 52. A third reference voltage Vref is input to the multiplexer MUX 52. While, these first to third reference voltages VH, VL, Vref are input to the selectors SEL5, 1 to SEL5, (n-1)/2. The multiplexer MUX 51 outputs VH when A1, 1 is in a high-level and VL in a low-level. In addition, the respective selectors generate outputs as shown in the following Table 1 by the combinations of inputs.

Table 1

Output of the selector SEL5, 1		
A 1, 2	A 1, 3	output
low level	low level	V L
high level	low level	V r e f
low level	high level	V r e f
high level	high level	V H

[0019] Thus, converting the sum of two ANDs to ternary data by the selector achieves a decrease in the number of data in the latter processing. As a result, this makes it possible to reduce circuit scale and power consumption. Further, the AND calculation is performed in digital, and the conversion to binary and ternary form thereof are made based on the reference voltages. This allows the high accuracy of operation to be insured. The reason why the multiplexer MUX 51 is provided is that the number of taps is an odd number, and that one residue of two inputs allocated to each selector should be handled. If the number of taps is an even number, the multiplexer MUX 51 can be omitted.

[0020] The outputs of the multiplexer MUX 52 and selectors SEL 5, 1 to SEL 5, (n-1)/2 are connected to the capacitances C51 to C5, ((n-1)/2+1), respectively, and the outputs of these capacitances are combined with each other and connected to an inverting input of an operational amplifier AMP 5. A capacity ratio among these capacitances is equal to each other. The inverting input of the operational amplifier AMP 5 and the output are connected to each other through a switch SW 51, and a capacitance C5F is connected to the inverting input at its one terminal. The other terminal of C5F is connected to a switch SW52 by which connection to the output of AMP 5 or to the non-inverting input thereof is switched. Moreover, the third reference voltage is input to the second multiplexer MUX 52. The refresh signal REF is input to SEL 5, 1 to SEL 5, (n-1)/2 and MUX 52. When the refresh signal is in a high level, the multiplexer and selector output Vref, so that the switch SW 51 is closed and SW 52 is connected to the non-inverting input.

[0021] In the normal operation state, MUX 52 outputs the output of MUX 51 directly to open 51, and to connect SW 52 to the output of the operational amplifier. At this time, suppose that the outputs of MUX 51, SEL 5, 1 to SEL 5, (n-1)/2 are expressed by V(M51) and V(S51) to V(S5, (n-1)/2), the output Vo5 of AMP 5 can be given by equation (2).

$$Vo5 - V_{ref} = \frac{V(M51) \cdot C5,1 + \sum_{j=2}^{\frac{n-1}{2}+1} V(S5, j-1) \cdot C5, j - V_{ref} \left(\sum_{j=1}^{\frac{n-1}{2}+1} C5, j + 1 \right)}{C5F} \quad (Eq.2)$$

[0022] From equation (2), it is shown that Vo5 represents the sum of inputs.

[0023] In addition, when the refresh signal is set to the high-level, the multiplexer and selector output Vref, and Vref is also input to the output side of C5F. In this state, charges of all capacitances are reset.

[0024] FIG. 6 shows the configuration of selector SEL5, 1. The selector 5, 1 has three gate circuits GH, GL, Gref arranged in parallel, and inputs A1, 2, and A1, 3 are input to these gate circuits in parallel. GH is an AND circuit, GL is a NOR circuit, and Gref is an EX-OR circuit. Outputs of these gate circuits GH, GL, Gref are input to switches SWH, SWL, SWREF, respectively, and these switches are connected to VH, VL, Vref, respectively. When both inputs are in a high level, the output of GH becomes high level, and VH is output by closing SWH. When one input is in a high level and the other input is in a low level, the output of Gref becomes high level and Vref is output by closing SWREF. When both inputs are in a low level, the output of GL becomes high level and VL is output by closing SWL. In other words, the output characteristic shown in Table 1 can be obtained by the configuration of FIG. 6. Other selectors SEL 52 to SEL 5, (n-1)/2 have the same configuration as mentioned above, and therefore the explanation thereof is omitted.

[0025] Thus, the multiplication of filter operation is performed by the digital AND operation and the analog addition. As a result, this makes it possible reduce circuit scale and power consumption while holding the operational accuracy high.

[0026] FIGS. 7 and 8 show an adder TADD of the filter circuits according to the second embodiment, and an ADD 7, 1 (corresponding to ADD 4,1 of FIG. 4) constituting the adder TADD, respectively.

[0027] In FIG. 7, the adder circuit TADD comprises a plurality (2s-1) of adders (ADD 7,1 to ADD7, (2s-1)), among which ADD 7, 1 calculates the sum of the ANDS of the least significant bits of data dijk (k = 1 to n) and those of multiplier mk (k = 1 to n). In this embodiment, resistances R71 to R7, (2s-1) are substituted for the capacitances C4, 1 to C4, (2s-1) of FIG. 4, and resistance R7F is substituted for C4F. This eliminates the need for executing the aforementioned refresh operation since no problem occurs on the residues of the charges of capacitances. Here, setting the input voltage in the same way as FIG. 4, an output voltage Vo7 of adder TADD can be expressed by equation (3).

$$Vo7 = \frac{\sum_{j=1}^{2s-1} \frac{V(A7, j) - Vref}{R7j}}{\frac{1}{R7F}} + Vref \quad (Eq.3)$$

[0028] In FIG. 8, ADD 7, 1 comprises a multiplexer MUX 81 to which A1, 1 is input, and (n-1)/2 selectors SEL8, 1 to SEL, (n-1)/2 to which other two data (A1, 2; A1, 3) ... (A1, n-1; A1, n) are input, respectively. The first reference voltage VH and the second reference voltage VL are input to the multiplexer MUX 81. While, these first to third reference voltages VH, VL, Vref are input to the selectors SEL 8, 1 to SEL 8, (n-1)/2. The multiplexer MUX 81 outputs VH when A1, 1 is in a high level, and VL in a low level. In addition, each selector generates the same output as shown in Table 1.

[0029] In this embodiment, resistances R81 to R8, (n-1) are substituted for the capacitances C51 to C5, (n-1)/2+1 of FIG. 5, and resistance R8F is substituted for C5F. This eliminates the need for executing the aforementioned refresh operation since no problem occurs on the residues of the charges of capacitances. Here, setting the input voltage in the same way as FIG. 5, an output voltage Vo8 of adder ADD 7, 1 can be expressed by equation (4).

$$Vo8 = \frac{\frac{V(M81) - Vref}{R81} + \sum_{j=2}^{\frac{n-1}{2}+1} \frac{V(s8, j-1) - Vref}{R8, j}}{\frac{1}{R8F}} \quad (Eq.4)$$

[0030] Thus, converting the sum of two ANDs to ternary data by the selector achieves a decrease in the number of data in the latter processing. As a result, this makes it possible to reduce circuit scale and power consumption. In addition, the AND calculation is performed in digital, and the conversion to binary and ternary form thereof are made based on the reference voltages. This allows the high accuracy of operation to be insured. The reason why the multiplexer MUX 81 is provided is that the number of taps is an odd number, and that one residue of two inputs allocated to each selector should be handled. If the number of taps is an even number, the multiplexer MUX 81 can be omitted.

[0031] The functions of the respective taps and those of the adders, employed in the filter circuits, are available as a normal multiplier.

[0032] FIG. 9 shows an example of multiplication of digital data, which is composed of 3 bits of a0 to a2, and digital data, which is composed of 3 bits of b0 to b2, in the multiplier corresponding to the aforementioned capacitance type filter (FIGS. 4, 5). In FIG. 9, there are provided AND circuits G91 to G99, which calculate ANDs of combinations of the respective bits of digital data, (a0, b0), (a1, b0), (a0, b1), (a2, b0), (a1, b1), (a0, b2), (a2, b1), (a1, b2), and (a2, b2), respectively. The output of AND circuit G91 is input to a multiplexer 91, and the outputs of AND circuits G92 and G93 are input to a selector SEL 91. Moreover, the output of AND circuit G94 is input to a multiplexer 92, and the outputs of AND circuits G95 and G96 are input to a selector SEL 92. Furthermore, the outputs of AND circuits G97 and G98 are input to a selector SEL 93, and the output of AND circuit 99 is input to a multiplexer 93. The outputs of MUX 91, SEL 91, MUX 92, SEL 92, SEL 93 and MUX 93 are connected to capacitances C 91 to C 96, respectively. The outputs of these capacitances are combined, and input to the inverting input of an operational amplifier AMP 9. These capacitances equal the capacities, which are proportional to the sum of the weights of the input bits of the respective ANDs. Upon calculation of the sum thereof, the multiplication result can be obtained. Here, the capacity ratio of capacitances C91 to C96 is shown in Table 2.

Table 2

Capacity ratio of capacitances of AND circuit					
C 9 1	C 9 2	C 9 3	C 9 4	C 9 5	C 9 6
2 ⁰	2 ¹	2 ²	2 ²	2 ³	2 ⁴

[0033] The inverting input of the operational amplifier AMP 9 and the output are connected to each other through a switch SW 91, and a capacitance C9F is connected to the inverting input at its one terminal. The other terminal of C9F is connected to a switch SW 92 by which connection to the output of AMP9 or to the non-inverting input thereof is switched

[0034] A refresh signal REF is input to MUX 91 to MUX 93, SEL 91 to SEL 93, and switches SW 91 and SW 92. When the refresh signal is in a high level, all Vref signals are output and the switch SW 91 is closed, and SW 92 is connected to the non-inverting input in order to refresh the capacitance. In the normal operational state, SW 91 is opened, and SW 92 is connected to the output of the operational amplifier.

[0035] As for the above multiplier, the multiplication result can be given by equation (5) using the above-mentioned bits in the same way as the equation (2). In this case, suppose that the outputs of MUX 91 to MUX 93, SEL 91 to SEL 93 are V(M91) to V(M93), and V(S91) to V(S93), respectively.

$$V_{O9} - V_{ref} = - \frac{(V(M91) - V_{ref})C91 + (V(M92) - V_{ref})C93 + (V(M93) - V_{ref})C96}{CF9} - \frac{(V(s91) - V_{ref})C92 + (V(s92) - V_{ref})C94 + (V(s93) - V_{ref})C95}{CF9} \quad (Eq.5)$$

[0036] Fig. 10 shows an example of multiplication of digital data, which is composed of 3 bits of a0 to a2, and digital data, which is composed of 3 bits of b0 to b2, in the multiplier corresponding to the aforementioned resistance type filter (FIGS. 7, 8). In FIG. 10, similar to FIG. 9, AND circuits G 101 to G 109, multiplexers MUX 101 to MUX 103, selectors SEL 101 to SEL 103 are used. The outputs of MUX 101, SEL 101, MUX 102, SEL 102, SEL 103, and MUX 103 are connected to resistances R 101 to R 106, respectively. The outputs of these resistances are combined and input to the inverting input of an operational amplifier AMP 10. These resistances are the resistance values, which are indirectly proportional to the sum of the weights of the input bits of the respective ANDs. Upon calculation of the sum thereof, the multiplication result can be obtained. Here, the resistance value ratio of resistances R 101 to R106 is shown in Table 3.

Table 3

Resistance value ratio of resistances of AND circuit					
R101	R102	R103	R104	R105	R106
$\frac{1}{2^0}$	$\frac{1}{2^1}$	$\frac{1}{2^2}$	$\frac{1}{2^2}$	$\frac{1}{2^3}$	$\frac{1}{2^4}$

[0037] The use of the above multiplier, the multiplication result can be obtained by equation (6). In this case, suppose that the outputs of MUX 101 to MUX 103, SEL 101 to SEL 103 are V(M101) to V(M103), and V(S101) to V(S103), respectively.

$$V_{o10} - V_{ref} = - \frac{\frac{V(M101) - V_{ref}}{R101} + \frac{V(M102) - V_{ref}}{R103} + \frac{V(M103) - V_{ref}}{R106}}{\frac{1}{R10F}} - \frac{\frac{V(s101) - V_{ref}}{R102} + \frac{V(s102) - V_{ref}}{R104} + \frac{V(s103) - V_{ref}}{R105}}{\frac{1}{R10F}} \quad (Eq.6)$$

[0038] Further, it is possible to apply the multipliers MUL 9 and MUL 10 of FIGS. 9 and 10 to the configuration of the ordinary FIR (Finite Impulse Response) filter (FIG. 2), and to generate the multiplication outputs (analog signals) of the respective taps by the analog adder.

[0039] As mentioned above, the multiplier according to the present invention calculates ANDs of all combinations of the bits of first digital data and the bits of second digital data. Weighted addition is performed by use of a plurality of capacitances each having capacity, which is proportional to the sum of weights of a pair of bits corresponding to each AND circuit, or resistances each having a resistance value, which is indirectly proportional to the weight, an amplifier wherein outputs of these capacitance or resistances are combined and connected thereto, and a feedback capacitance or resistance, which is connected to a negative feedback of the amplifier. A multiplication result is output as an analog voltage. Therefore, the present invention can provide multipliers and filter circuits, which are small scale, and low power consumption as well as suitable for digital multiplication operation.

Claims

1. A multiplier comprising:

- a plurality of AND circuits for generating ANDs of all combinations of the respective bits of first digital data and the respective bits of second digital data;
- a plurality of capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to each AND circuit;
- an amplifier to which outputs of these capacitances are combined and connected;
- a feedback capacitance, which is connected to the amplifier to form a negative feedback circuit.

2. A multiplier wherein a multiplexer with two inputs and one output is controlled by an AND of the most significant digits of first digital data and second digital data and an AND of the least significant digits thereof, respectively, one or a plurality of selectors with three inputs and one output and one or zero multiplexer with two inputs and one output are controlled by an AND wherein the sum of weights of corresponding pair of bits is equal with respect to other ANDs, a first reference voltage, a second reference voltage, and a third reference voltage are input to said selector, the first reference voltage and second reference voltage are input to said multiplexer, capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said multiplexer, capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said selector, outputs of these capacitances are combined and connected to the amplifier, and a feedback capacitance is connected to the amplifier to form a negative feedback circuit.

3. A multiplier comprising:

- a plurality of AND circuits for generating ANDs of all combinations of the respective bits of first digital data and the respective bits of second digital data;
- a plurality of resistances each having a resistance value, which is indirectly proportional to the sum of weights of bits corresponding to each AND circuit;
- an inverting amplifier to which outputs of these resistances are combined and connected;
- a feedback resistance, which is connected to the amplifier to form a negative feedback circuit.

4. A multiplier wherein a multiplexer with two inputs and one output is controlled by an AND of the most significant digits of first digital data and second digital data and an AND of the least significant digits thereof, respectively, one or a plurality of selectors with three inputs and one output and one or zero multiplexer with two inputs and one

output are controlled by an AND wherein the sum of weights of corresponding pair of bits is equal with respect to other ANDs, a first reference voltage, a second reference voltage, and a third reference voltage are input to said selector, the first reference voltage and second reference voltage are input to said multiplexer, resistances each having a resistance value, which is indirectly proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said multiplexer, resistances each having a resistance value, which is indirectly proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said selector, outputs of these resistances are combined and connected to the amplifier, and a feedback resistance is connected to the amplifier to form a negative feedback circuit.

5. A filter circuit for calculating the sum of products of a plurality of time series digital data and digital multipliers corresponding to these digital data, said filter circuit comprising:

a plurality of AND circuits for calculating ANDs of all combinations of the respective bits of the respective digital data and the respective bits of corresponding digital multipliers;

a plurality of combining circuits for combining corresponding bits of outputs in these AND circuits to generate analog outputs; and

an adder for adding the outputs of these combining circuits in analog;

wherein when the number of inputs of said combining circuit is even, one or a plurality of selectors with three inputs and one output is controlled by two inputs, a first reference voltage, a second reference voltage, and a third reference voltage are input to these selectors, and when the number of inputs of said combining circuit is odd, one multiplexer with two inputs and one output is controlled by one input, one or a plurality of selectors with three inputs and one output is controlled by two inputs, said first reference voltage, second reference voltage, and third reference voltage are input to these selectors, and capacitances each having an equal capacity are connected to the output of said multiplexer and that of said selector; and

said adder has a plurality of capacitances each having a capacity, which is proportional to weights of the outputs of the respective combining circuits, the outputs of these capacitances are combined and connected to an amplifier, and a feedback capacitance is connected to the amplifier to form a negative feedback circuit.

6. A filter circuit for calculating the sum of products of a plurality of time series digital data and digital multipliers corresponding to these digital data, said filter circuit comprising:

a plurality of AND circuits for calculating ANDs of all combinations of the respective bits of the respective digital data and the respective bits of corresponding digital multipliers;

a plurality of combining circuits for combining corresponding bits of outputs in these AND circuits to generate analog outputs; and

an adder for adding the outputs of these combining circuits in analog;

wherein when the number of inputs of said combining circuit is even, one or a plurality of selectors with three inputs and one output is controlled by two inputs, a first reference voltage, a second reference voltage, and a third reference voltage are input to these selectors, and when the number of inputs of said combining circuit is odd, one multiplexer with two inputs and one output is controlled by one input, one or a plurality of selectors with three inputs and one output is controlled by two inputs, said first reference voltage, second reference voltage, and third reference voltage are input to these selectors, and resistances each having an equal resistance value are connected to the output of said multiplexer and that of said selector; and

said adder has a plurality of resistances each having a resistance value, which is indirectly proportional to weights of the outputs of the respective combining circuits, the outputs of these resistances are combined and connected to an amplifier, and a feedback resistance is connected to the amplifier to form a negative feedback circuit.

7. A filter circuit for calculating the sum total of products of a plurality of time series digital data and digital multipliers corresponding to these digital data, said filter circuit comprising:

a plurality of AND circuits for calculating ANDs of all combinations of the respective bits of the respective digital data and the respective bits of corresponding digital multipliers;

a plurality of combining circuits for combining corresponding bits of outputs in these AND circuits to generate analog outputs; and

an adder for adding the outputs of these combining circuits in analog;

wherein a multiplexer with two inputs and one output is controlled by an AND of the most significant

digits of first digital data and second digital data and an AND of the least significant digits thereof, respectively, one or a plurality of selectors with three inputs and one output and one or zero multiplexer with two inputs and one output are controlled by an AND wherein the sum of weights of corresponding pair of bits is equal with respect to other ANDs, a first reference voltage, a second reference voltage, and a third reference voltage are input to said selector, the first reference voltage and second reference voltage are input to said multiplexer, capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said multiplexer, capacitances each having a capacity, which is proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said selectors, outputs of these capacitances are combined and connected to the amplifier, and a feedback capacitance is connected to the amplifier to form a negative feedback circuit; and said adder connects the capacitances each having an equal capacity to the outputs of the respective combining circuits, said adder combines and connects the outputs of these capacitances to the amplifier, and said adder connects a feedback capacitance to the amplifier to form a negative feedback circuit.

8. A filter circuit for calculating the sum of products of a plurality of time series digital data and digital multipliers corresponding to these digital data, said filter circuit comprising:

a plurality of AND circuits for calculating ANDs of all combinations of the respective bits of the respective digital data and the respective bits of corresponding digital multipliers;
 a plurality of combining circuits for combining corresponding bits of outputs in these AND circuits to generate analog outputs; and
 an adder for adding the outputs of these combining circuits in analog;
 wherein a multiplexer with two inputs and one output is controlled by an AND of the most significant digits of first digital data and second digital data and an AND of the least significant digits thereof, respectively, one or a plurality of selectors with three inputs and one output and one or zero multiplexer with two inputs and one output are controlled by an AND wherein the sum of weights of corresponding pair of bits is equal with respect to other ANDs, a first reference voltage, a second reference voltage, and a third reference voltage are input to said selector, the first reference voltage and second reference voltage are input to said multiplexer, resistances each having a resistance value, which is indirectly proportional to the sum of weights of a pair of bits corresponding, to an input of an AND corresponding to a control signal, are connected to the output of said multiplexer, resistances each having a resistance value, which is indirectly proportional to the sum of weights of a pair of bits corresponding to an input of an AND corresponding to a control signal, are connected to the output of said selectors, outputs of these resistances are combined and connected to the amplifier, and a feedback capacitance is connected to the amplifier to form a negative feedback circuit; and said adder connects the resistances each having an equal resistance value to the outputs of the respective combining circuits, said adder combines and connects the outputs of these resistances to the amplifier, and said adder connects a feedback capacitance to the amplifier to form a negative feedback circuit.

9. The multiplier according to claim 1, wherein said selector has a NOR gate, an AND gate, and an EX-OR gate to which two ANDs are input in common, the first reference voltage is generated by an output of said AND gate, the second reference voltage is generated by an output of said NOR gate, and the third reference voltage is generated by an output of said EX-OR gate.

FIG. 1

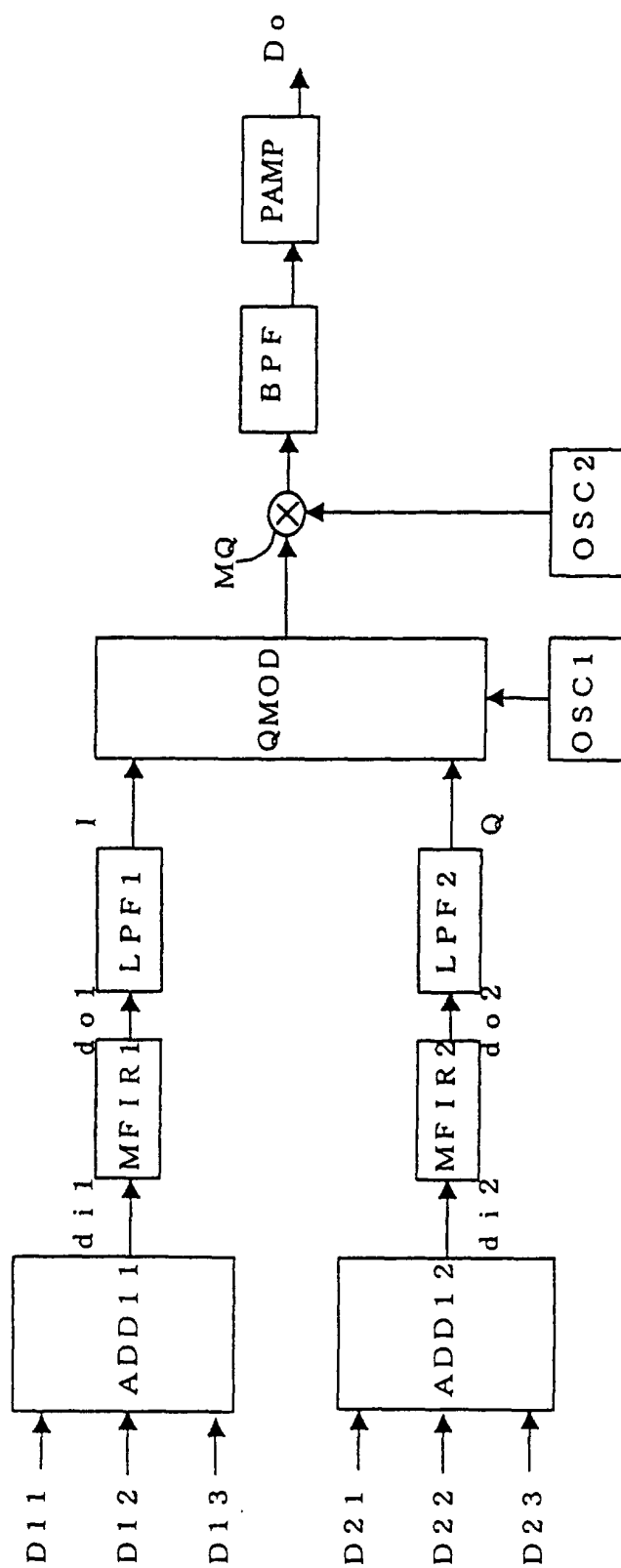


FIG.2

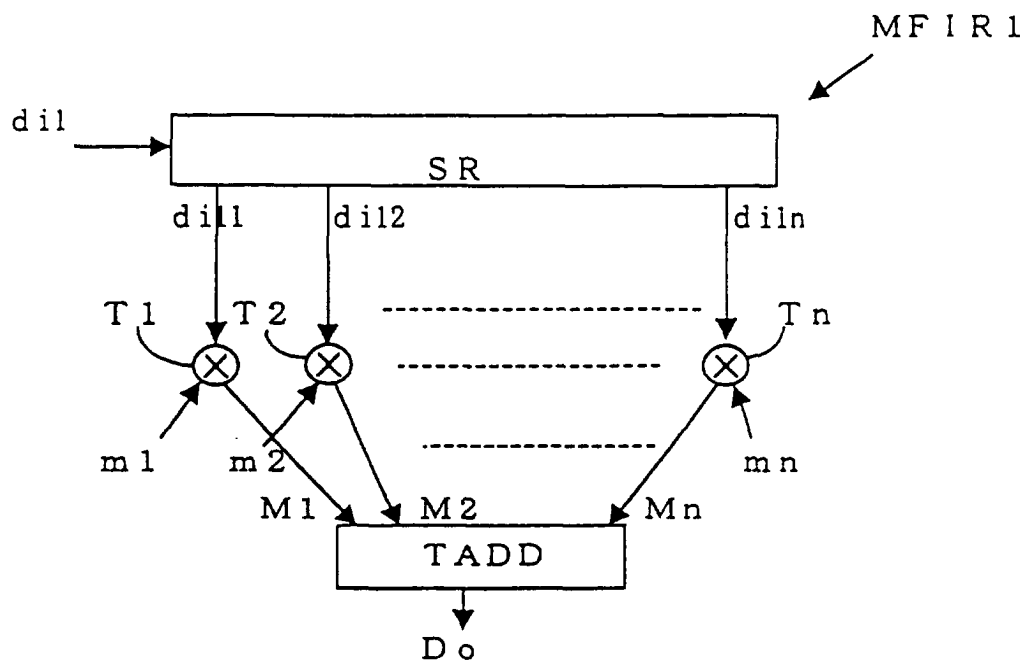


FIG.3

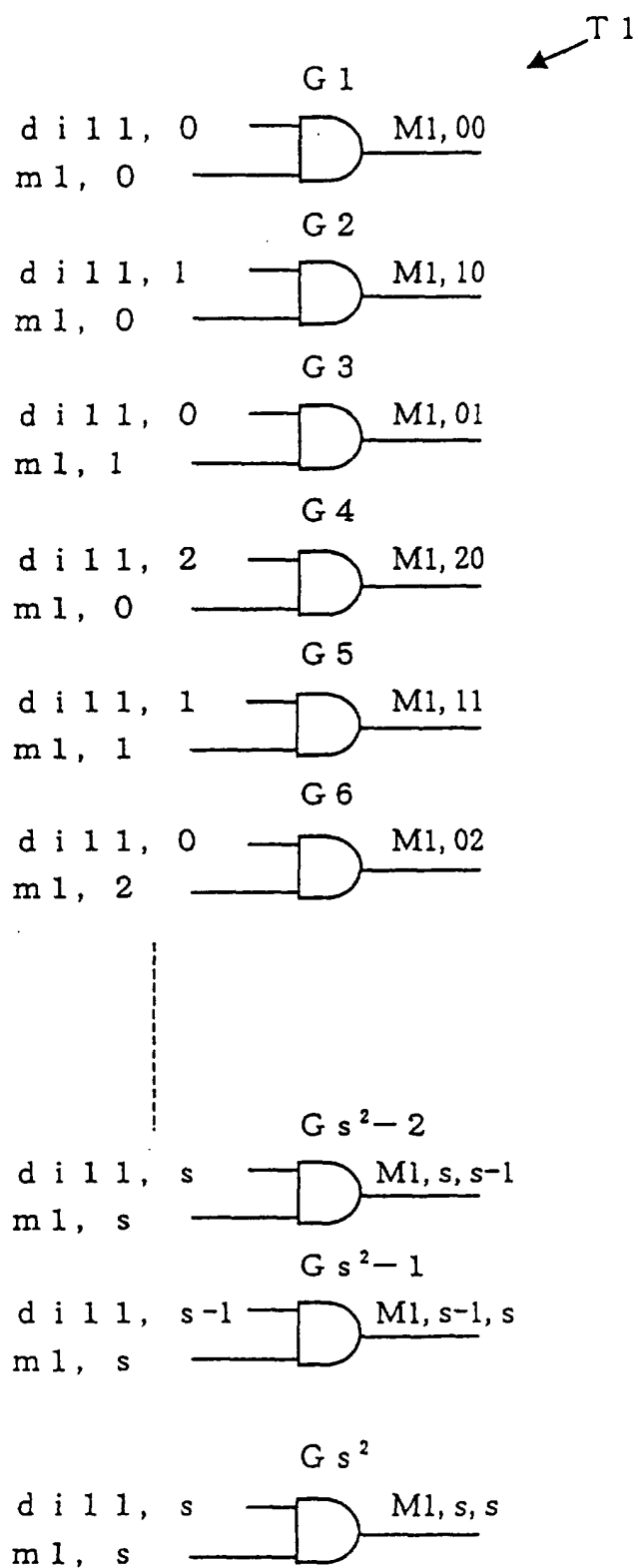


FIG.4

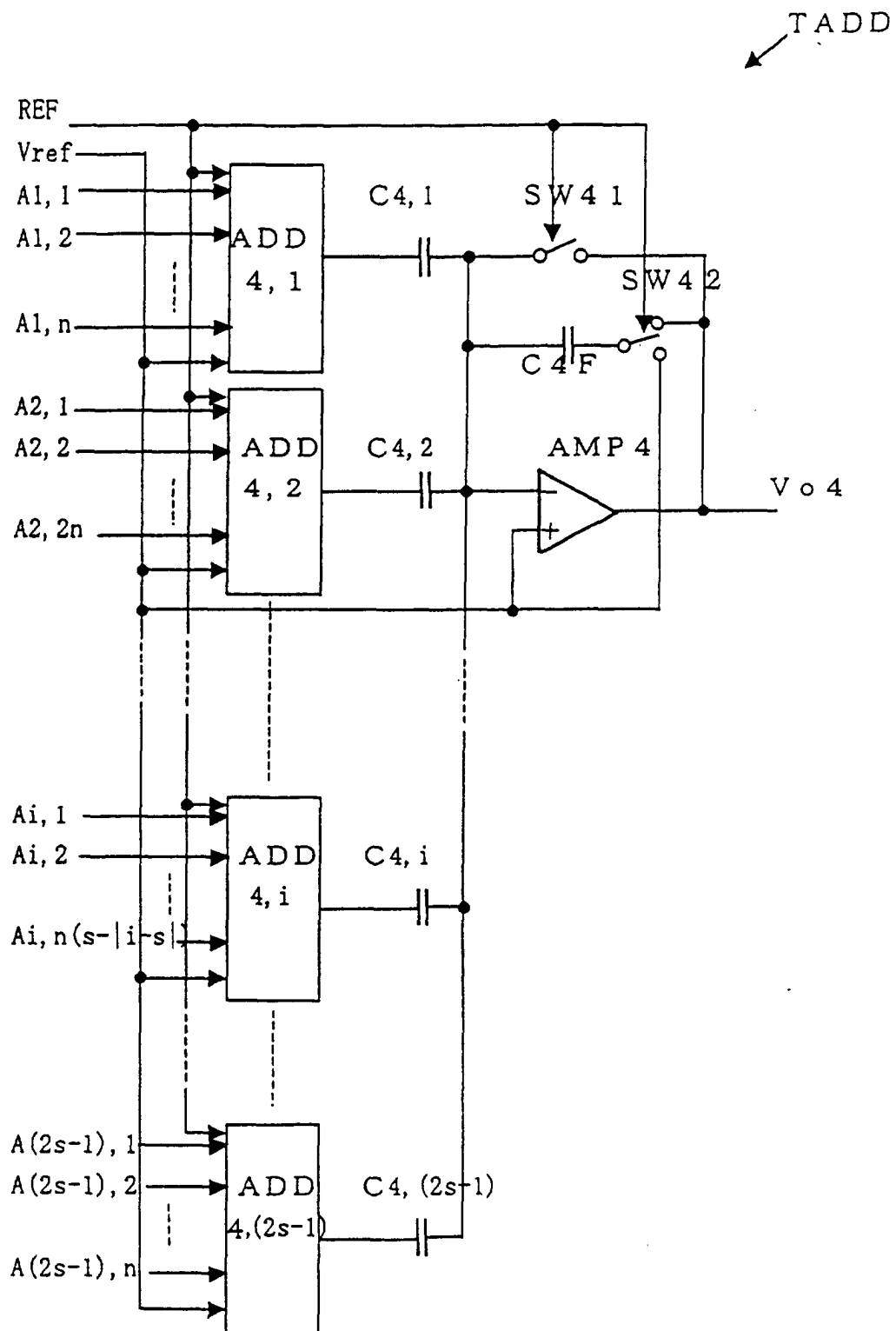


FIG.5

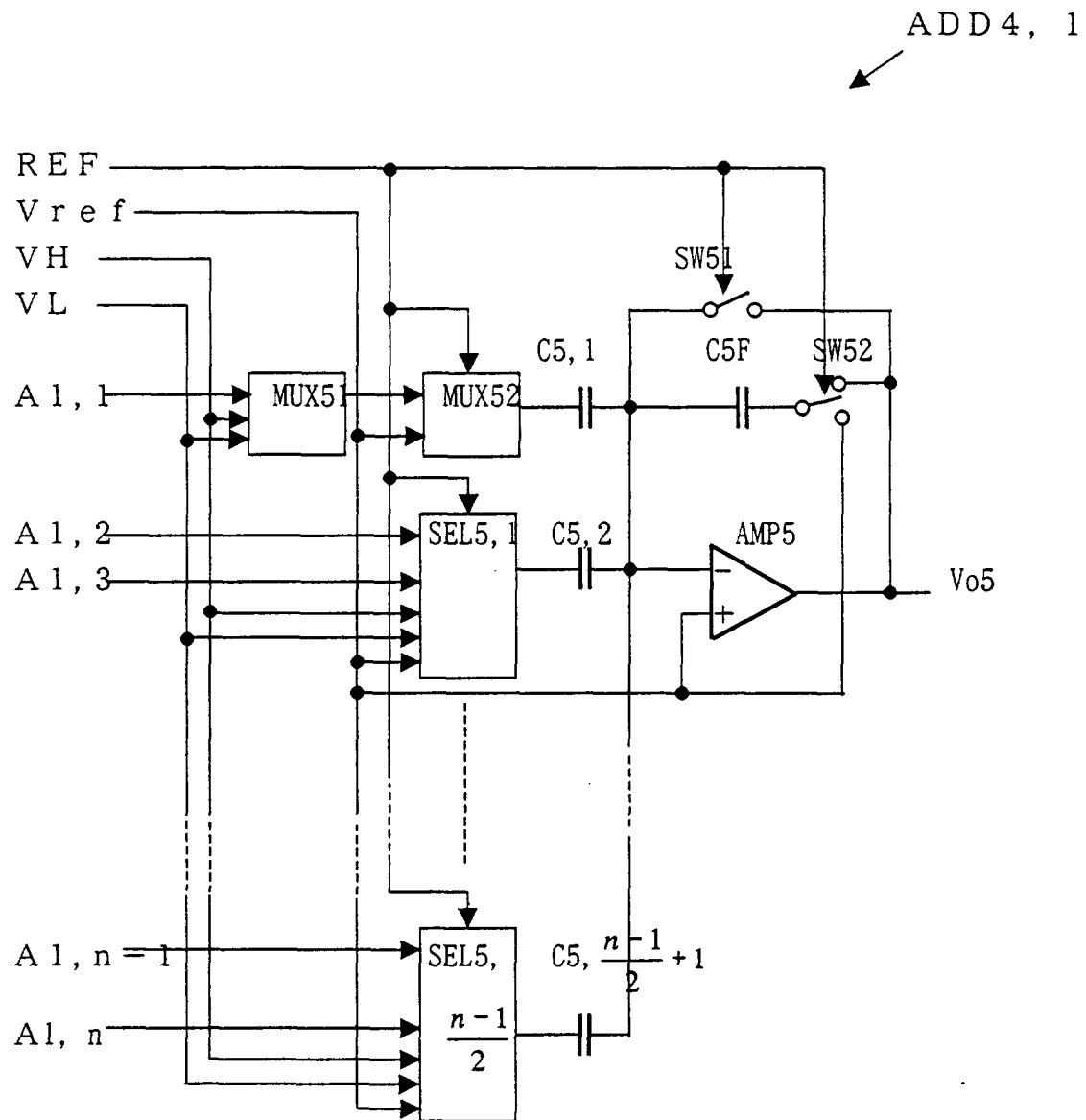


FIG.6

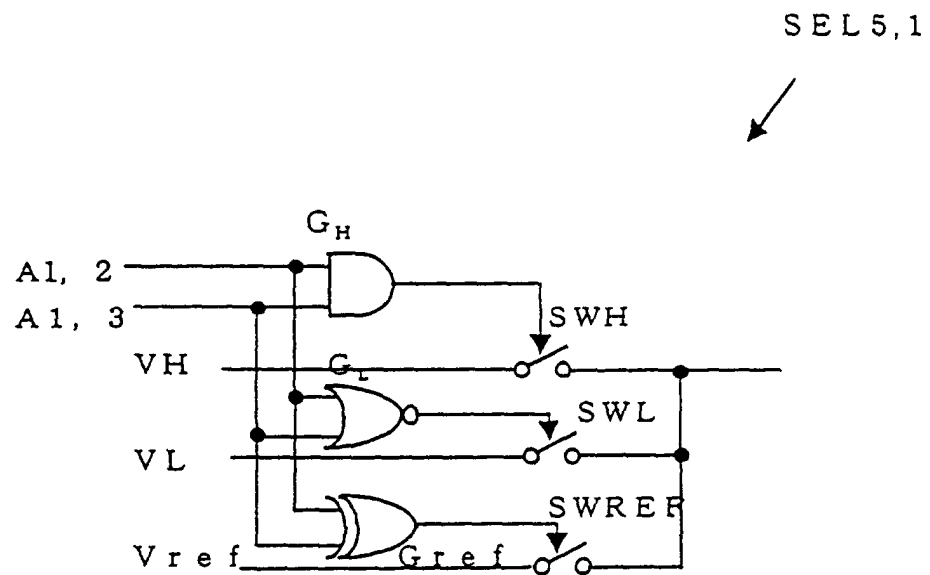


FIG.7

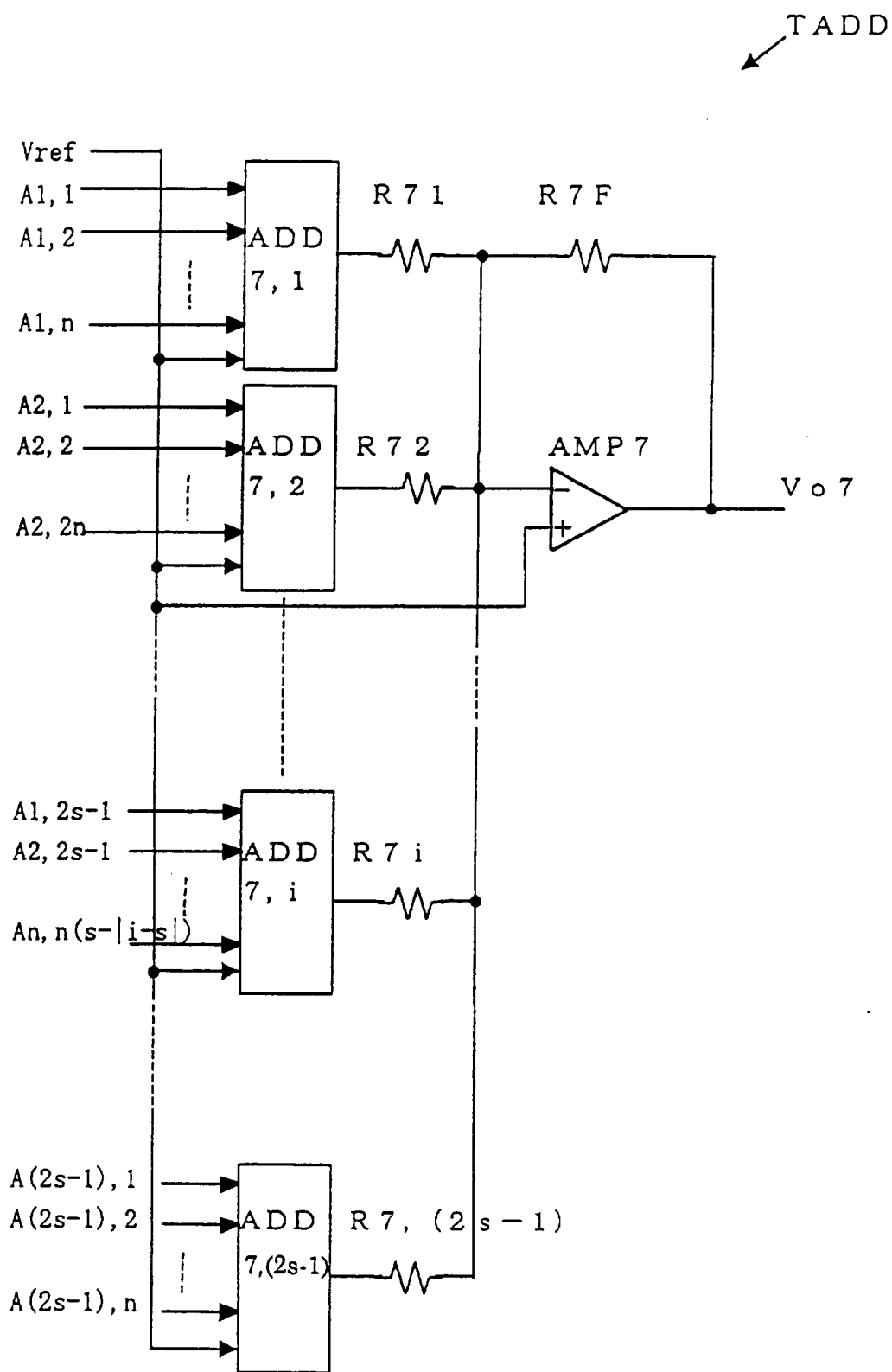


FIG.8

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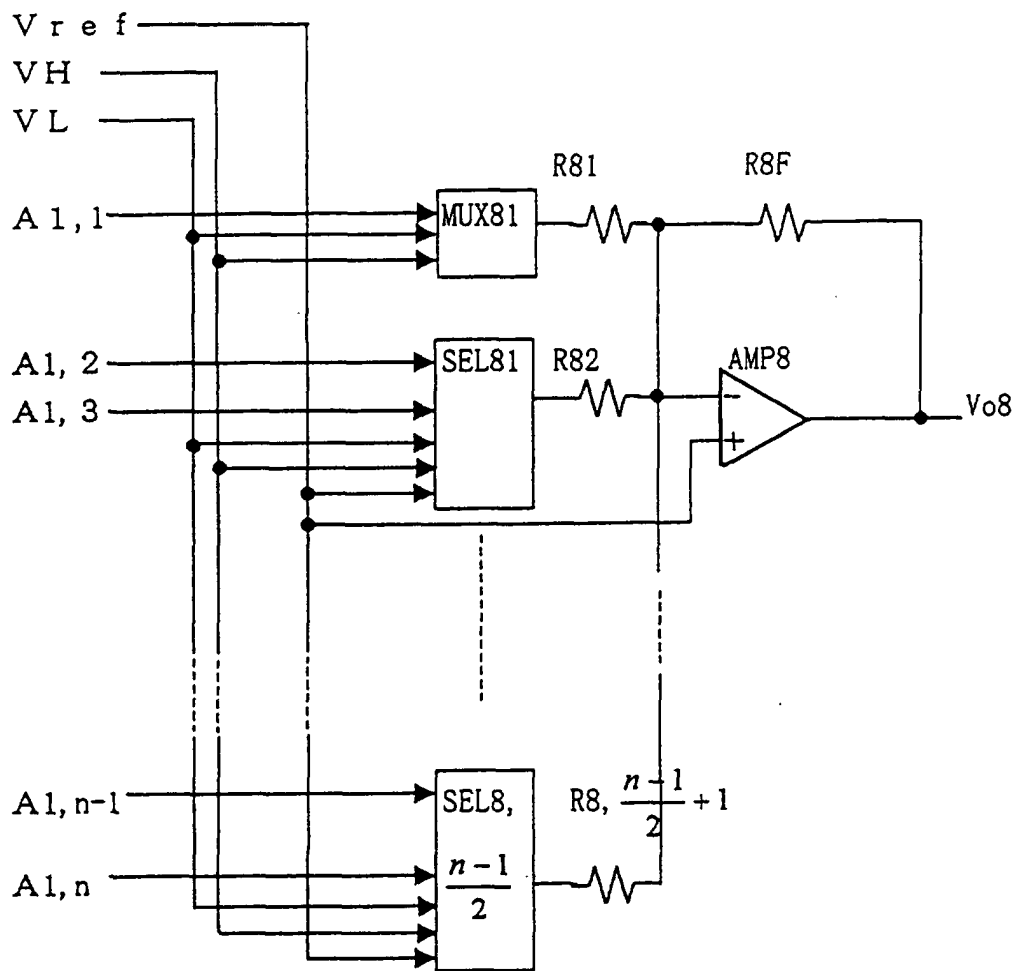


FIG.9

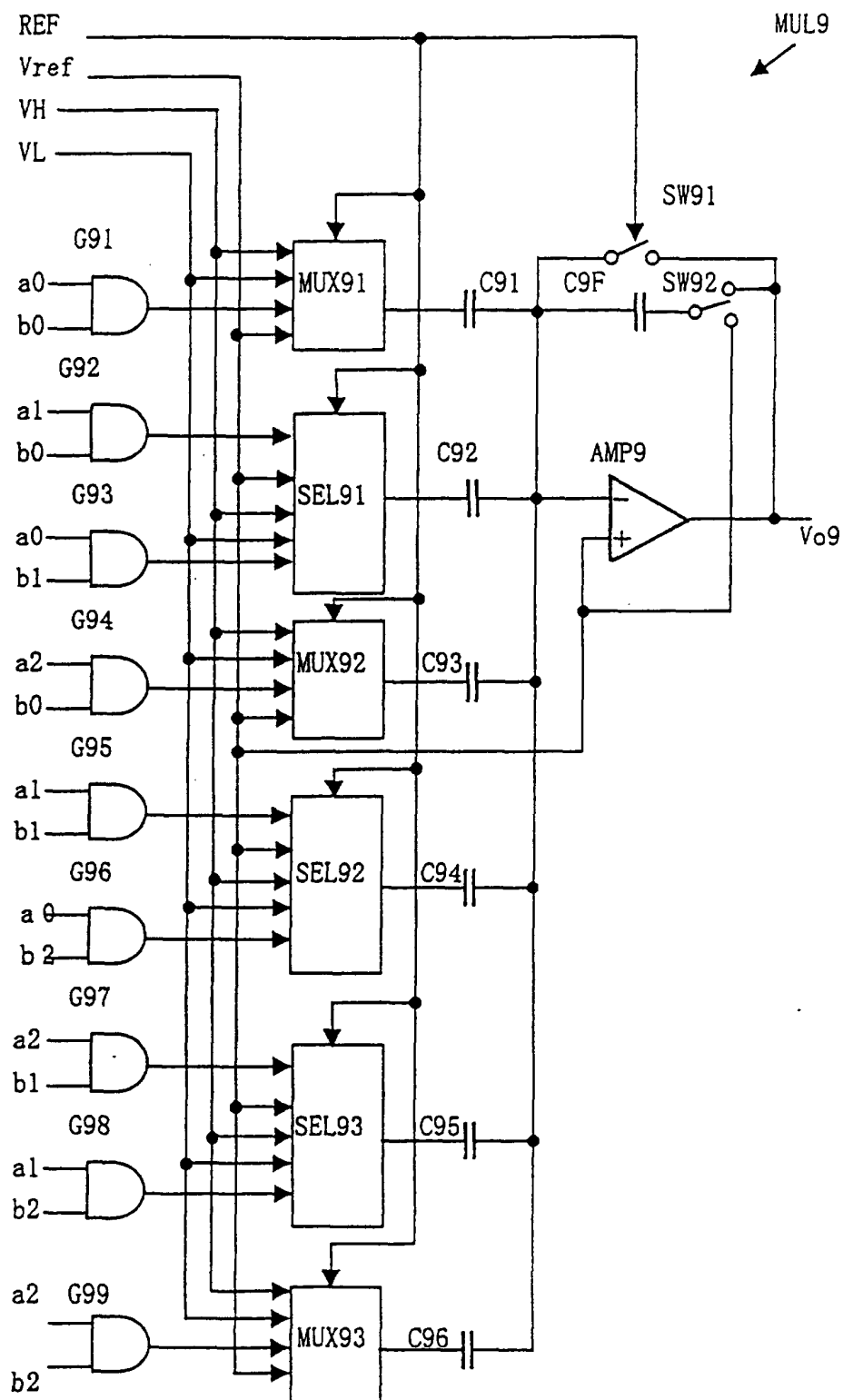
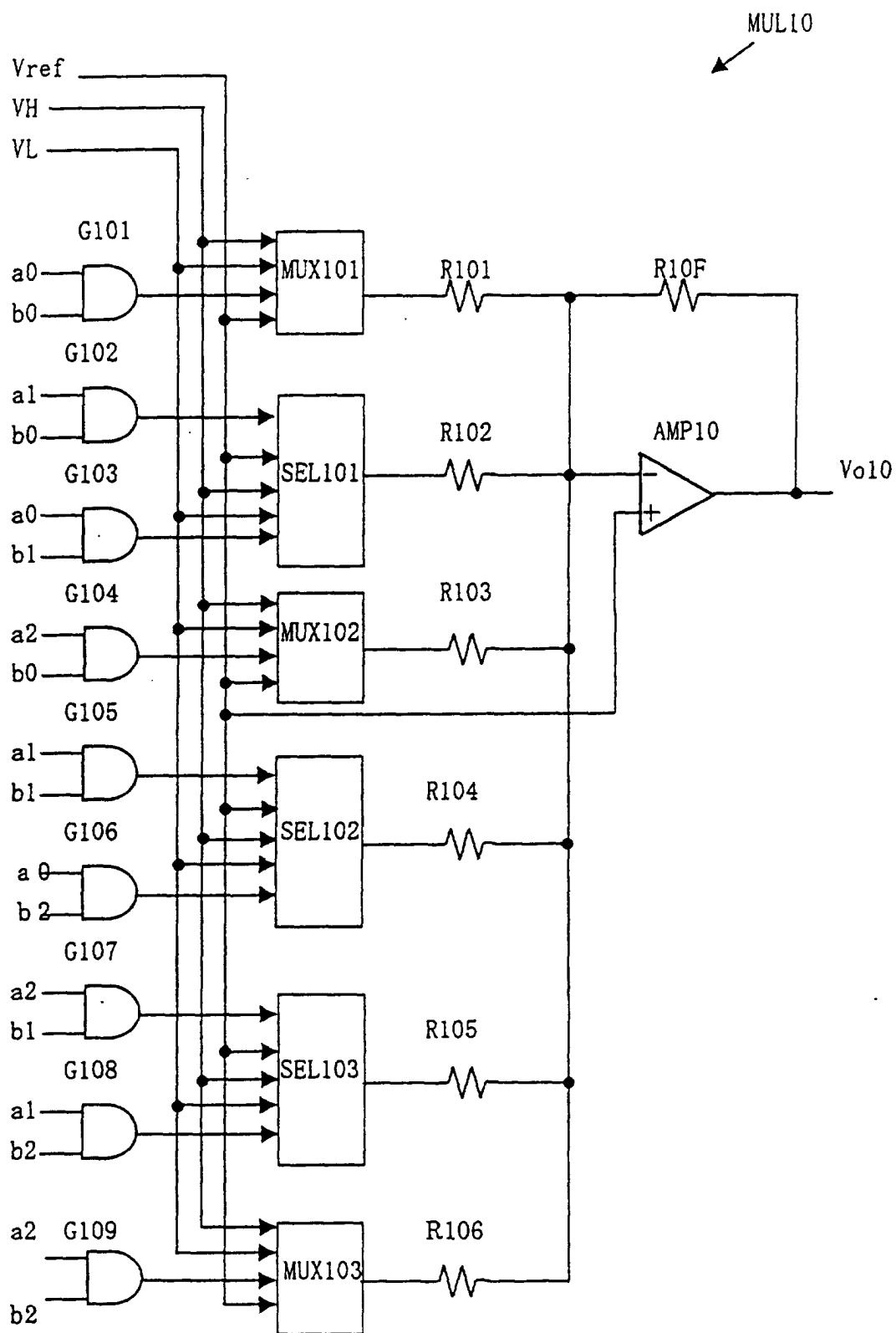


FIG.10





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EUROPEAN SEARCH REPORT

Application Number
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Place of search THE HAGUE		Date of completion of the search 14 November 2000	Examiner Beindorff, W
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