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(71) Applicant: **Thomson Licensing S.A.**
92100 Boulogne-Billancourt (FR)

(72) Inventors:
- **Ipek, Mehmet**
  78050 Villingen-Schwenningen (DE)
- **Rieger, Martin**
  78628 Rottweil (DE)
- **Schemmann, Heinrich**
  78052 Villingen-Schwenningen (DE)

(74) Representative: **Rossmanith, Manfred, Dr. et al**
Deutsche Thomson-Brandt GmbH European Patent Operations Karl-Wiechert-Allee 74
30625 Hannover (DE)

(54) High frequency oscillator

(57) A fully integrated 6 GHz oscillator is presented which is suitable for wireless networks in the available frequency bands between 5 GHz and 6 GHz. The high frequency oscillator comprises a reference oscillator (6), a phase-locked loop circuit with a phase frequency detector (1), a charge pump (2), a ring oscillator (4) and a divider (5), the reference oscillator (6) being coupled to the phase frequency detector (1) for frequency control. The ring oscillator (4) is a symmetrical delay cell oscillator containing two amplifiers with a dual output stage for providing I/Q output signal generation. The reference oscillator (6) works in the range of 1,25 - 1,5 GHz and is a Colpitts type digital controlled frequency synthesizer with an external tank circuit (7) for providing a low phase noise, and the dividing factor of the divider (5) is four for providing a tuned output range of 5 to 6 GHz. The phase-locked loop circuit is integrated together with the reference oscillator into an integrated circuit, using advantageously a BICMOS Silicon/Germanium process, which is well suited for RF applications.

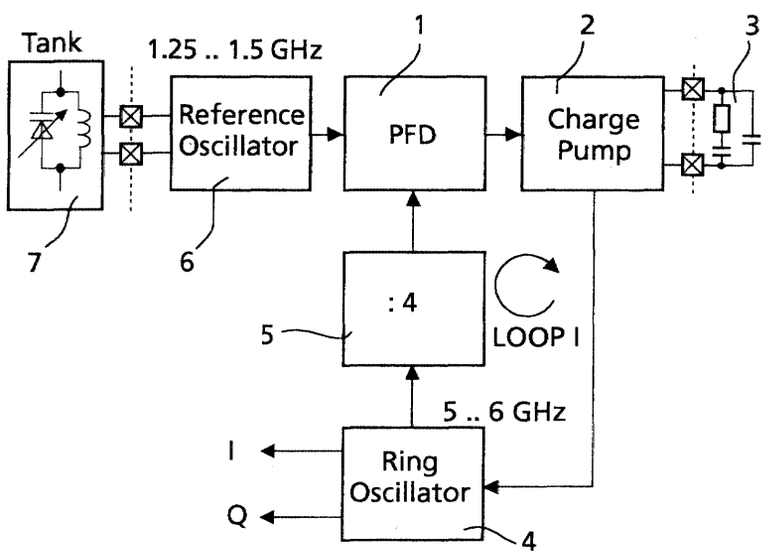

Fig.1

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Description

[0001] The present invention relates to a high frequency oscillator comprising a phase-locked loop (PLL), providing a tuned frequency range in the 5 to 6 GHz band.

[0002] Today, there are various activities to establish new wireless services in the 5 to 6 GHz band, e. g. European Hyperlan2 and IEEE 802.11a in the United States. As a consequence, a high demand for integrated oscillators and I/Q generation circuits exists, comprising a good phase noise.

[0003] High frequency oscillators using a phase-locked loop are well known in literature, for example from "Theorie und Anwendungen des Phase-Locked Loops", Roland Best, in "Der Elektroniker, No. 6/1975. A high frequency oscillator with a phase-locked loop comprising a phase frequency detector, a charge pump with a filter, a voltage control oscillator and a divider, the high frequency oscillator being controlled by a reference frequency, is known from Mehmet Soyuer et al.: "A FULLY MONOLITHIC 1,25 GHZ CMOS FREQUENCY SYNTHESIZER" Symposium on VLSI Circuits, US, New York, IEEE, 9 June 1994, pages 127 - 128, ISBN: 0-7803-1919-2, also from Buchwald et al.: "A 6 GHZ INTEGRATED PHASE-LOCKED LOOP USING ALGAAS/GAAS HETEROJUNCTION BIPOLAR TRANSISTORS", IEEE Journal of Solid State Circuits, US, IEEE Inc. New York, Vol. 27, No. 12, 01.12.1992, pages 1752-1762, XP000329025, and Novof et al.: "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and 50 ps jitter", IEEE Journal of Solid State Circuits, US, IEEE Inc New York, Vol. 30, No. 11, 01.11.1995, pages 1259-1266, XP000553064. A further reference, relating to a fully integrated oscillator in the GHz range and to a ring oscillator, is Pottbaecker and Langmann: "AN 8 GHZ SILICON BIPOLAR CLOCK-RECOVERY AND DATA-REGENERATOR IC", *IEEE Journal of Solid-State Circuits,* IEEE, Dec. 1994, Vol. 29, pp. 1572-1576.

[0004] The object of the present invention is therefore to provide a high frequency oscillator with a good phase noise in the 5 to 6 GHz band, which allows especially a cost effective integration on an IC.

[0005] This object is achieved by means of the invention as specified in claim 1. Advantageous developments of the invention are specified in the subclaims.

[0006] The high frequency oscillator of the invention comprises a reference oscillator and a phase-locked loop circuit with a phase frequency detector, a charge pump, a ring oscillator and a divider, the reference oscillator being coupled to the phase frequency detector for frequency control. The reference oscillator works advantageously in the range of 1,25 - 1,5 GHz and is a Colpitts type digital controlled frequency synthesizer with an external tank circuit for providing low phase noise, and the dividing factor of the divider is four for providing a tuned output range of 5 to 6 GHz. The ring oscillator is a symmetrical delay cell oscillator containing two delay cell amplifiers, which provide advantageously ground-free I/Q output signals, having a very low phase noise due to the phase-locked loop.

[0007] The phase-locked loop circuit is integrated together with the reference oscillator into an integrated circuit, using advantageously a BICMOS Silicon/Germanium process, which is well suited for RF applications. The tank circuit of the reference oscillator and the loop filter of the charge pump are external to the integrated circuit. Advantageous embodiments, especially relating to the charge pump and to the ring oscillator, are set up in the subclaims and are explained in the further description.

[0008] The invention is now explained below by way of an embodiment with reference to schematic drawings, which show:

Fig. 1 a high frequency oscillator for the 5 to 6 GHz range;
Fig. 2 the charge pump of the high frequency oscillator of Fig. 1;
Fig. 3 the ring oscillator of the high frequency oscillator of Fig 1;
Fig. 4 the ring oscillator according to Fig. 1, comprising a loop with a phase detector;
Fig. 5 the delay cell oscillator according to Fig. 3 comprising a arrangement for phase and frequency control; and
Fig. 6 a circuit diagram of the delay cell oscillator according to Fig. 5.

[0009] As shown in Fig 1, a reference oscillator 6 with a tuning circuitry, an external tank circuit 7, is used as a VCO for providing a reference frequency with a good phase noise. To cover a local oscillator (LO) range from 5 to 6 GHz, a small tuning range from 1.25 to 1.5 GHz is preferably used for the reference oscillator 6. This is achievable with an external LC-tank 7 of reasonably high Q.

[0010] The reference frequency of the reference oscillator 6 is applied to a phase-frequency detector 1, operating from 1,25 to 1,5 GHz, of a phase-locked loop (PLL) circuit, which comprises further a charge pump 2 with a loop filter 3, a ring oscillator 4 (DCO, delay cell oscillator) and a divider 5. The PFD (phase-frequency detector) 1 compares phase and frequency of the DCO 4 against the reference oscillator 6. The PFD output is filtered by the loop filter 3 of the charge pump 2 and applied to the DCO 4 for frequency control.

[0011] For the charge pump 2 and the loop filter 3, a fully differential architecture is used to avoid disturbances on the tuning control voltage. If the loop bandwidth is high, the loop reaction to phase changes is very fast, therefore phase noise is reduced. The DCO frequency is divided by four by the divider 5, before it is applied to the PFD 1. For this

reason, the phase noise performance of the PLL-controlled DCO is worse than that of the reference source 6, in theory, by 12 dB.

[0012] The phase-frequency-detector 1 consists of two D-Flipflops (DFF) and an AND-gate for the RESET path. ECL-structures are used and optimized to operate up to 1.8 GHz. As the reference source an integrated Colpitts type oscillator with an external LC-tank 7 is used for the reference oscillator 6. The divider by four 5 is realized with ECL-Flipflops and optimized in terms of speed and current consumption.

[0013] The delay cell oscillator 4 (DCO) and the charge pump 2 will be explained now in more detail with regard to Fig. 2 and Fig. 3.

[0014] The charge pump 2 according to Fig. 2 has a wide bandwidth, only limited by the pin-pad-interface to the external loop filter 3 and the loop filter 3 itself. This is achieved by an architecture that uses only npn-transistors in the signal path, not requiring fast pnp or pMOS transistors. A first current source, pnp transistors 12, feed a constant current I_0, which is controlled by V_{ref}, to the collectors of the npn-transistor pair 11. At the input IN_{ch} of the npn transistor pair 11, the output signal of the PFD 1 is applied. The emitters of the transistor pair 11 are coupled via a second current source, $2*I_0$, to ground GND. At the output OUT_{ch} the difference of $\pm 2\times I_0 - I_0$ flows to the external loop filter 3. The signal at the loop filter 3 is sensed by a buffer 13 and forwarded as an output control voltage V_{cont} to the control input of the DCO 4.

[0015] To keep the output nodes in the proper operating range, a common mode amplifier 14 controls the average current of the pnp-transistors 12 to be exactly half of the current of the npn-transistors 11. A clamp circuit 15 ensures that the control signal of the DCO 4 is inside the allowed limits. The loop filter 3 is connected differentially to avoid distortions and crosstalk on the tuning line; there is no ground path for the loop filter 3. This is necessary for a steep tuning characteristic of the DCO 4.

[0016] The voltage controlled DCO 4, as shown in Fig. 3, is built up of two amplifiers A_1 and A_2, and forms a symmetrical ring oscillator. The voltage V_{cont} from the charge pump 2, Fig. 2, controls the tail current $2I_0$ for the amplifiers A1, A2 via a control amplifier A_c, see also Fig. 6. The delay of the amplifiers A1 and A2 is nearly linear depending on the current $2I_0$, enabling a rather linear characteristic of the frequency tuning. The current output of the amplifiers A1, A2 causes a voltage drop across load resistors R_c, see Fig. 6, resulting in a small-signal gain of about $\frac{I_0 \cdot R_c}{V_T}$.

[0017] By implementing the differential architecture completely on a chip (integrated circuit), RF interference effects, like LO leakage, can be minimized. This is a requirement for modern direct conversion receiver concepts. The principle of the circuit is well suited for fully integrated oscillators in the multi-GHz range and offers a very wide tuning range.

[0018] The phase noise of ring oscillators has been modelled in many studies, see for example in references A. Hajimiri, S.Limotyrakis and T.H.Lee, "Jitter and Phase Noise in Ring Oscillators", *IEEE Journal of Solid-State Circuits,* IEEE, June 1999, Vol. 34, pp. 790 - 804 [1], and B.Razavi, "A Study of Phase Noise in CMOS Oscillators", *IEEE Journal of Solid-State Circuits,* IEEE, March 196, Vol. 31, pp. 331 - 343 [2]. The calculation of phase noise in this work follows the comprehensive work of reference Hajimiri, A. and T.H. Lee, "The Design of *Low Noise Oscillators",* Kluwer Academic Publishers, Norwell, Massachusetts, USA, 1999 [3].

[0019] If we apply the calculations of the single-sideband phase noise of [3] to a bipolar differential ring oscillator 4 as depicted in Figure 3, we obtain the equation

$$L(\Delta f) = 10\log\left(\frac{N}{3}\cdot\frac{f_0^2}{\Delta f^2}\cdot\left(\frac{e}{I_0}+\frac{4kT}{R_c\cdot I_0^2}\right)\right) \qquad \text{(Eq. 1).}$$

[0020] In this equation, N is the number of delay stages, f_0 is the oscillation frequency and Δf is the frequency offset, where the phase noise is measured. As the noise sources, the collector current shot noise and the noise of the load resistor are taken into consideration, while the noise of the base resistance and the 1/f-noise are neglected. From Eq. 1 it is understood, that the tail current I_0 and the voltage swing $R_c \cdot I_0$ should be made large, which stands in contradiction to a low power design. A further conclusion from Eq. 1 is, to take only a minimum number of delay stages.

[0021] If we evaluate Eq. 1 with N = 2, I_0 = 400µA, R_c = 400Ω, f_0 = 6GHz and Δf = 10kHz, we obtain as phase noise L(10kHz) = -41 dBc/Hz. That means for systems with higher order modulation methods like QAM, this oscillator has to be controlled by a wideband PLL with a reference oscillator of respectively low phase noise.

[0022] Therefore, the phase noise performance of the delay cell oscillator 4 does not satisfy the needs of modern digital transmission systems. When controlled within a PLL, the reference oscillator 6 governs the phase noise of the VCO inside the loop bandwidth. The phase noise $S_{\phi o}$ of the PLL-output as a function of the frequency offset Δf may be expressed therefore as

$$S_{\Phi 0}(\Delta f) = S_{\Phi DCO}(\Delta f) \cdot \left(\frac{1}{1+G(\Delta f) \cdot H(\Delta f)} \right)^2 + S_{\Phi ref}(\Delta f) \cdot \left(\frac{G(s)}{1+G(\Delta f) \cdot H(\Delta f)} \right)^2 \quad \text{(Eq.2).}$$

[0023] In Eq. 2, $S_{\phi DCO}$ is the phase noise of the DCO as calculated in accordance with Eq. 1, $S_{\phi ref}$ is the phase noise of the reference oscillator 6, G(Δf) is the forward loop gain and H(Δf) stands for the reverse loop gain.

[0024] As the reference oscillator 6 inhibits a tank circuit 7 of resonance frequency f_{0ref} and quality factor Q_{ref}, noise figure F_{ref} and output power P_{ref}, its phase noise $S_{\phi ref}$ may be expressed according to Leesons formula as

$$S_{\Phi ref}(\Delta f) = \frac{1}{2} \left(1 + \frac{1}{4 \cdot Q_{ref}^2} \cdot \left(\frac{\omega_{0ref}}{\Delta f} \right)^2 \right) \frac{F_{ref} kT}{P_{ref}} \quad \text{(Eq. 3).}$$

[0025] The forward loop gain G(Δf) depends according

$$G(\Delta f) = K_{\Phi} \cdot Z_L(\Delta f) \frac{K_{VCO}}{\Delta f} \quad \text{(Eq. 4)}$$

on the phase detector and charge pump constant K_{Φ}, on the impedance Z_L of the loop filter 3 and on the tuning constant K_{VCO} of the VCO 4.

[0026] The reverse loop gain H(Δf) may be expressed as

$$H(\Delta f) = \frac{1}{N} \quad \text{(Eq. 5)}$$

as a function of the divider ratio N.

[0027] Inserting Eq. 4 to Eq. 6 in Eq. 3, the phase noise of the PLL circuit 1-5 can be calculated. For a realistic embodiment, the calculation is based on the assumptions:

6. DCO phase noise as calculated in section 3.1 for f_{DCO} = 6 GHz
7. DCO tuning constant K_{DCO} = 1000 2π MHz/V
8. Phase detector constant K_{Φ} = 0.5 mA/(2π rad)
9. Divider factor N = 4
10. Loop filter Z_L with C_1 = 0, C_2 = 22 pF, R_2 = 15 kΩ
11. Reference oscillator Q_{ref} = 20, f_{0ref} = 1.5 GHz, F_{ref} = 3, P_{ref} = 0.2 mW

[0028] As a result, the PLL is able to improve the phase noise, at e.g. 10 kHz offset frequency, from -41 dBc/Hz (free running VCO) to -78 dBc/Hz (VCO is PLL controlled). However, towards lower frequencies the phase noise increases, as the phase noise of the reference oscillator 6 increases. The choice of the loop filter 3 is critical, in that it influences the resonance at the characteristic frequency of the PLL. To achieve a good phase noise performance, the low-noise-reference oscillator 6 has to operate also on a high-Q-resonator with Q_{ref} > 20 and the bandwidth of the loop PLL should be > 20 MHz.

[0029] According to measurements, the DCO frequency may be tuned from 3.5 GHz up to 6 GHz. The phase noise performance is limited by the reference oscillator 6. Using an external reference with L(10kHz)=-104 dBc/Hz at 1.25 GHz operating frequency, the measured phase noise is -90 dBc/Hz at 5 GHz overall. This is 2 dB worse than the expected theoretical 12 dB reduction in phase noise between reference and DCO.

[0030] The high frequency oscillator may comprise also a second loop with a phase detector 21 coupled to the I/Q output signals of the ring oscillator 4, as shown in Fig. 4. The phase detector 21 provides an error signal V_{phase} for the ring oscillator 4, when the phase difference between the I and the Q signal differs from 90°, so that always orthogonality between the I and Q signals is maintained over the complete frequency bandwidth during the operation of the high frequency oscillator.

[0031] The phase control signal V_{phase} is coupled to the delay cell amplifiers A1 and A2 of the ring oscillator 4, as shown in Fig. 5. The delay cell amplifiers A1 and A2 are coupled in series, and provide each a phase shift of 90°. The outputs of the delay cells A1, A2 are ground-free, and the output of the delay cell A2 is used for the I+ and the I- signal, and the output of the delay cell A1 is used for the Q+ and the Q- signal, see also Fig. 3. The output of the delay cell A2 is coupled via an inversion IV to the input of the delay cell A1, so that the oscillation condition of 360° is fulfilled.

[0032] The ring oscillator 4 comprises further an amplifier section $2I_0$ for providing a current of $2I_0$ to each of the delay cells A1 and A2, and to which amplifier section the control signal V_{cont} of the charge pump 2 is coupled, for providing the frequency control. The amplifier sections $2I_0$ are identical, so that the delay cells A1 and A2 are tuned symmetrically. The amplifier sections $2I_0$ are coupled to same current source 23.

[0033] The control signal of the phase detector 21 is coupled to a controllable current source 22, which is coupled to each of the amplifier sections $2I_0$. Via the current source 22 the control voltage V_{phase} provides an unsymmetry of the curents of the current source 23, via which a discrepancy of the required phase difference of 90° of the I/Q signals is corrected.

[0034] A detailed circuit diagram of the delay cell oscillator 4 is shown in Fig. 6. The ring oscillator 4 consists essentially of the delay cell amplifiers A1 and A2, the feedback loop with the inversion IV, and the control amplifier Ac for phase and frequency control. The delay cell amplifier 1 comprises an amplifier 31 which is coupled to the inputs of amplifier 32 of the delay cell amplifier A2, and which outputs provide the output signals I+/I- and Q+/Q- via load resistors R_c, which are coupled to a supply voltage VCC.

[0035] To the outputs of the amplifier 31 two amplifiers 33 and 34 are coupled for the delay and therefore the frequency tuning of the amplifier 31. The delay cell amplifier A2 is set up with amplifiers 32, 35 and 36 in correspondence to the delay cell amplifier A1, for providing a symmetrical delay cell oscillator.

[0036] The outputs of the amplifier 37 are coupled to the inputs of the amplifiers 33, 34 for providing a voltage control of the signals Q+, Q-, and are coupled to the outputs of the amplifiers 33, 34 for providing the delay, respectively the frequency adjustment. The frequency adjustment is provided by amplifier 37 of the control amplifier Ac, to which inputs the control signal V_{cont} is applied, and which outputs are coupled each as a supply voltage to the amplifiers 33 and 34. The amplifiers 35, 36 for the delay cell A2 are set up in the same manner as the amplifiers 33, 34. The control amplifier Ac comprises further an amplifier 38 for the delay cell A2, to which input the control signal V_{cont} is also applied, for a symmetric tuning of the delay cells A1 and A2.

[0037] The control amplifier Ac comprises further an amplifier 39, to which the phase control signal Vphase is applied at the input side. The outputs of the amplifier 39 are each coupled to amplifiers 37 and 38 for shifting amplifier 37 with respect to amplifier 38, to obtain the correct phase difference of 90° for the output signals I and Q. The delay cell oscillator 4 comprises therefore two symmetrical amplifier sections 33, 34, 37; 35, 36, 38 for frequency control, and an amplifier 39, which provides the phase control and which is coupled to these amplifier sections.

Claims

1. High frequency oscillator comprising a reference oscillator (6) and a phase locked-loop circuit with a phase-frequency detector (1), a charge pump (2), a ring oscillator (4) and a divider (5), the reference oscillator (6) being coupled to the phase-frequency detector (1) for frequency control, **characterized in that** the ring oscillator (4) is a symmetrical delay cell oscillator containing two delay cell amplifiers (A1, A2).

2. High frequency oscillator according to claim 1, **characterized in that** the reference oscillator (6) is a Colpitts type oscillator with a tank circuit (7), the reference oscillator (6) and the phase locked-loop circuit being integrated within an integrated circuit and the tank circuit (7) being external to the integrated circuit.

3. High frequency oscillator according to claim 1 or 2, **characterized in that** the tuning range of the reference oscillator (6) is 1,25 - 1,5 GHz, and the dividing factor of the divider (5) is four for providing a tuned output range of 5-6 GHz.

4. High frequency oscillator according to one of the preceding claims, **characterized in that** the two delay cell amplifiers (A1, A2) comprise a dual output stage for providing ground-free I/Q output signal generation.

5. High frequency oscillator according to one of the preceding claims, **characterized in that** the charge pump (2) comprises a ground-free loop filter (3), the loop filter (3) being external to the integrated circuit.

6. High frequency oscillator according to claim 5, **characterized in that** the input stage of the charge pump (2) is a differential amplifier and comprises only npn-transistors (11) in the signal path.

7. High frequency oscillator according to claim 6, **characterized in that** the charge pump (2) comprises a first current source with two pnp-transistors (12) and a second, common current source ($2I_0$), both being coupled to the differential amplifier (11), and that the current of first current source (12) is controlled by a reference voltage (VREF) to provide in each of the pnp-transistors half of the current of the second current source ($2I_0$).

8. High frequency oscillator according to one of the preceding claims, **characterized in that** to the delay cell oscillator (4) a loop (loop II) with a phase detector (21) is coupled for a phase control between the I- and the Q-signal.

9. High frequency oscillator according to one of the preceding claims, **characterized in that** the delay cell oscillator (4) comprises two symmetrical amplifier sections (33, 34, 37; 35, 36, 38) for frequency control, which are each coupled to an output of an delay cell amplifier (31, 32), and an amplifier (39) for a phase control, which is coupled to the two amplifier sections (33, 34, 37; 35, 36, 38).

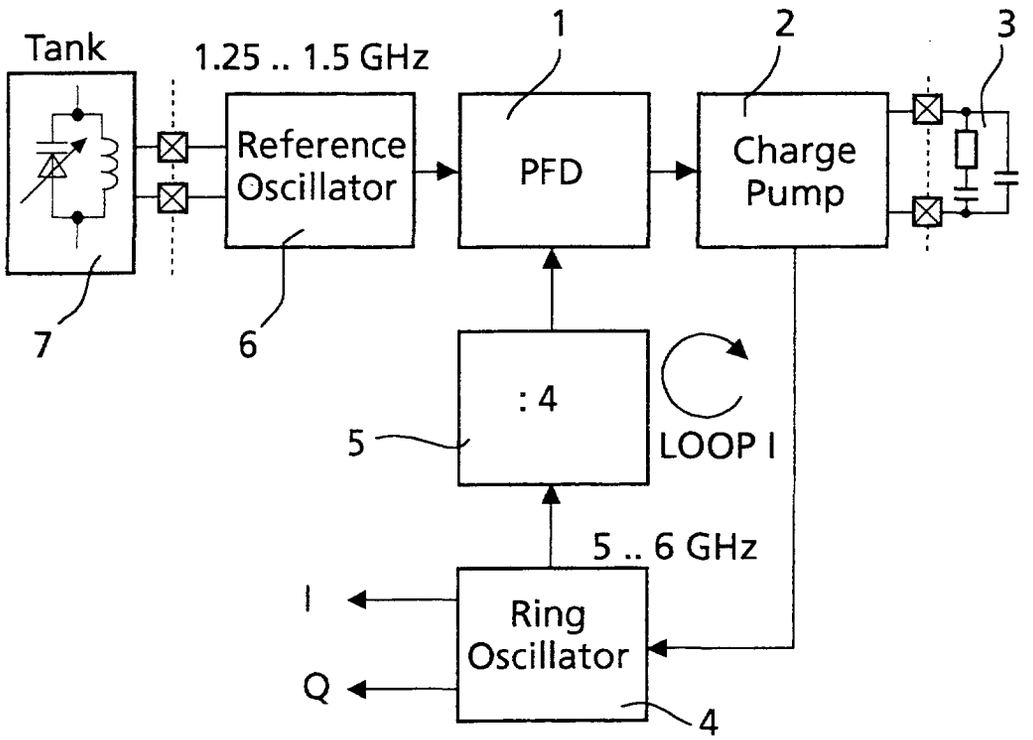

Tank
1.25 .. 1.5 GHz
1
2
3
Reference Oscillator
PFD
Charge Pump
7
6
: 4
5
LOOP I
5 .. 6 GHz
I
Ring Oscillator
Q
4

Fig.1

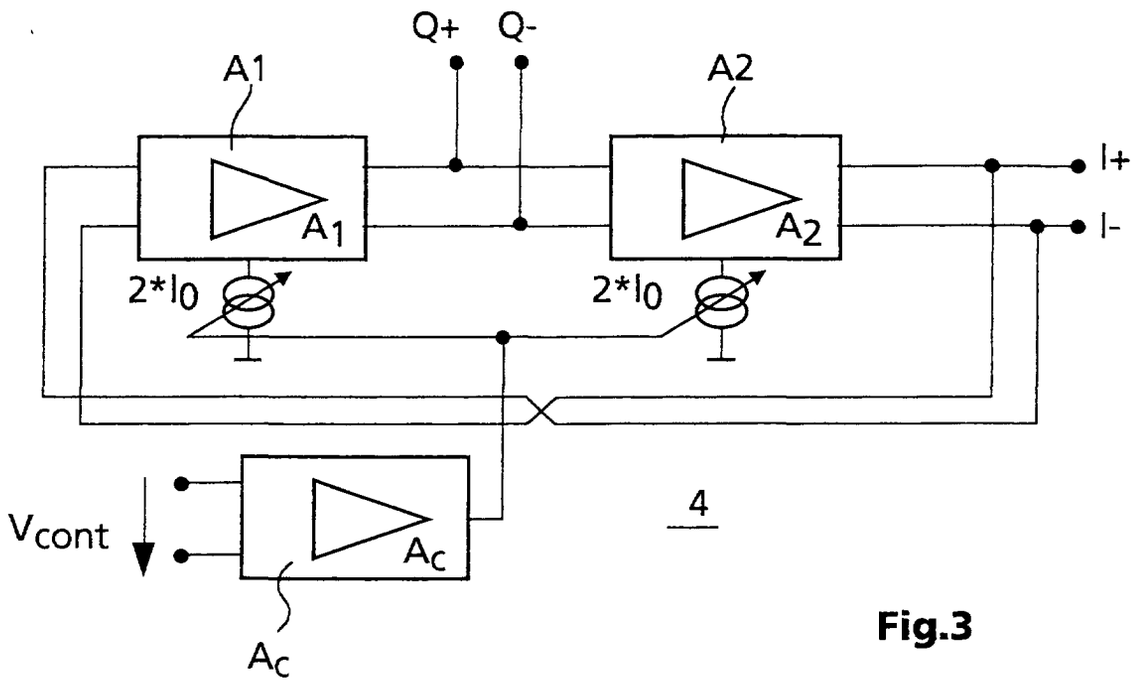
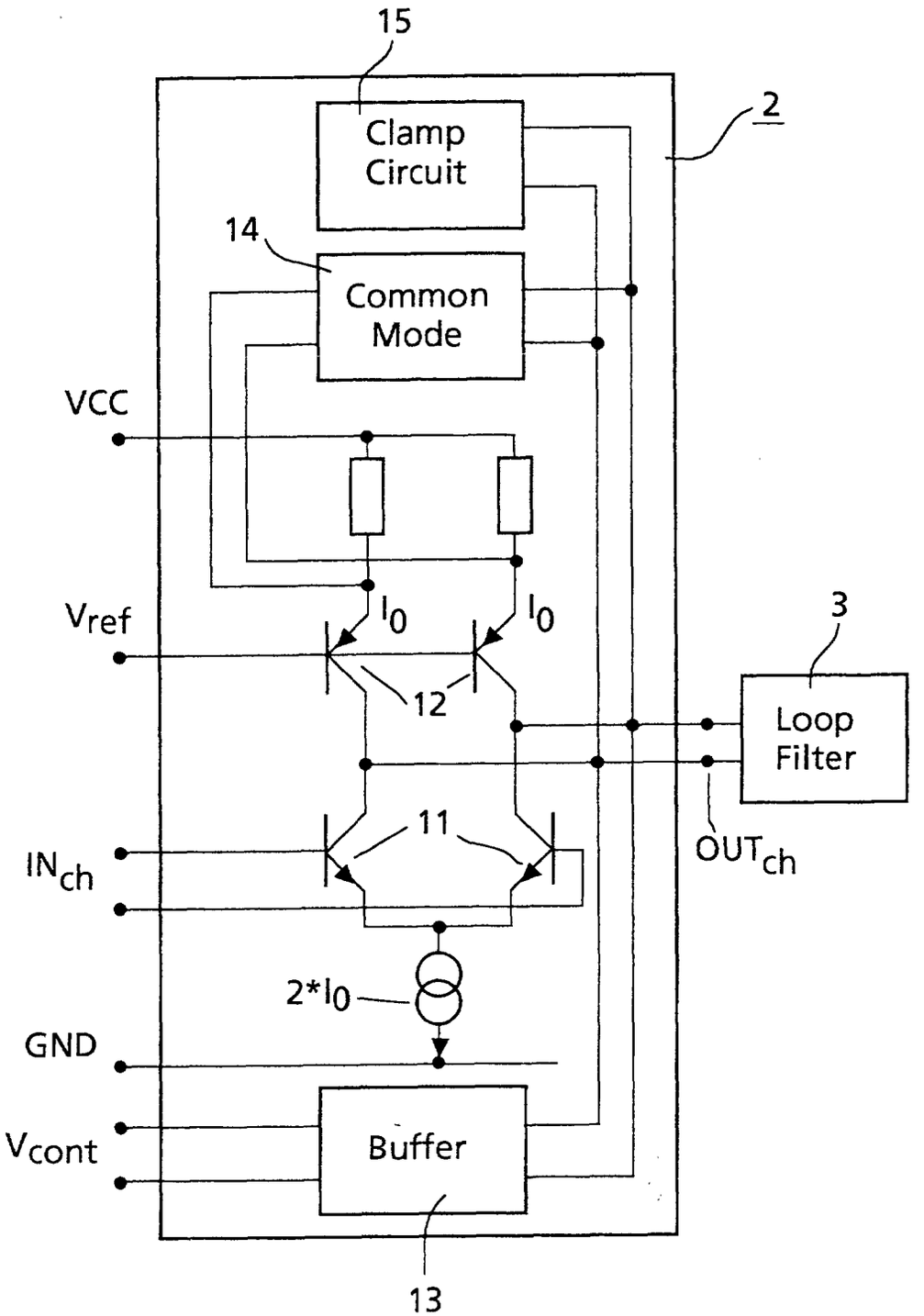

Q+
Q-
A1
A2
A1
A2
I+
I-
2*I0
2*I0
Vcont
Ac
4
Ac

Fig.3


15
Clamp Circuit
2
14
Common Mode
VCC
Vref
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I_0
12
3
Loop Filter
11
IN_{ch}
OUT_{ch}
$2*I_0$
GND
Vcont
Buffer
13

Fig.2

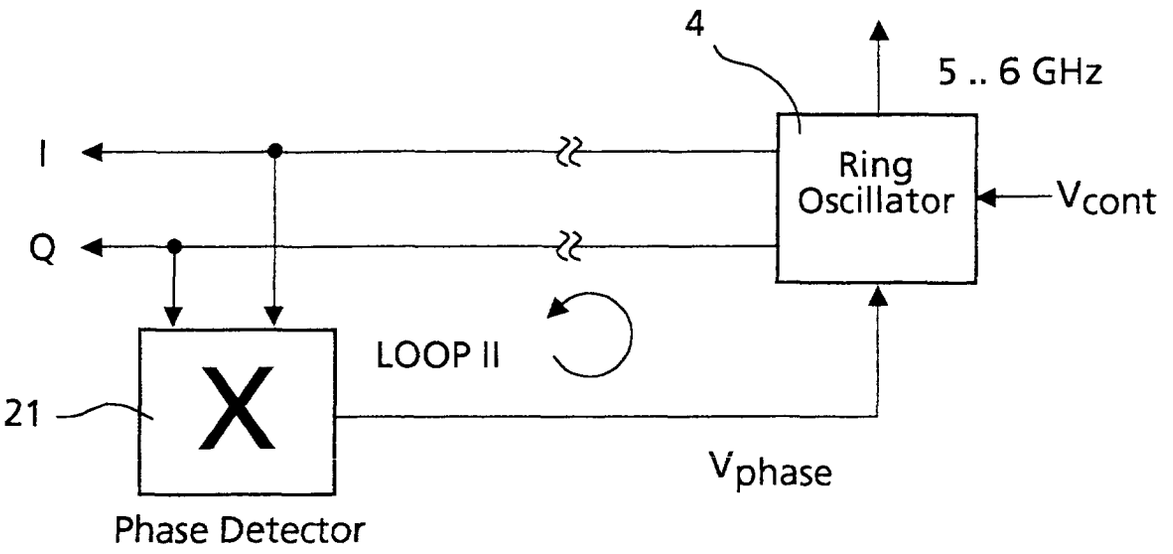
4
5 .. 6 GHz
I
Q
Ring
Oscillator
Vcont
LOOP II
21
X
Vphase
Phase Detector

Fig.4

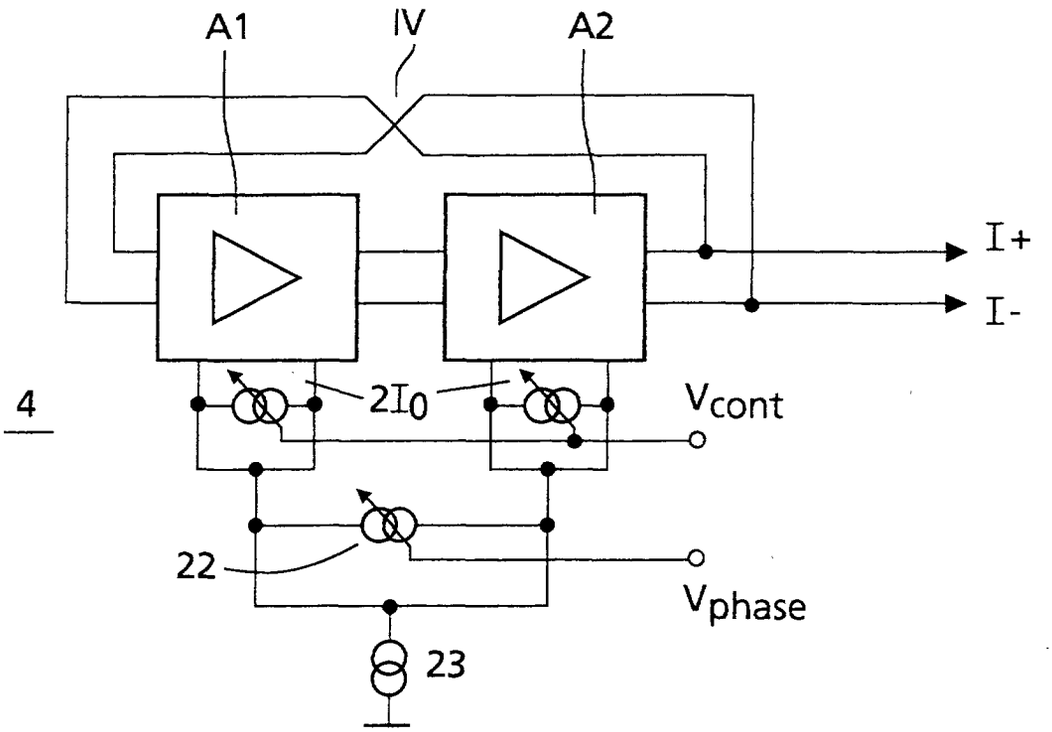
A1
IV
A2
I+
I-
4
2I0
Vcont
22
Vphase
23

Fig.5

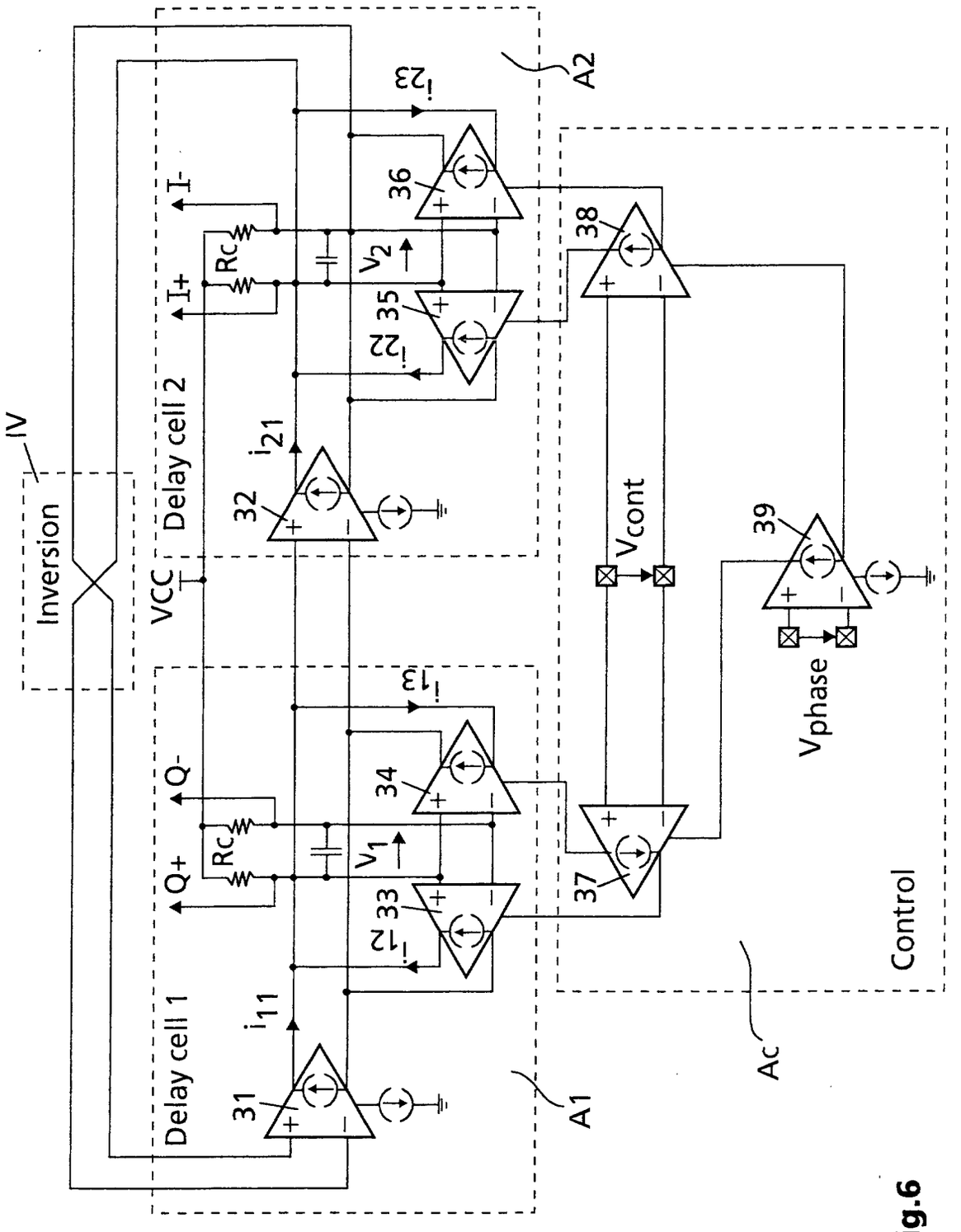
IV
Inversion
VCC
Delay cell 2
Delay cell 1
A2
A1
Ac
Control
I-
I+
Q-
Q+
Rc
V_2
V_1
i_{21}
i_{11}
i_{23}
i_{13}
i_{22}
i_{12}
31
32
33
34
35
36
37
38
39
Vcont
Vphase

Fig.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 11 4626

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X,D	MEHMET SOYUER ET AL: "A FULLY MONOLITHIC 1.25GHZ CMOS FREQUENCY SYNTHESIZER" SYMPOSIUM ON VLSI CIRCUITS. DIGEST OF TECHNICAL PAPERS. HONOLULU, JUNE 9 - 11, 1994, NEW YORK, IEEE, US, 9 June 1994 (1994-06-09), pages 127-128, XP000501055 ISBN: 0-7803-1919-2 * the whole document *	1,4	H03L7/099
X	US 5 889 437 A (LEE SEOG-JUN) 30 March 1999 (1999-03-30) * column 1, line 6 - line 10 * * column 2, line 35 - line 60 * * column 3, line 25 - column 4, line 20 * * column 4, line 62 - column 5, line 5 * * column 5, line 36 - column 6, line 20 * * column 10, line 4 - line 56 * * figures 1,2,5,7 *	1,5	
Y		2	
Y	US 6 081 164 A (KARASAWA HIDEO ET AL) 27 June 2000 (2000-06-27) * column 10, line 42 - column 12, line 37 * * column 14, line 49 - line 62; figures 1-4,6A,6B * * column 22, line 35 - column 24, line 36 * * figures 1-4,6A,6B,16-18 *	2	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H03L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	22 November 2001	Balbinot, H

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US 6081164 A	27-06-2000	WO 9831104 A1	16-07-1998

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