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(71) Applicant: **TEXAS INSTRUMENTS DEUTSCHLAND GMBH**
85356 Freising (DE)

(72) Inventor: **Gerber, Johannes**
80995 München (DE)

(74) Representative:
Schwepfinger, Karl-Heinz, Dipl.-Ing.
Prinz & Partner GbR
Manzingerweg 7
81241 München (DE)

(54) Current mirror circuit

(57) A current mirror circuit serves to produce an output current flowing in an output branch corresponding to a reference current flowing in an input branch located between a supply voltage terminal and ground. Located in the input branch is a first bipolar transistor (10) through the collector/emitter circuit of which the reference current furnished by a current source (14) connected to the collector flows. Through the collector/emitter circuit of a second bipolar transistor (12) located in the output branch the output current flows. The bases of the two transistors (10, 12) are connected to each other. A further current mirror circuit (16, 18, 20) is provided having an input branch located between the supply voltage terminal and ground and an output branch located between the supply voltage terminal and the connected bases of the two bipolar transistors (10, 12) for generating a base current (I_b) for these transistors. A current source (20) controlled by the collector voltage of the first bipolar transistor (10) is located in the input branch of this further current mirror circuit (16, 18, 20), the output current ($2I_b$) of said current source (20) being mirrored in the output branch of said further current mirror circuit (16, 18, 20).

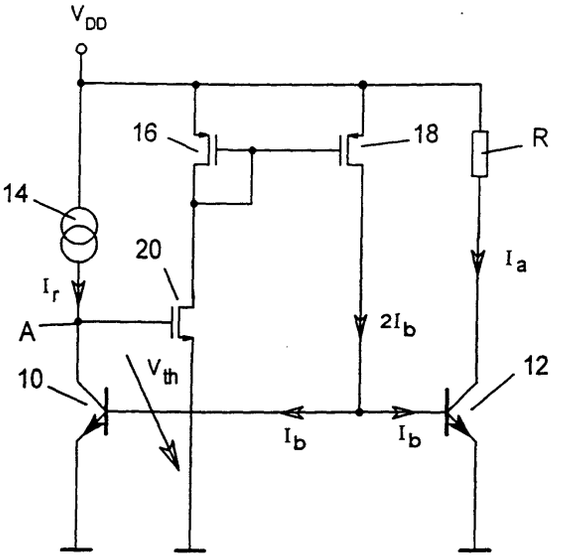

Fig.1

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Description

[0001] The invention relates to a current mirror circuit for producing an output current flowing in an output branch corresponding to a reference current flowing in an input branch located between a supply voltage terminal and ground, including a first bipolar transistor in the input branch through the collector/emitter circuit of which the reference current furnished by a current source connected to the collector flows and a second bipolar transistor in the output branch through the collector/emitter circuit of which the output current flows, the bases of the two transistors being connected to each other.

[0002] Current mirror circuits are used to generate a current in an output branch corresponding as precisely as possible to a current flowing in an input branch. It is also possible to generate the current in such a circuit in the output branch so that it is available in a precise ratio to the current in the input branch. In a known circuit of this kind, as shown in Fig. 2, two bipolar transistors 10, 12 are provided, the first of which is located in the input branch whilst the second is located in the output branch. The reference current I_r flowing in the input branch for mirroring in the output branch as the current I_a is generated by a current source 14. As evident, the bases of the two transistors 10 and 12 are connected to each other and the base current I_b required by these transistors is furnished via the drain/source circuit of a MOS field-effect transistor 16 the gate of which is connected to the collector of the transistor 10. Since the gate of the MOS field-effect transistor 16 absorbs no current it is the reference current I_r generated by the current source 14 that flows through the collector/emitter circuit of the transistor 10. This current then flows due to the known current mirror effect also through the collector/emitter circuit of the transistor 12 so that the desired effect is achieved, namely that in the output branch of the circuit a current I_a flows corresponding to the reference current I_r.

[0003] Although this known circuit as shown in Fig. 2 satisfies the cited condition very precisely it has drawbacks when only a small supply voltage V_{DD} is available as is often the case in modern battery-powered electronic instruments. As evident a voltage materializes at point A of the circuit corresponding to the sum of the base/emitter voltage of the bipolar transistor 10 and the threshold voltage V_{th} of the MOS field-effect transistor 16. These two voltages amount to roughly 0.7 V so that at point A a voltage of at least 1.4 V occurs. When, however, the supply voltage V_{DD} amounts only to 1.8 V as may very well be the case in practical applications then a voltage of not more than 0.4 V is available for operation of the current source 14 which is not sufficient to configure the current source 14 with simple means to reliably furnish the desired reference current I_r. Thus, the circuit as shown in Fig. 2 is only suitable for operation with higher supply voltages.

[0004] The invention is based on the object of configuring a current mirror circuit of the aforementioned kind so that it is able, despite low operating voltages, to mirror the reference current flowing in the input branch with high accuracy in the output branch.

[0005] This object is achieved in a current mirror circuit of the aforementioned kind by a further current mirror circuit having an input branch located between the supply voltage terminal and ground and an output branch located between the supply voltage terminal and the connected bases of the two bipolar transistors for generating a base current for these transistors, a current source controlled by the collector voltage of the first bipolar transistor being located in the input branch of this further current mirror circuit, the output current of this current source being mirrored in the output branch of this further current mirror circuit.

[0006] In the current mirror circuit in accordance with the invention the base current required for the bipolar transistors is produced by a further current mirror circuit capable of producing this base current in its output branch without requiring current to be branched from the reference current I_r. Due to making use of this further current mirror circuit and its current source located in the input branch between the supply voltage terminal and ground the unavoidable drop in voltage is greatly reduced so that the voltage remaining for operating the current source furnishing the reference current I_r in the input branch becomes corresponding larger. The current mirror circuit is thus able to mirror the reference current I_r in its output branch with high accuracy even when the supply voltage is low.

[0007] The invention will now be detailled by way of example with reference to the drawing in which:

Fig. 1 is a circuit diagram of a current mirror circuit in accordance with the invention and

Fig. 2 is a circuit diagram of a prior art current mirror circuit.

[0008] Referring now to Fig. 1 there is illustrated the current mirror circuit containing as its basic components the two bipolar transistors 10 and 12 as well as the current source 14 furnishing the reference current I_r. The output current I_a to be generated flows through a load resistor R.

[0009] The circuit as shown in Fig. 1 contains a further current mirror circuit consisting of two p-channel MOS field-effect transistors 16 and 18 as well as an n-channel MOS field-effect transistor 20 acting as the current source. The gates of the p-channel MOS field-effect transistors 16 and 18 are connected to each other whilst their sources receive the supply voltage V_{DD}. The drain of the p-channel MOS field-effect transistor 16 is connected to the gates of these two MOS transistors. Furthermore, the drain of the p-channel MOS field-effect transistor 16 is connected to the drain of the n-channel MOS field-effect transistor 20 whose source is directly

grounded.

[0010] As evident from Fig. 1 a voltage occurs at the point A which corresponds to the threshold voltage V_{th} of the n-channel MOS field-effect transistor 20. This means that for the same supply voltage V_{DD} for operating the current source 14 a voltage is available which as compared to that of the current mirror circuit as shown in Fig. 2 is higher by the base/emitter voltage V_{be}. For a supply voltage V_{DD} of 1.8 V and a threshold voltage V_{th} of 0.7 V a voltage of 1.1 V is thus available at the circuit point A. It is with this voltage that the current source 14 can be operated by simple ways and means. The wanted object, namely to mirror the reference current I_r flowing in the input branch precisely in the output branch is thus achieved by very simple circuitry.

Claims

1. A current mirror circuit for producing an output current flowing in an output branch corresponding to a reference current flowing in an input branch located between a supply voltage terminal and ground, including a first bipolar transistor in the input branch through the collector/emitter circuit of which the reference current furnished by a current source connected to the collector flows and a second bipolar transistor in the output branch through the collector/emitter circuit of which the output current flows, the bases of the two transistors being connected to each other, **characterized by** a further current mirror circuit (16, 18, 20) having an input branch located between the supply voltage terminal and ground and an output branch located between the supply voltage terminal and the connected bases of the two bipolar transistors (10, 12) for generating a base current (I_b) for these transistors, a current source (20) controlled by the collector voltage of the first bipolar transistor (10) being located in the input branch of this further current mirror circuit (16, 18, 20), the output current ($2I_b$) of said current source (20) being mirrored in the output branch of said further current mirror circuit (16, 18, 20).

2. The current mirror circuit as set forth in claim 1, **characterized in that** said controlled current source is an n-channel MOS field-effect transistor (20) whose source is grounded, that said further current mirror circuit contains two p-channel MOS field-effect transistors (16, 18) whose gates are connected to each other, the drain of the one p-channel MOS field-effect transistor (16) being connected to the drain of said n-channel MOS field-effect transistor (20) and its gate, and the drain of the other p-channel MOS field-effect transistor (18) being connected to the bases of said two bipolar transistors bipolar transistor (10, 12) whilst the sources of said p-channel MOS field-effect transistors (16, 18) are connected to the supply voltage terminal.

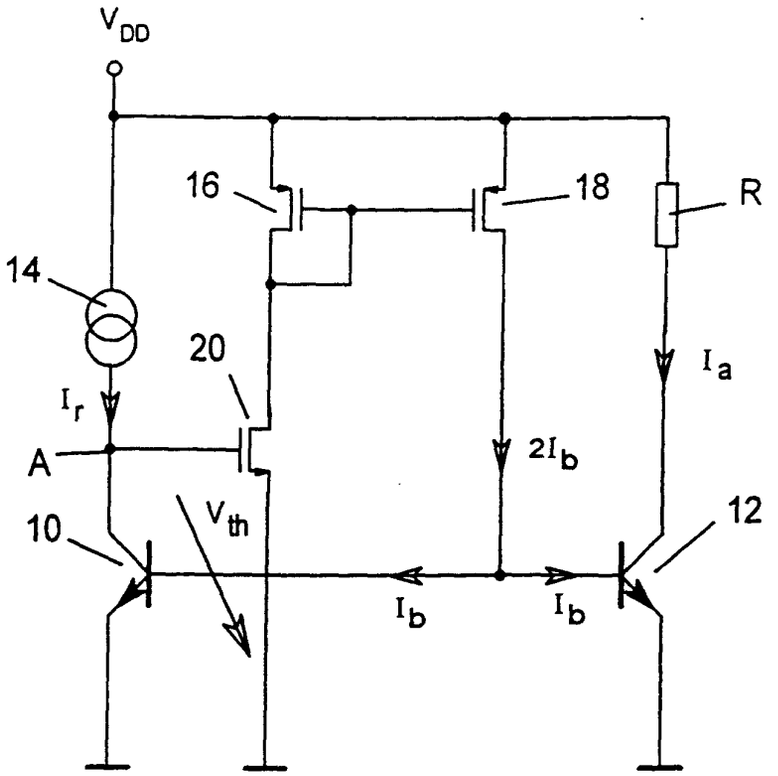
V_{DD}
16
18
R
14
20
I_a
I_r
A
$2I_b$
V_{th}
10
12
I_b
I_b

Fig.1

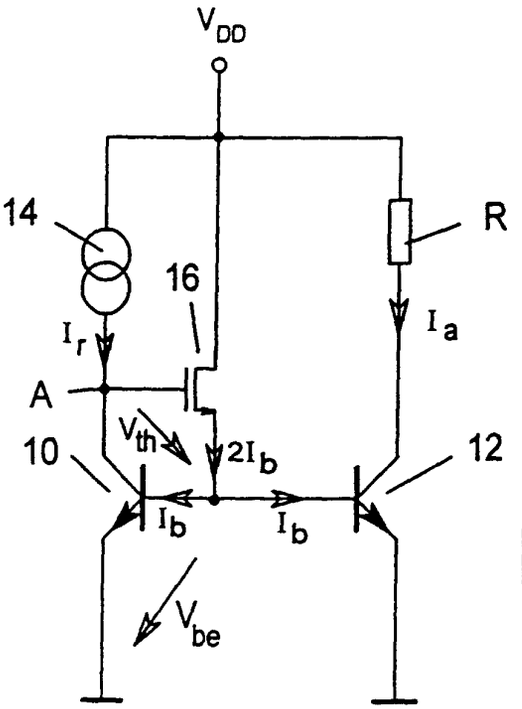
V_{DD}
14
R
16
I_a
I_r
A
V_{th}
$2I_b$
10
12
I_b
I_b
V_{be}

Fig.2