

Europäisches Patentamt European Patent Office Office européen des brevets



(11) **EP 1 239 591 A3**

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3: **02.05.2003 Bulletin 2003/18**

(51) Int Cl.7: **H03K 19/0185**, H03K 19/003

(43) Date of publication A2: 11.09.2002 Bulletin 2002/37

(21) Application number: 02004689.2

(22) Date of filing: 31.03.1998

(84) Designated Contracting States: **DE FR NL**

(30) Priority: 31.03.1997 JP 7938597

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC: 98105843.1 / 0 869 616

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(54) Input circuit for an integrated circuit

(57) An input circuit comprising:

a first type field effect transistor (P1) having a channel of one conductivity, having a gate connected to a first power supply (V_{DD}), having a first electrode connected said first power supply and having a second electrode connected a first node (S),

a second type field effect transistor (P_2) having a channel of one conductivity, having a gate connected to a second node (G), having a first electrode connected to said first node, having a second electrode connected to a third node (IN), having a substrate connected to a fourth node (B) which is floating,

a third type field effect transistor (P_4) having a channel of one conductivity, having a gate connected to said first power supply, having a first electrode connected to said second node (G), having a second electrode connected to said third node (IN) and having a substrate connected to said fourth node (B), a fourth type field effect transistor (N_7) having a channel of the opposite conductivity, having a gate connected to said first power supply, having a first electrode connected to said third node (IN) and having a second electrode connected to a fifth node

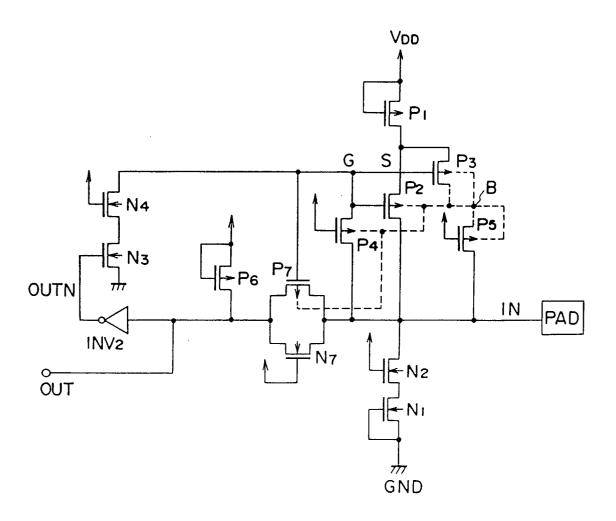
(OUT).

a fifth type field effect transistor (P₇) having a channel of one conductivity, having a gate connected said second node (G), having a first electrode connected to said fifth node (OUT), having a second electrode connected to said third node (IN) and having a substrate connected to said fourth node (B), an inverter means (INV₂) having an input terminal connected to said fifth node (OUT) and an output terminal connected to a sixth node (OUTN),

a sixth type field effect transistor (N_3) having a channel of the opposite conductivity, having a gate connected to said sixth node (OUTN), having a first electrode connected to a second power supply and having a second electrode connected to a seventh node, and

a seventh type field effect transistor (N_4) having a channel of the opposite conductivity, having a gate connected to said first power supply, having a first electrode connected to said seventh node and having a second electrode connected to said second node (G).

FIG. 14





EPO FORM 1503 03.82 (P04C01)

EUROPEAN SEARCH REPORT

Application Number EP 02 00 4689

Category	Citation of document with indica of relevant passages		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CI.7)	
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27-02-2003

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FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82