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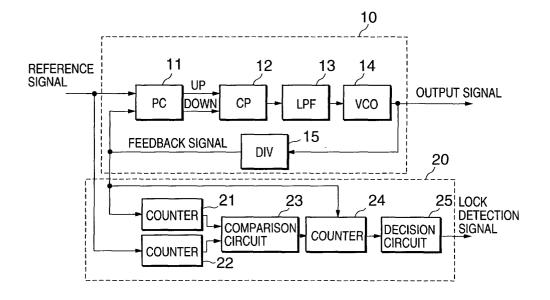
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(54) Lock detection circuit

(57) There is provided a lock detection circuit for optimizing a lock detection time and an unlock detection time of a PLL circuit. The present invention has counters 21 and 22 for inputting and counting feedback signals and reference signals inputted to a phase comparator 11 of a PLL circuit 10; a comparison circuit 23 for inputting and comparing count values of the counters 21 and 22 and outputting a control signal in an active state when the count value of the counter 21 is a first value and the

count value of the counter 22 is the first value; a counter 24 for counting the feedback signals when the control signal outputted from the comparison circuit 23 is active; and a decision circuit 25 for outputting an output signal of a value showing a lock state when a count value of the counter 24 reaches a second value. The comparison circuit 23 resets the counter 24 when the count value of the counter 21 is the first value and the count value of the counter 22 is not the first value.

FIG. 1





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Application Number EP 02 00 7351

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