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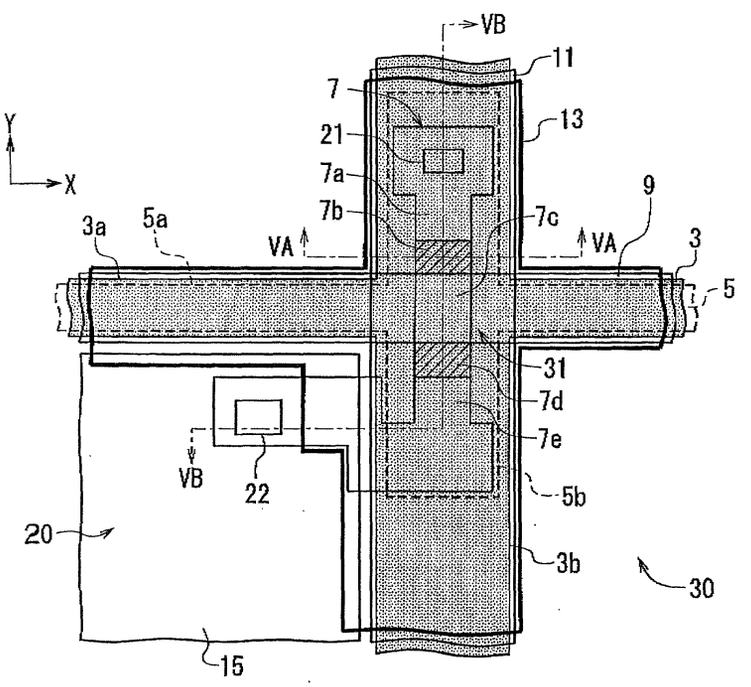
(54) TFT array substrate and active-matrix addressed liquid-crystal display device

(57) A TFT array substrate (30) is provided, which effectively blocks the light traveling toward the active layers of the TFTs. A patterned first light-shielding layer (3) is formed between a transparent plate and TFTs in such a way as to overlap with the active layers of the TFTs. A patterned third light-shielding layer (13) is formed to cover the TFTs on the opposite side to the plate with respect to the TFTs. The third light-shielding layer (13) has the first parts extending along the rows of the matrix and the second parts extending along the columns thereof. A patterned second light-shielding layer (5) is formed between the first light-shielding layer and the TFTs. The second light-shielding layer (5) has a light-absorbing property, which absorbs the light entering the inside of the substrate. A patterned fourth light-shielding layer, which has a light-absorbing property, may be additionally provided between the TFTs and the third light-shielding layer.

FIG. 4



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to Liquid-Crystal Display (LCD) devices. More particularly, the invention relates to a substrate on which Thin-Film Transistors (TETs) are arranged in a matrix array, i.e., a TFT array substrate, and an active-matrix addressing LCD device equipped with the substrate. This substrate and device are preferably applicable to the light bulb of the projection type display device.

2. Description of the Related Art

[0002] In recent years, various types of display devices applicable to wall-hung type televisions (TVs), projection type TVs, or Office Automation (OA) equipment have been developed. To realize high-grade display devices for OA equipment or high-definition TVs (HDTVs), active-matrix addressing LCD devices utilizing TFTs as their switching elements are more promising within the conventional display devices. This is because active-matrix LCD devices have an advantage that contrast and response speed do not degrade even if the count of the scan lines is increased. Moreover, active-matrix LCD devices have another advantage that a large-sized display screen can be easily realized if they are used as the light bulb of projection-type display devices.

[0003] With the LCD device designed for the light bulb, normally, high-luminance light is inputted into the LCD device from a light source and then, the light thus inputted is controlled according to the image information while the light passes through the same device. In other words, the intensity of the light transmitted through the device is adjusted by changing the transmittance of the individual pixels by application of electric field to the respective pixels while driving the TFTs. The light passed through the device is then enlarged and projected onto a large screen by way of a projection light system including specific lenses.

[0004] The light source is located on the opposite substrate side of the LCD device while the projection light system is on the TFT-array substrate side. Thus, not only the light emitted from the light source but also the light reflected by the projection light system will enter the device.

[0005] With the active-matrix addressing LCD device, a layer of semiconductor such as amorphous silicon or polysilicon (i.e., a semiconductor layer) is used for the active layer of each TFT. If light is irradiated to the active layer, current leakage will be induced due to optical excitation. On the other hand, as described previously, high-luminance light is inputted into the LCD device for the light bulb and thus, the current leakage will be large. Since, in addition to the light from the source, the reflected light by the projection light system is irradiated to the active layer, the current leakage is likely to be larger.

[0006] Recently, there is a tendency that the projection type LCD device is designed to be more compact and to have higher luminance. Thus, the luminance of the light inputted into the device tends to be higher. From this point of view, the above-described problem about the current leakage will be more serious. To solve this problem, with prior-art active-matrix addressing LCD devices for the light bulb, light-shielding layers are provided to prevent the light from irradiating to the active layers of the TFTs.

[0007] Fig. 1 and Figs. 2A and 2B show the schematic configuration of the TFT array substrate 100 of a prior-art LCD device of this type, in which only one pixel is illustrated for simplification. Fig. 1 is a partial plan view of the substrate 100, Fig. 2A is a cross-sectional view along the line IIA-IIA in Fig. 1, and Fig. 2B is a cross-sectional view along the line IIB-IIB in Fig. 1. These figures show the structure of one pixel, because all the pixels have the same structure.

[0008] The prior-art TFT array substrate 100 comprises a transparent plate 101, on which TFTs 131 are arranged in a matrix array. A lower light-shielding layer 103, which is made of tungsten silicide (WSi_2), is formed over the plate 101 by way of a silicon dioxide (SiO_2) layer 102. The plan shape of the lower light-shielding layer 103 is like a lattice, which is formed by lateral strips extending along the rows (the X direction in Fig. 1) of the matrix of the TFTs 131 and vertical strips extending along the columns (the Y direction in Fig. 1) thereof and intersecting with the lateral ones. The whole layer 103 is covered with an overlying SiO_2 layer 104.

[0009] Patterned polysilicon layers 107, which serve as the active layers of the TFTs 131, are formed on the SiO_2 layer 104. Each of the layers 107 has a plan shape like L.

[0010] Each of the polysilicon active layers 107 comprises an undoped channel region 107c, two lightly-doped LDD (Lightly-Doped Drain) regions 107b and 107d, a heavily-doped source region 107a, and a heavily-doped drain region 107e. The source and drain regions 107a and 107e are located at each side of the channel region 107c. The LDD region 107b is located between the source region 107a and the channel region 107c. The LDD region 107d is located between the channel region 107c and the drain region 107e.

[0011] The source region 107a, the LDD region 107b, the channel region 107c, the LDD region 107d, and the drain region 107e are arranged along the Y direction in such a way as to overlap with the lower light-shielding layer 103. Part of the drain region 107e is extended in the X direction.

[0012] A gate dielectric layer 108 is formed on the SiO_2 layer 104 to cover the underlying active layers 107.

[0013] Gate lines 109, which are made of impurity-doped polysilicon or silicide, are formed on the gate dielectric layer 108. These lines 109 are parallel to each

other and extend in the X direction. Each of the lines 109 is located to overlap with the channel regions 107c of the TFTs 131 that belong to the same row of the matrix. The parts of the line 109 placed right over the regions 107c serve as gate electrodes of the corresponding TFTs 131. The lines 109 are entirely covered with a first interlayer dielectric layer 110.

[0014] Data lines 111, which are made of aluminum (Al), are formed on the first interlayer dielectric layer 110. These lines 111 are parallel to each other and extend in the Y direction. Each of the lines 111 is located to overlap with the active layers 107 of the TFTs 131 that belong to the same column of the matrix. The line 111 entirely covers the source regions 107a, the channel regions 107c, and the LDD regions 107b and 107d of the corresponding TFTs 131. The line 111 covers parts of the drain regions 107e of the corresponding TFTs 131. The line 111 is mechanically contacted with and electrically connected to the source regions 107a of the TFTs 131 that belong to the same row of the matrix by way of contact holes 121 that penetrate the first interlayer dielectric layer 110 and the gate dielectric layer 108. The lines 111 are entirely covered with a second interlayer dielectric layer 112.

[0015] A patterned black matrix layer 113, which is made of chromium (Cr), is formed on the second interlayer dielectric layer 112. The plan shape of the layer 113 is like a lattice, which is formed by lateral strips extending along the rows (the X direction in Fig. 1) of the matrix and vertical strips extending along the columns (the Y direction in Fig. 1) thereof and intersecting with the lateral ones. The layer 113 is patterned to overlap with the gate lines 109 and the data lines 111 and to cover the TFTs 131. The layer 113 serves as an upper light-shielding layer. The layer 113 is entirely covered with a third interlayer dielectric layer 114.

[0016] Pixel electrodes 115, which have an approximately rectangular plan shape, are formed on the third interlayer dielectric layer 114. The electrodes 115 are located in corresponding pixel areas 120 defined by the gate lines 109 and the data lines 111. The electrodes 115 are mechanically contacted with and electrically connected to the drain regions 107e of the corresponding TFTs 131 by way of contact holes 122 that penetrate the third interlayer dielectric layer 114, the second interlayer dielectric layer 112, the first interlayer dielectric layer 110, and the gate dielectric layer 108.

[0017] With a prior-art LCD device including the prior-art TFT array substrate 100 having the above-described structure, an opposite substrate (not shown) is coupled with the substrate 100 to form a liquid-crystal layer between these two substrates. The light entering the LCD device from the side of the opposite substrate is blocked by the black matrix layer (i.e., the upper light-shielding layer) 113. The light entering from the side of the TFT array substrate 100 is blocked by the lower light-shielding layer 103. However, there is a problem that the light entering from the side of the substrate 100 is unable to sufficiently prevent

being irradiated to the LDD regions 107b and 107b and/or the channel region 107c of the TFT 131. This is explained in more detail below with reference to Fig. 3.

[0018] As shown in Fig. 3, the light L101 entering the LCD device from the side of the opposite substrate is blocked by the black matrix layer (i.e., the upper light-shielding layer) 113. Alternately, the light L101 penetrates the substrate 100 without reflection by the lower light-shielding layer 103. This is because the widths of the layers 113 and 103 and the interval between the layers 113 and 103 are well adjusted for this purpose. The light L102 entering the LCD device from the side of the substrate 100 is blocked by the lower light-shielding layer 103.

[0019] However, as seen from Fig. 3, the light L103 entering the LCD device from the side of the TFT array substrate 100 toward the black matrix layer 113 is reflected by the layer 113 to go to the lower light-shielding layer 103. Then, the light L103 travels the space between the layer 103 and the data line 111 through multiple reflections and finally, it reaches the LDD region 107b. Moreover, the light L104 entering the LCD device from the side of the substrate 100 toward the data line 111 travels the space between the layer 103 and the data line 111 through multiple reflections and finally, it reaches the LDD region 107b. Similarly, light is irradiated to the LDD region 107d after multiple reflections. Practically, various light including the light L103 and L104 enters from the side of the substrate 100 and thus, the light is irradiated to the channel region 107c.

[0020] To avoid this problem, various improvements have ever been developed and disclosed.

[0021] For example, the Japanese Non-Examined Patent Publication No. 2000-180899 published in June 2000 discloses a LCD device, in which the ends of the lower light-shielding layer are tapered to form a trapezoidal cross section. In this device, if the width of the lower light-shielding layer and the width of the data line are well adjusted, light entering the LCD device from the side of the TFT array substrate is blocked by the lower light-shielding layer and thus, the light is prevented from being irradiated to the channel region.

[0022] The Japanese Non-Examined Patent Publication No. 2000-356787 published in December 2000 discloses a LCD device, in which dummy contact holes are formed near the channel region in the dielectric layer that covers the lower light-shielding layer. The dummy contact holes are filled with a wiring material. In this device, the wiring material filled in the dummy contact holes block the light entering the LCD device from the side of the TFT array substrate and thus, the light is prevented from being irradiated to the channel region.

Additionally, as already known, the black matrix layer may be placed on the TFT array substrate or the opposite substrate. If the black matrix layer is placed on the opposite substrate, an alignment error (i.e., allowance) of approximately 10 μm needs to be considered in ad-

vance in the coupling process of the TFT array substrate and the opposite substrate, while taking the typical overlay accuracy between these two substrates into consideration. As a result, the black matrix layer needs to be larger in width. This leads to a disadvantage that the aperture ratio is unable to be increased.

[0023] Unlike this, if the black matrix layer is placed on the TFT array substrate, the alignment accuracy between the black matrix layer and the TFTs can be raised by utilizing the known fabrication processes of semiconductor devices. Therefore, as shown in Figs. 1, 2A, and 2B, this structure is becoming a main stream.

[0024] As explained above, with the prior-art LCD device having the prior-art TFT array substrate 100 of Figs. 1 and 2A to 2B, part of the light entering the LCD device from the side of the substrate 100 is likely to reach the LDD regions 107b and 107d and/or the channel region 107c. Thus, optically induced current leakage increases and as a result, a problem of degradation of contrast and non-uniformity of image quality occurs.

[0025] With the LCD device disclosed by the Publication No. 2000-180899, the process step of forming the tapered ends of the lower light-shielding layer is required. Therefore, there is a problem that the fabrication processes are complicated.

[0026] With the LCD device disclosed by the Publication No. 2000-356787, the process step of forming the dummy contact holes near the channel region in the dielectric layer that covers the lower light-shielding layer and the process step of filling the dummy contact holes with the wiring material, as required. Therefore, there is a problem that the fabrication processes are complicated, which is the same as that of the Publication No. 2000-180899.

[0027] Furthermore, with the LCD devices disclosed by the Publication Nos. 2000-180899 and 2000-356787, if these devices are applied to the light bulb for high-luminance projection-type display devices, it is difficult to effectively and sufficiently block the light traveling toward the active layer of the TFT.

SUMMARY OF THE INVENTION

[0028] Accordingly, an object of the present invention is to provide a TFT array substrate and a LCD device that effectively block the light traveling toward the active layers of the TFTs.

[0029] Another object of the present invention is to provide a TFT array substrate and a LCD device that suppress the optically induced current leakage in the TFTs.

[0030] Still another object of the present invention is to provide a TFT array substrate and a LCD device that improve the contrast and uniformity of image quality.

[0031] A further object of the present invention is to provide a TFT array substrate and a LCD device that can be fabricated easily without complicated process steps.

[0032] The above objects together with others not specifically mentioned will become clear to those skilled in the art from the following description.

[0033] According to a first aspect of the invention, a TFT array substrate is provided, which comprises:

(a) a transparent plate;
(b) TFTs arranged on the plate in a matrix array with rows and columns;
each of the TFTs having a first source/drain region, a second source/drain region, and an active layer;
(c) gate lines formed on the plate in such a way as to extend along the rows of the matrix;
(d) data lines formed on the plate in such a way as to extend along the columns of the matrix;
each of the data lines being electrically connected to corresponding ones of the TFTs at their first source/drain regions;
(e) pixel electrodes formed in pixel areas on the plate;
each of the pixel electrodes being electrically connected to corresponding ones of the TFTs at their second source/drain regions;
(f) a patterned first light-shielding layer formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs;
(g) a patterned second light-shielding layer formed between the first light-shielding layer and the TFTs;
the second light-shielding layer having light-absorbing properties;
(h) a patterned third light-shielding layer formed to cover the TFTs on an opposite side to the plate with respect to the TFTs;
the third light-shielding layer having first parts extending along the rows of the matrix and second parts extending along the columns thereof.

[0034] With the TFT array substrate according to the first aspect of the invention, the patterned first light-shielding layer is formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs. The patterned third light-shielding layer is formed to cover the TFTs on the opposite side to the plate with respect to the TFTs. The third light-shielding layer has first parts extending along the rows of the matrix and second parts extending along the columns thereof. Moreover, the patterned second light-shielding layer is formed between the first light-shielding layer and the TFTs. The second light-shielding layer has light-absorbing properties.

[0035] Therefore, even if light entering the inside of the TFT array substrate from the side of the plate is reflected by the third patterned light-shielding layer and/or the data lines and then, it is reflected by the first patterned light-shielding layer, the whole reflected light will reach the patterned second light-shielding layer. Since the second light-shielding layer has light-absorbing

properties the reflected light will be absorbed by the second light-shielding layer. Thus, any light traveling toward the active layers of the TFTs in the TFT array substrate is effectively blocked. This means that the active layers are not exposed to the light. As a result, the optically induced current leakage in the TFTs is suppressed, thereby improving the contrast and uniformity of image quality.

[0036] Moreover, the complicated fabrication process steps as disclosed in the Japanese Non-Examined Patent Publication Nos. 2000-180899 and 2000-356787 are unnecessary. Thus, the TFT array substrate can be fabricated easily without complicated process steps.

[0037] In a preferred embodiment of the substrate according to the first aspect of the invention, each of the TFTs has a channel region and a LDD region. The second light-shielding layer has first parts covering the channel regions of the TFTs and second parts covering the LDD regions thereof. In this embodiment, there is an additional advantage that the light traveling toward the channel regions and the LDD regions is certainly blocked. In general, irradiation of light to the channel region or the LDD region will induce current leakage. Thus, current leakage can be effectively reduced by blocking or suppressing the light.

[0038] In another preferred embodiment of the substrate according to the first aspect of the invention, the second light-shielding layer is made of a material including silicon. More preferably, the second light-shielding layer is made of silicon. In this embodiment, there is an additional advantage that current leakage is suppressed more efficiently.

[0039] In yet another preferred embodiment of the substrate according to the first aspect of the invention, the second light-shielding layer has conductivity. The second light-shielding layer has a structure that allows application of a constant voltage. In this embodiment, there is an additional advantage that the second light-shielding layer can be biased at a desired potential and that the characteristic of the TFT can be controlled.

[0040] In a further preferred embodiment of the substrate according to the first aspect of the invention, the second light-shielding layer has conductivity and is connected electrically to the gate lines. In this embodiment, there is an additional advantage that the TFTs have a dual-gate structure having an improved on/off characteristic.

[0041] In yet a further preferred embodiment of the substrate according to the first aspect of the invention, the second light-shielding layer is made of silicon doped with an impurity. In this embodiment, there is an additional advantage that desired conductivity can be easily given to the second light-shielding layer.

[0042] Preferably, the gate lines are arranged in such a way as to overlap with the channel regions of the corresponding TFTs. The gate lines have a function of gate electrodes of the TFTs at their overlapping parts.

[0043] Preferably, gate electrodes are formed for the respective TFTs separately from the gate lines. The gate lines are electrically connected to the corresponding gate electrodes.

[0044] In yet a further preferred embodiment of the substrate according to the first aspect of the invention, a dielectric sandwiched by the second light-shielding layer and the active layers of the TFTs has a thickness ranging from 100 nm to 500 nm. In this embodiment, the light shielding effect of the invention is ensured. More preferably, the dielectric thickness ranges from 150 nm to 300 nm. In this case, the light-shielding effect of the invention is enhanced.

[0045] In yet a further preferred embodiment of the substrate according to the first aspect of the invention, a driver circuit section including TFTs is provided in addition to a pixel matrix section where the TFTs are arranged in a matrix array. The second light-shielding layer is provided for the TFTs in the pixel matrix section while the second light-shielding layer is not provided for the TFTs in the driver circuit section. In this embodiment, the second light-shielding layer is provided for the TFTs in the pixel matrix section and the second light-shielding layer is not provided for the TFTs in the driver circuit section Therefore, if laser light is irradiated to amorphous silicon layers designed for the active layers of the TFTs in the pixel matrix section and the driver circuit section in a laser annealing process, the laser-inducing heat will propagate more quickly into the vicinities of the amorphous silicon layers by way of the second light-shielding layer in the pixel matrix section than that in the driver circuit section. As a result, the amorphous silicon layers in the pixel matrix section are turned to polysilicon layers with low crystallinity. This means that optically induced current leakage is further suppressed. At the same time as this, the amorphous silicon layers in the driver circuit section are turned to polysilicon layers with high mobility.

[0046] According to a second aspect of the invention, an active-matrix addressing LCD device is provided, which comprises:

(a) the TFT array substrate according to the first aspect;
(b) an opposite substrate located to be opposite to the TFT array substrate; and
(c) a liquid-crystal layer formed between the TFT array substrate and the opposite substrate.

[0047] With the active-matrix addressing LCD device according to the second aspect of the invention, the same advantages as those shown in the TFT array substrate according to the first aspect of the invention are obtainable because of the same reason as above.

[0048] According to a third aspect of the invention, another TFT array substrate is provided, which comprises:

(a) a transparent plate;
(b) TFTs arranged on the plate in a matrix array with

rows and columns;

each of the TFTs having a first source/drain region, a second source/drain region, and an active layer;

(c) gate lines formed on the plate in such a way as to extend along the rows of the matrix;

(d) data lines formed on the plate in such a way as to extend along the columns of the matrix;

each of the data lines being electrically connected to corresponding ones of the TFTs at their first source/drain regions;

(e) pixel electrodes formed in pixel areas on the plate;

each of the pixel electrodes being electrically connected to corresponding ones of the TFTs at their second source/drain regions;

(f) a patterned first light-shielding layer formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs;

(g) a patterned third light-shielding layer formed to cover the TFTs on an opposite side to the plate with respect to the TFTs;

the third light-shielding layer having first parts extending along the rows of the matrix and second parts extending along the columns thereof; and

(h) a patterned fourth light-shielding layer formed between the TFTs and the third light-shielding layer;

the fourth light-shielding layer having light-absorbing properties.

[0049] With the TFT array substrate according to the third aspect of the invention, the patterned first light-shielding layer is formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs. The patterned third light-shielding layer is formed to cover the TFTs on the opposite side to the plate with respect to the TFTs. The third light-shielding layer has first parts extending along the rows of the matrix and second parts extending along the columns thereof, Moreover, the patterned fourth light-shielding layer is formed between the TFTs and the third light-shielding layer. The fourth light-shielding layer has light-absorbing properties.

[0050] Therefore, even if light entering the inside of the TFT array substrate from the side of the plate is reflected by the third patterned light-shielding layer and/or the data lines and then, it is reflected by the first patterned light-shielding layer, the whole reflected light will reach the patterned fourth light-shielding layer. Since the fourth light-shielding layer has light-absorbing properties the reflected light will be absorbed by the fourth light-shielding layer. Thus, any light traveling toward the active layers of the TFTs in the TFT array substrate is effectively blocked. This means that the active layers are not exposed to the light. As a result, the optically induced current leakage in the TFTs is suppressed, thereby improving the contrast and uniformity of image quality.

[0051] Moreover, the complicated fabrication process steps as disclosed in the Japanese Non-Examined Patent Publication Nos. 2000-180899 and 2000-356787 are unnecessary. Thus, the TFT array substrate can be fabricated easily without complicated process steps.

[0052] In a preferred embodiment of the substrate according to the third aspect of the invention, each of the TFTs has a channel region and a LDD region. The fourth light-shielding layer has first parts covering the channel regions of the TFTs and second parts covering the LDD regions thereof. In this embodiment, there is an additional advantage that the light traveling toward the channel regions and the LDD regions is certainly blocked. In general, irradiation of light to the channel region or the LDD region will induce current leakage. Thus, current leakage can be effectively reduced by blocking or suppressing the light.

[0053] In another preferred embodiment of the substrate according to the third aspect of the invention, the fourth light-shielding layer is made of a material including silicon. More preferably, the fourth light-shielding layer is made of silicon. In this embodiment, there is an additional advantage that current leakage is suppressed more efficiently.

[0054] In yet another preferred embodiment of the substrate according to the third aspect of the invention, the fourth light-shielding layer has conductivity. The fourth light-shielding layer has a structure that allows application of a constant voltage. In this embodiment, there is an additional advantage that the fourth light-shielding layer can be biased at a desired potential and that the characteristic of the TFT can be controlled.

[0055] In a further preferred embodiment of the substrate according to the third aspect of the invention, the fourth light-shielding layer has conductivity and is electrically connected to the gate lines.

[0056] In yet a further preferred embodiment of the substrate according to the third aspect of the invention, the fourth light-shielding layer is made of silicon doped with an impurity. In this embodiment, there is an additional advantage that desired conductivity can be easily given to the fourth light-shielding layer.

[0057] Preferably, the gate lines are arranged in such a way as to overlap with the channel regions of the corresponding TFTs. The gate lines have the function of gate electrodes of the TFTs at their overlapping parts.

[0058] Preferably, gate electrodes are formed for the respective TFTs separately from the gate lines. The gate lines are electrically connected to the corresponding gate electrodes.

[0059] In yet a further preferred embodiment of the substrate according to the third aspect of the invention, a patterned second light-shielding layer is additionally formed between the first light-shielding layer and the TFTs. The second light-shielding layer has light-absorbing properties. In this embodiment, the light is blocked at each side of the TFTs and therefore, very high light-shielding effect is obtainable.

[0060] In yet a further preferred embodiment of the substrate according to the third aspect of the invention, a dielectric sandwiched by the second light-shielding layer and the active layers of the TFTs has a thickness ranging from 100 nm to 500 nm. In this embodiment, the light shielding effect of the invention is ensured. More preferably, the dielectric thickness ranges from 150 nm to 300 nm. In this case, the light shielding effect of the invention is enhanced.

[0061] In yet a further preferred embodiment of the substrate according to the third aspect of the invention, a driver circuit section including TFTs is provided in addition to a pixel matrix section where the TFTs are arranged in a matrix array. The second light-shielding layer is provided for the TFTs in the pixel matrix section while the second light-shielding layer is not provided for the TFTs in the driver circuit section. In this embodiment, the second light-shielding layer is provided for the TFTs in the pixel matrix section and the second light-shielding layer is not provided for the TFTs in the driver circuit section. Therefore, if laser light is irradiated to amorphous silicon layers designed for the active layers of the TFTs in the pixel matrix section and the driver circuit section in a laser annealing process, the laser-inducing heat will propagate more quickly into the vicinities of the amorphous silicon layers by way of the second light-shielding layer in the pixel matrix section than that in the driver circuit section. As a result, the amorphous silicon layers in the pixel matrix section are turned to polysilicon layers with low crystallinity. This means that optically induced current leakage is further suppressed. At the same time as this, the amorphous silicon layers in the driver circuit section are turned to polysilicon layers with high mobility.

[0062] According to a fourth aspect of the invention, another active-matrix addressing LCD device is provided, which comprises:

(a) the TFT array substrate according to the third aspect;
(b) an opposite substrate located to be opposite to the TFT array substrate; and
(c) a liquid-crystal layer formed between the TFT array substrate and the opposite substrate.

[0063] With the active-matrix addressing LCD device according to the fourth aspect of the invention, the same advantages as those shown in the TFT array substrate according to the third aspect of the invention are obtainable because of the same reason as above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0064] In order that the present invention may be readily carried into effect, it will now be described with reference to the accompanying drawings.

Fig. 1 is a partial plan view showing the layout of a prior-art TFT array substrate.
Fig. 2A is a partial, cross-sectional view along the line IIA-IIA in Fig. 1, which shows the structure of the prior-art substrate of Fig. 1.
Fig. 2B is a partial, cross-sectional view along the line IIB-IIB in Fig. 1, which shows the structure of the prior-art substrate of Fig. 1.
Fig. 3 is a schematic cross-sectional view showing the effect to block the light entering the inside of the prior-art substrate of Fig. 1, which is along the line IIA-IIA in Fig. 1.
Fig. 4 is a partial plan view showing the layout of a TFT array substrate according to the first embodiment of the invention.
Fig. 5A is a partial, cross-sectional view along the line VA-VA in Fig. 4, which shows the structure of the substrate of Fig. 4.
Fig. 5B is a partial, cross-sectional view along the line VB-VB in Fig. 4, which shows the structure of the substrate of Fig. 4.
Fig. 6 is a schematic cross-sectional view showing the effect to block the light entering the inside of the substrate of Fig. 4, which is along the line VA-VA in Fig. 4.
Figs. 7A to 11A are partial, cross-sectional views along the line VA-VA in Fig. 4, respectively, which show the process steps of fabricating the substrate of Fig. 4.
Figs. 7B to 11B are partial, cross-sectional views along the line VB-VB in Fig. 4, respectively, which show the process steps of fabricating the substrate of Fig. 4.
Fig. 12 is a partial plan view showing the layout of a TFT array substrate according to the second embodiment of the invention.
Fig. 13A is a partial, cross-sectional view along the line XIIIA-XIIIA in Fig. 12, which shows the structure of the substrate of Fig. 12.
Fig. 13B is a partial, cross-sectional view along the line XIIIB-XIIIB in Fig. 12, which shows the structure of the substrate of Fig. 12.
Fig. 14 is a partial plan view showing the layout of a TFT array substrate according to the third embodiment of the invention.
Fig. 15 is a partial plan view showing the layout of a TFT array substrate according to the fourth embodiment of the invention.
Fig. 16A is a partial, cross-sectional view along the line XVIA-XVIA in Fig. 15, which shows the structure of the substrate of Fig. 15.
Fig. 16B is a partial, cross-sectional view along the line XVIB-XVIB in Fig. 15, which shows the structure of the substrate of Fig. 15.
Fig. 17 is a schematic cross-sectional view showing the effect to block the light entering the inside of the substrate of Fig. 15, which is along the line XVIA-XVIA in Fig. 15.
Fig. 18 is a partial plan view showing the layout of

a TFT array substrate according to the fifth embodiment of the invention.

Fig. 19 is a partial plan view showing the layout of a TFT array substrate according to the sixth embodiment of the invention.

Fig. 20 is a schematic cross-sectional view showing the structure of an active-matrix addressing LCD device using the TFT array substrate according to the invention.

Fig. 21A is a partial, cross-sectional view along the line VA-VA in Fig. 4, which shows the structure of a TFT array substrate according to the seventh embodiment of the invention.

Fig. 21B is a partial, cross-sectional view along the line VB-VB in Fig. 4, which shows the structure of the substrate of Fig. 21A.

Fig. 22A is a partial, cross-sectional view along the line VA-VA in Fig. 4, which shows the structure of a TFT array substrate according to the eighth embodiment of the invention.

Fig. 22B is a partial, cross-sectional view along the line VB-VB in Fig. 4, which shows the structure of the substrate of Fig. 22A.

Fig. 23A is a partial, cross-sectional view along the line XVIA-XVIA in Fig. 15, which shows the structure of a TFT array substrate according to the ninth embodiment of the invention.

Fig. 23B is a partial, cross-sectional view along the line XVIB-XVIB in Fig. 15, which shows the structure of the substrate of Fig. 23A.

Fig. 24A is a partial, cross-sectional view along the line XVIA-XVIA in Fig. 15, which shows the structure of a TFT array substrate according to the tenth embodiment of the invention.

Fig. 24B is a partial, cross-sectional view along the line XVIB-XVIB in Fig. 15, which shows the structure of the substrate of Fig. 24A.

Fig. 25 shows a graph showing the relationship of the optically induced current leakage of the TFTs provided in the pixel matrix section with the dielectric layer thickness between the active layer and the second light-shielding layer, which was obtained under a specific irradiation condition of projection light.

Fig. 26 is a schematic plan view of a TFT array substrate according to the eleventh embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMETNS

[0065] Preferred embodiments of the present invention will be described in detail below while referring to the drawings attached.

FIRST EMBODIMENT

[0066] Fig. 4 and Figs. 5A and 5B show the schematic configuration of a TFT array substrate 30 according to the first embodiment of the invention, in which only one pixel is illustrated for simplification. This is applicable to any other embodiments explained later.

[0067] The TFT array substrate 30 comprises a transparent plate 1, on which TFTs 31 are arranged in a matrix array. The plate 1 is made of transparent and dielectric material such as glass.

[0068] A SiO_2 layer 2 is formed on the plate 1 to cover its whole surface. This layer 2 is to prevent heavy metals contained in the plate 1 from diffusing into the inside of the substrate 30.

[0069] A patterned first light-shielding layer 3 is formed on the SiO_2 layer 2. The plan shape of the layer 3 is like a lattice, which is formed by lateral strips 3a extending along the rows (the X direction in Fig. 4) of the matrix of the TFTs 31 and vertical strips 3b extending along the columns (the Y direction in Fig. 4) thereof and intersecting with the lateral ones. The layer 3 is made of a material having a sufficiently low optical transmittance (e.g.., WSi_2). The thickness of the layer 3 is set to be large enough for blocking light entering directly from the back side of the substrate 30, i.e., from the side of the plate 1. The whole layer 3 is covered with an overlying SiO_2 layer 4.

[0070] On the SiO_2 layer 4, a patterned second light-shielding layer 5 is formed. The layer 5 is made of amorphous silicon having a light-absorbing property. The layer 5 comprises lateral strip-shaped parts 5a extending along the rows (the X direction in Fig. 4) of the matrix of the TFTs 31 and vertical rectangular parts 5b extending along the columns (the Y direction in Fig. 4) thereof and intersecting with the lateral parts 5a. The strip-shaped parts 5a are arranged vertically (in the Y direction) at equal intervals, which are parallel to each other. The rectangular parts 5b are arranged horizontally (in the X direction) at equal intervals, which are parallel to each other. The layer 5 is patterned to entirely overlap with the underlying first light-shielding layer 3, The layer 5 is covered with a SiO_2 layer 6 formed on the SiO_2 layer 4.

[0071] On the SiO_2 layer 6, polysilicon layers 7 are formed. Each of the layers 7 is patterned to have a plan shape of approximately L character. Each of the layers 7 is located at a position right below the intersection of a gate line 9 and a data line 11, which are explained later. The layer 7 serves as the active layer of each TFT 31.

[0072] Each of the polysilicon active layers 7 comprises an undoped channel region 7c, two lightly-doped LDD regions 7b and 7d, a heavily-doped source region 7a, and a heavily-doped drain region 7e. The source and drain regions 7a and 7e are located at each side of the channel region 7c. The LDD region 7b is located between the source region 7a and the channel region 7c. The LDD region 7d is located between the channel region 7c and the drain region 7e.

[0073] The source region 7a, the LDD region 7b, the channel region 7c, the LDD region 7d, and the drain re-

gion 7e are arranged along the Y direction in such a way as to overlap with the first and second light-shielding layers 3 and 5. Part of the drain region 7e is extended in the X direction.

[0074] A gate dielectric layer 8 is formed on the SiO_2 layer 6 to cover the underlying active layers 7.

[0075] Gate lines 9, which are made of impurity-doped polysilicon or silicide, are formed on the gate dielectric layer 8. These lines 9 are parallel to each other and extend in the X direction. Each of the lines 9 is located to overlap with the channel regions 7c of the TFTs 31 that belong to the same row of the matrix. The parts of the line 9 placed right over the regions 7c serve as gate electrodes of the corresponding TFTs 31. The lines 9 are entirely covered with a first interlayer dielectric layer 10 formed on the layer 8.

[0076] Data lines 11, which are made of Al, are formed on the first interlayer dielectric layer 10. These lines 11 are parallel to each other and extend in the Y direction. Each of the lines 11 is located to overlap with the active layers 7 of the TFTs 31 that belong to the same column of the matrix. The line 11 entirely covers the source regions 7a, the channel regions 7c, and the LDD regions 7b and 7d of the corresponding TFTs 31. The line 11 covers parts of the drain regions 7e of the corresponding TFTs 31. The line 11 is mechanically contacted with and electrically connected to the source regions 7a of the TFTs 31 that belong to the same row of the matrix by way of contact holes 21 that penetrate the first interlayer dielectric layer 10 and the gate dielectric layer 8. The lines 11 are entirely covered with a second interlayer dielectric layer 12.

[0077] A patterned black matrix layer 13, which is made of Cr, is formed on the second interlayer dielectric layer 12. The plan shape of the layer 13 is like a lattice, which is formed by lateral strips extending along the rows (the X direction in Fig. 4) of the matrix and vertical strips extending along the columns (the Y direction in Fig. 4) thereof and intersecting with the lateral ones. The layer 13 is patterned to overlap with the gate lines 9 and the data lines 11 and to cover the TFTs 31. The layer 13 serves as a third light-shielding layer. The layer 13 is entirely covered with a third interlayer dielectric layer 14 formed on the layer 12.

[0078] Pixel electrodes 15, which have an approximately rectangular plan shape, are formed on the third interlayer dielectric layer 14. The electrodes 15 are located in corresponding pixel areas 20 defined by the gate lines 9 and the data lines 11. The electrodes 15 are mechanically contacted with and electrically connected to the drain regions 7e of the corresponding TFTs 31 by way of contact holes 22 that penetrate the third interlayer dielectric layer 14, the second interlayer dielectric layer 12, the first interlayer dielectric layer 10, and the gate dielectric layer 8.

[0079] Fig. 20 shows the structure of an active-matrix addressing LCD device 50, which includes the TFT array substrate 51 having the structure according to the first embodiment. An opposite substrate 52 is coupled with the substrate 51 to form a liquid crystal layer 54 therebetween with a sealing member 53. In the layer 54, an alignment layer 55 is formed on the substrate 51 and an alignment layer 56 is formed on the substrate 52. A polarizer plate 57 is provided on the substrate 52. A back light 58 is provided near the substrate 51.

[0080] With the active-matrix addressing LCD device 50, as shown in Fig. 6, the light L1 entering the device 50 from the side of the opposite substrate 52 is blocked by the black matrix layer (i.e., the third light-shielding layer) 13. Alternately, the light L1 penetrates the substrate 30 without reflection by the first light-shielding layer 3. This is because the widths of the layers 13 and 3 and the interval between the layers 13 and 3 are well adjusted for this purpose.

[0081] On the other hand, the light L2 entering the device 50 from the side of the TFT array substrate 30 (51) is blocked by the first light-shielding layer 3. The light L3 entering the device 50 from the side of the substrate 30 toward the black matrix layer 13 is reflected by the layer 13 to go to the first light-shielding layer 3. Then, the light L3 reaches the second light-shielding layer 5 located between the layer 3 and the TFTs 31. Alternately, the light L3 is reflected by the layer 13 and 3 and then, the light L3 reaches the second light-shielding layer 5. Moreover, the light L4 entering the device 50 from the side of the substrate 30 toward the data line 11 is reflected by the line 11 and finally, it reaches the layer 5.

[0082] As explained above, the second light-shielding layer 5 is made of amorphous Si having light-absorbing properties Thus, light L1 to L4 is absorbed by the layer 5.

[0083] In this way, even if light traveling from the side of the plate 1 is directly inputted into the inner space between the first light-shielding layer 3 and the data lines 11 or indirectly inputted into the same by way of reflection by the third patterned light-shielding layer (i. e., the black matrix layer) 13, the light will be absorbed by the second light-shielding layer 5. Thus, any light traveling toward the channel region 7c and the LDD regions 7b and 7d of each TFT 31 is blocked effectively and certainly.

[0084] In addition, the channel region 7c of each TFT 31 is covered with the corresponding one of the gate lines 9 and therefore, the effect to block the light traveling toward the region 7c is enhanced.

[0085] Generally, the silicon layer has a spectral light-absorption characteristic that the light-absorption rate is relatively high for the wavelength range of green and blue and relatively low for the wavelength range of red. This is applicable to the amorphous Si for forming the second light-shielding layer 5 and polysilicon layer for forming the active layer 7. As already know the current leakage of the TFTs 31 is induced by absorption of light in the polysilicon active layer 7 and therefore, the magnitude or quantity of the currant leakage varies depending on the wavelength of light to be irradiated. As a result, by making the second light-shielding layer 5 of

amorphous silicon whose spectral absorption characteristic is similar in tendency to that of polysilicon, the current leakage can be efficiently suppressed or decreased.

[0086] when high-luminance light is inputted into the TFT array substrate 30, the temperature of the vicinity of the TFT 31 will rise due to the heat generated by absorption of light in the second light-shielding layer 5. As described above, the absorption rate of the layer 5 is relatively lower for the wavelength range of red. Therefore, there is an additional advantage that the temperature rise occurring in the vicinity of the TFT 31 is suppressed further.

[0087] Instead of amorphous Si, microcrystalline silicon or polysilicon, or silicide including Si may be used for the same purpose. Substantially the same advantages as those of amorphous Si are obtainable.

[0088] Next, a method of fabricating the TFT array substrate 30 according to the first embodiment of Figs. 4 and 5A to 5B is explained below with reference to Figs. 7A to 11A and 7B to 11B.

[0089] First, as shown in Figs. 7A and 7B, by a known CVD (Chemical Vapor Deposition) process, the SiO_2 layer 2 is formed on the transparent plate 1. Then, a tungsten silicide (WSi_2) layer (not shown) is formed on the SiO_2 layer 2. The WSi_2 layer thus formed is patterned to form the first light-shielding layer 3 with known photolithography and etching techniques. Thereafter, the SiO_2 layer 4 is formed on the SiO_2 layer 2 by a CVD process to cover the whole layer 3.

[0090] Next, an amorphous Si layer (not shown) is deposited on the SiO_2 layer 4 by a Low-Pressure CVD (LPCVD) or plasma-Enhanced CVD (PECVD) process. The SiO_2 layer thus formed is patterned with known photolithography and etching techniques, thereby forming the second light-shielding layer 5 on the layer 4.

[0091] Thereafter, as shown in Figs. 8A and 8B, the SiO_2 layer 6 is deposited on the SiO_2 layer 4 by a CVD process to cover the second light-shielding layer 5. An amorphous Si layer (not shown) is deposited on the layer 6 by a LPCVD or PECVD process. The amorphous Si layer thus deposited is crystallized by a laser annealing method. The Si layer thus crystallized is patterned with known photolithography and etching techniques, thereby forming the polysilicon active layers 7 of the TFTs 31 on the layer 6.

[0092] Subsequently, as shown in Figs. 9A and 9B, the SiO_2 layer (i.e., the gate dielectric layer) 8 is deposited on the SiO_2 layer 6 by a CVD process to cover the polysilicon active layers 7. An impurity-doped polysilicon layer (not shown) and a silicide layer (not shown) are successively deposited on the gate dielectric layer 8 and then, they are patterned with known photolithography and etching techniques, thereby forming the gate lines 9.

[0093] Using the gate lines 9 thus formed as a mask, an impurity is selectively doped into the polysilicon active layers 7 at a low doping concentration. Then, using a patterned photoresist mask (not shown), an impurity is selectively doped into the polysilicon active layers 7 at a high doping concentration. Thus, the source regions 7a, the LDD regions 7b and 7d, the channel regions 7c, and the drain regions 7e are formed in the layers 7.

[0094] Following this, as shown in Figs. 10A and 10B, a SiO_2 layer serving as the first interlayer dielectric layer 10 is deposited on the gate dielectric layer 8 by a CVD process to cover the gate lines 9. Then, with known photolithography and etching techniques, the first interlayer dielectric layer 10 and the gate dielectric layer 8 are selectively removed, thereby forming the contact holes 21 that expose the source regions 7a.

[0095] An Al layer (not shown) is deposited by a sputtering process and patterned with known photolithography and etching techniques, thereby forming the data lines 11. The lines 11 are contacted with the source regions 7a by way of the holes 21. Thus, the lines 11 are electrically connected to the regions 7a.

[0096] As shown in Figs. 11A and 11B, a SiO_2 layer serving as the second interlayer dielectric layer 12 is deposited on the first interlayer dielectric layer 10 by a CVD process to cover the data lines 11. Then, a Cr layer (not shown) is deposited on the layer 12 by a sputtering process and then, it is patterned with known photolithography and etching techniques, thereby forming the black matrix layer 13 serving as the third light-shielding layer.

[0097] Thereafter, a SiO_2 layer serving as the third interlayer dielectric layer 14 is deposited on the second interlayer dielectric layer 12 by a CVD process to cover the black matrix layer 14.

[0098] With known photolithography and etching techniques, the third interlayer dielectric layer 14, the second interlayer dielectric layer 12, the first interlayer dielectric layer 10, and the gate dielectric layer 8 are selectively removed, thereby forming the contact holes 22 that expose the drain regions 7e. Then, an ITO (Indium Tin Oxide) layer (not shown) is deposited on the layer 14 and then, it is patterned with known photolithography and etching techniques, thereby forming the pixel electrodes 15. The electrodes 15 are contacted with the drain regions 7e by way of the holes 22. Thus, the electrodes 15 are electrically connected to the regions 7e.

[0099] Through the above-described process steps, the TFT array substrate 30 shown in Figs. 1 and 2A to 2B is formed. As seen from this easily, the fabrication process steps of the substrate 30 are simple and include no complicated steps. As a result, the substrate 30 can be fabricated easily.

[0100] With the TFT array substrate 30 according to the first embodiment of the invention, the patterned first light-shielding layer 3 is formed between the plate 1 and the TFTs 31 in such a way as to overlap with the active layers o7 f the TFTs 31. The patterned third light-shielding (i.e. the black matrix) layer 13 is formed to cover the TFTs 31 on the opposite side to the plate 1 with respect to the TFTs 31. The third light-shielding layer 13 has first parts extending along the rows of the matrix and second

parts extending along the columns thereof. Moreover, the patterned second light-shielding layer 5 is formed between the first light-shielding layer 3 and the TFTs 31. The layer 5 has light-absorbing properties.

[0101] Therefore, even if light entering the inside of the TFT array substrate 30 from the side of the plate 1 is reflected by the third patterned light-shielding layer 13 and/or the data lines 11 and then, it is reflected by the first patterned light-shielding layer 3, the whole reflected light will reach the patterned second light-shielding layer 5. Since the second light-shielding layer 5 has light-absorbing properties the reflected light will be absorbed by the layer 5. Thus, any light traveling toward the active layers 7 of the TFTs 31 in the substrate 30 is effectively blocked. This means that the active layers 7 are not exposed to the light. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality.

[0102] Moreover, the complicated fabrication process steps as disclosed in the Japanese Non-Examined Patent Publication Nos. 2000-180899 and 2000-356787 are unnecessary. Thus, the substrate 30 can be fabricated easily without complicated process steps.

[0103] The dielectric layer thickness between the first light-shielding layer 3 and the second light-shielding layer 5 and the dielectric layer thickness between the second light-shielding layer 5 and the active layers 7 are important parameters for the present invention. In particular, the dielectric layer thickness between the second light-shielding layer 5 and the active layers 7 is more important. The smaller the dielectric layer thickness between the second light-shielding layer 5 and the active layers 7, the higher the light-shielding effect. According to the inventors' test, it was found that the light-shielding effect was striking when the dielectric layer thickness between the layers 5 and 7 was set at 500 nm or less.

[0104] Moreover, the inventors found that if the dielectric layer thickness between the second light-shielding layer 5 and the active layers 7 was small, the transistor characteristics of the TFTs 31 were affected, and the laser annealing process to crystallize amorphous silicon layers designed for the active layers 7 was affected as well. Therefore, to get the light-shielding effect of the invention, they found that the dielectric layer thickness between the layers 5 and 7 was preferably set in the range from 500 nm to 100 nm, and more preferably in the range from 300 nm to 150 nm. This is applicable to the other embodiments of the invention explained below.

SECOND EMBODIMENT

[0105] Figs. 12 and 13A to 13B show the structure of a TFT array substrate 30A according to the second embodiment of the invention, in which only one pixel is illustrated for simplification.

[0106] The substrate 30A of the second embodiment has the same configuration as the substrate 30 of the first embodiment, except that a second light-shielding layer 5A has conductivity and electrically connected to the corresponding gate lines 9. Therefore, the explanation about the same configuration is omitted here for the sake of simplification by attaching the same reference symbols as used in the first embodiment of Figs. 4 and 5A to 5B to the same or corresponding elements in the second embodiment of Figs. 12 and 13A and 13B.

[0107] In the substrate 30A, the second light-shielding layer 5A, which is made of an impurity-doped polysilicon, is formed on the SiO_2 layer 4. The layer 5A has strip-shaped first parts 5Aa extending along the rows of the matrix (i.e., in the X direction) and rectangular second parts 5Ab extending along the columns of the matrix (i.e., in the Y direction). The first parts 5Aa are parallel to each other. The layer 5A is formed in such a way as to overlap with the first light-shielding layer 3. The second parts 5Ab are overlapped with the respective polysilicon active layers 7.

[0108] The second light-shielding layer 5A is electrically connected to the corresponding gate lines 9 by way of internal wiring lines 41. Therefore, parts of the gate lines 9 serve as first gate electrodes of the TFTs 31 and at the same time, the layer 5A serves as the common second gate electrode thereof. This means that the TFTs 31 serve as dual-gate Field-Effect Transistors (FETs).

[0109] In this way, with the substrate 30A of the second embodiment, the second light-shielding layer 5A is used as the common second gate electrode and therefore, the inter-electrode capacitance of the TFTs 31 increases. To suppress the increase of the inter-electrode capacitance, the length L of the second part 5Ab in the Y direction is decreased compared with the first embodiment.

[0110] Specifically, the second part 5Ab of the second light-shielding layer 5A is overlapped with the channel region 7c, and the LDD regions 7b and 7d of the TFT 31 while it is scarcely overlapped with the source and drain regions 7a and 7e. Due to this structure, the increase of the inter-electrode capacitance of the TFT 31 can be suppressed at a level where practically no problem occurs while keeping the effect to block the light traveling toward the channel and LDD regions 7c, 7b, and 7d.

[0111] The substrate 30A is fabricated in substantially the same method as used in the first embodiment.

[0112] With the TFT array substrate 30A according to the second embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, any light traveling toward the active layers 7 of the TFTs 31 in the substrate 30A is effectively blocked. This means that the active layers 7 are not exposed to the light. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality. Moreover, the substrate 30A can be fabricated easily without complicated process steps.

[0113] The substrate 30A has an additional advantage that an improved on/off characteristic of the TFTs 31 is obtainable, because the TFTs 31 serve as dual-gate FETs.

THIRD EMBODIMENT

[0114] Figs. 14 and 15A to 15B show the structure of a TFT array substrate 30B according to the third embodiment of the invention, in which only one pixel is illustrated for simplification.

[0115] The substrate 30B of the third embodiment has the same configuration as the substrate 30 of the first embodiment, except that a second light-shielding layer 5B has conductivity and is applied with a constant voltage V_c. Therefore, the explanation about the same configuration is omitted here for the sake of simplification by attaching the same reference symbols as used in the first embodiment of Figs. 4 and 5A to 5B to the same or corresponding elements in the second embodiment of Figs. 14 and 15A and 15B.

[0116] In the substrate 30B, the second light-shielding layer 5B, which is made of an impurity-doped polysilicon, is formed on the SiO_2 layer 4. The layer 5B has strip-shaped first parts 5Ba extending along the rows of the matrix (i.e., in the X direction) and strip-shaped second parts 5Bb extending along the columns of the matrix (i.e., in the Y direction). The first parts 5Ba are parallel to each other and at the same time, the second parts 5Bb are parallel to each other. The first and second parts 5Ba and 5Bb are intersected with each other to form a lattice-shaped plan shape. The layer 5B is formed in such a way as to overlap with the first light-shielding layer 3. The second parts 5Bb are overlapped with the respective polysilicon active layers 7.

[0117] The second light-shielding layer 5B is electrically connected to an external terminal 51 through which a constant voltage V_c is supplied to the layer 5B. Thus, the layer 5B is biased at the voltage V_c. By adjusting the value of the voltage V_c, the characteristic of the TFT 31 can be controlled as desired.

[0118] The substrate 30B is fabricated in substantially the same method as used in the first embodiment.

[0119] With the TFT array substrate 30B according to the third embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, any light traveling toward the active layers 7 (especially, the channel region 7c and the LDD regions 7b and 7d) of the TFTs 31 in the substrate 30B is effectively blocked. This means that the active layers 7 are not exposed to the light. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality. Moreover, the substrate 30B can be fabricated easily without complicated process steps.

[0120] The substrate 30B has an additional advantage that the characteristic of the TFTs 31 is controllable by adjusting the value of the voltage VC applied to the second light-shielding layer 5B.

FOURTH EMBODIMENT

[0121] Figs. 15 and 16A to 16B show the structure of a TFT array substrate 30C according to the fourth embodiment of the invention, in which only one pixel is illustrated for simplification.

[0122] The substrate 30C of the fourth embodiment is obtained by applying the invention to the structure or form of the TFT array substrate where the TFTs 31 are not covered with the data lines 11.

[0123] Specifically, polysilicon active layers 7' of the TFTs 31 extend along the rows of the matrix. A patterned first light-shielding layer 3', a patterned second light-shielding layer 5C, and a patterned third light-shielding layer (i.e., a black matrix layer) 13' are formed in such a way as to overlap with the active layers 7'. The TFTs 31 have their respective gate electrodes 9a electrically connected to the gate lines 9.

[0124] In the substrate 30C, the first light-shielding layer 3', which is formed on the SiO_2 layer 2, has strip-shaped first parts 3a' extending along the rows of the matrix (i.e., in the X direction) , strip-shaped second parts 3b' extending along the columns of the matrix (i. e., in the Y direction), and rectangular third parts 3c' laterally protruding to cover the corresponding pixel areas 20. The first and second parts 3a' and 3b' are intersected with each other to thereby constitute a lattice-like plan shape. The third parts 3c' are located at the respective intersections of the parts 3a' ad 3b'. The layer 3' is made of a material having a sufficiently low optical transmittance (e.g.., WSi_2). The thickness of the layer 3' is set to be large enough for blocking light entering directly from the back side of the substrate 30C, i.e., from the side of the plate 1. The whole layer 3' is covered with an overlying SiO_2 layer 4.

[0125] On the SiO_2 layer 4, the patterned second light-shielding layer 5C is formed. The layer 5C is made of amorphous silicon having light-absorbing properties. The layer 5C comprises lateral strip-shaped parts 5Ca extending along the rows (the X direction in Fig. 4) of the matrix of the TFTs 31 and vertical rectangular parts 5Cb extending along the columns (the Y direction in Fig. 4) thereof and intersecting with the lateral parts 5Ca. The strip-shaped parts 5Ca are arranged vertically (in the Y direction) at equal intervals, which are parallel to each other. The rectangular parts 5Cb are arranged horizontally (in the X direction) at equal intervals, which are parallel to each other. The layer 5C is patterned to entirely overlap with the underlying first light-shielding layer 3'. The layer 5C is covered with a SiO_2 layer 6 formed on the SiO_2 layer 4.

[0126] On the SiO_2 layer 6, the polysilicon active layers 7' are formed. Each of the layers 7' is patterned to have an approximately linear plan shape. Each of the layers 7' is located at a position near the intersection of a corresponding gate line 9 and a corresponding gate

data line 11.

[0127] Each of the polysilicon active layers 7' comprises an undoped channel region 7c', two lightly-doped LDD regions 7b' and 7d', a heavily-doped source region 7a', and a heavily-doped drain region 7e'. The source and drain regions 7a' and 7e' are located at each side of the channel region 7c'. The LDD region 7b' is located between the source region 7a' and the channel region 7c'. The LDD region 7d' is located between the channel region 7c' and the drain region 7e'.

[0128] The source region 7a', the LDD region 7b', the channel region 7c', the LDD region 7d', and the drain region 7e' are arranged along the X direction in such a way as to overlap with the first and second light-shielding layers 3' and 5C.

[0129] A gate dielectric layer 8 is formed on the SiO_2 layer 6 to cover the underlying active layers 7'.

[0130] Gate lines 9 and gate electrodes 9a, both of which are made of impurity-doped polysilicon or silicide, are formed on the gate dielectric layer 8. The gate lines 9 are parallel to each other and extend in the X direction in such a way as not to overlap with the active layers 7' of the TFTs 31. Instead, the gate electrodes 9a are formed to overlap with the corresponding channel regions 7c' of the respective TFTs 31. The gate electrodes 9a are mechanically and electrically connected to the corresponding gate lines 9. The gate lines 9 and the gate electrodes 9a are entirely covered with a first interlayer dielectric layer 10 formed on the layer 8.

[0131] Data lines 11, which are made of Al, are formed on the first interlayer dielectric layer 10. These lines 11 are parallel to each other and extend in the Y direction. Each of the lines 11 is located to overlap with the active layers 7' of the TFTs 31 that belong to the same column of the matrix. The line 11 entirely covers the source regions 7a' of the corresponding TFTs 31. The line 11 is mechanically contacted with and electrically connected to the source regions 7a' of the TFTs 31 that belong to the same row of the matrix by way of contact holes 21 that penetrate the first interlayer dielectric layer 10 and the gate dielectric layer 8. The lines 11 are entirely covered with a second interlayer dielectric layer 12.

[0132] The patterned black matrix layer 13', which is made of Cr, is formed on the second interlayer dielectric layer 12. The plan shape of the layer 13' is like a lattice, which is formed by lateral strips extending along the rows (the X direction in Fig. 4) of the matrix and vertical strips extending along the columns (the Y direction in Fig. 4) thereof and intersecting with the lateral ones. The layer 13' is patterned to overlap with the gate lines 9, the gate electrodes 9a, and the data lines 11. The rectangular parts of the layer 13', which protrude laterally to overlap with the pixel electrodes 20, cover the corresponding TFTs 31. The layer 13' serves as the third light-shielding layer. The layer 13' is entirely covered with a third interlayer dielectric layer 14 formed on the layer 12.

[0133] Pixel electrodes 15, which have an approximately rectangular plan shape, are formed on the third interlayer dielectric layer 14. The electrodes 15 are located in corresponding pixel areas 20 defined by the gate lines 9 and the data lines 11. The electrodes 15 are mechanically contacted with and electrically connected to the drain regions 7e' of the corresponding TFTs 31 by way of contact holes 22 that penetrate the third interlayer dielectric layer 14, the second interlayer dielectric layer 12, the first interlayer dielectric layer 10, and the gate dielectric layer 8.

[0134] With the TFT array substrate 30C according to the fourth embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, as shown in Fig. 17, the light L1 entering the LCD device from the side of the opposite substrate 52 is blocked by the black matrix layer (i.e., the third light-shielding layer) 13'. Alternately, the light L1 penetrates the substrate 30C without reflection by the first light-shielding layer 3'. This is because the widths of the layers 13' and 3' and the interval between the layers 13' and 3' are well adjusted for this purpose.

[0135] On the other hand, the light L2 entering the LCD device from the side of the TFT array substrate 30C (51) is blocked by the first light-shielding layer 3'. The light L3 entering from the side of the substrate 30C toward the black matrix layer 13' is reflected by the layer 13' to go to the first light-shielding layer 3'. Then, the light L3 reaches the second light-shielding layer 5C located between the layer 3' and the TFTs 31. Alternately, the light L3 is reflected by the layer 13' and 3' and then, the light L3 reaches the second light-shielding layer 5C. Since the second light-shielding layer 5C is made of amorphous Si having light-absorbing properties the light L1 to Le are absorbed by the layer 5C.

[0136] In this way, even if light traveling from the side of the plate 1 is reflected by the third patterned light-shielding layer (i.e., the black matrix layer) 13' and then, reflected by the first light-shielding layer 3', the light will be absorbed by the second light-shielding layer 5C. Thus, any light traveling toward the channel region 7c' and the LDD regions 7b' and 7d' of each TFT 31 is effectively and certainly blocked.

[0137] In addition, the channel region 7c' of each TFT 31 is covered with the corresponding one of the gate electrodes 9a and therefore, the effect to block the light traveling toward the region 7c' is enhanced.

[0138] The substrate 30C is fabricated in substantially the same method as used in the first embodiment.

[0139] With the TFT array substrate 30C according to the fourth embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, any light traveling toward the channel region 7c' and the LDD regions 7b' ad 7d' of the TFTs 31 in the substrate 30C is effectively blocked. This means that these regions 7c', 7b' and 7d' are not exposed to the light. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality. Moreover, the substrate 30C can be fabricated easily without complicated process steps.

FIFTH EMBODIMENT

[0140] Fig. 18 shows the structure of a TFT array substrate 30D according to the fifth embodiment of the invention, in which only one pixel is illustrated for simplification.

[0141] The substrate 30D of the fifth embodiment has the same configuration as the substrate 30C of the fourth embodiment, except that a second light-shielding layer 5D has conductivity and electrically connected to the corresponding gate lines 9. Therefore, the explanation about the same configuration is omitted here for the sake of simplification by attaching the same reference symbols as used in the fourth embodiment of Figs. 15 and 16A to 16B to the same or corresponding elements in the fifth embodiment of Fig. 18.

[0142] In the substrata 30D, the second light-shielding layer 5D is made of an impurity-doped polysilicon. The layer 5D has strip-shaped first parts 5Da extending along the rows of the matrix (i.e., in the X direction) and rectangular second parts 5Db extending along the columns of the matrix (i.e., in the Y direction) . The first parts 5Da are parallel to each other. The second parts 5Db, which laterally protrude over the pixel regions 20, are overlapped with the respective polysilicon active layers 7'. The layer 5D is formed in such a way as to overlap with the first light-shielding layer 3'.

[0143] The second light-shielding layer 5D is electrically connected to the corresponding gate lines 9 by way of internal wiring lines 41, like the second embodiment. Therefore, the gate electrodes 9a serve as first gate electrodes of the TFTs 31 and at the same time, the layer 5D serves as the common second gate electrode thereof. This means that the TFTs 31 serve as dual-gate FETs.

[0144] In this way, with the substrate 30D of the fifth embodiment, the second light-shielding layer 5D is used as the common second gate electrode and therefore, the inter-electrode capacitance of the TFTs 31 increases. To suppress the increase of the inter-electrode capacitance, the width W of the second part 5Db in the X direction is decreased compared with the fourth embodiment.

[0145] Specifically, the second part 5Db of the second light-shielding layer 5D is overlapped with the channel region 7c' and the LDD regions 7b' and 7d' of the TFT 31 while it is scarcely overlapped with the source and drain regions 7a' and 7e'. Due to this structure, the increase of the inter-electrode capacitance of the TFT 31 can be suppressed at a level where practically no problem

occurs while keeping the effect to block the light traveling toward the channel and LDD regions 7c', 7b', and 7d'.

[0146] The substrate 30d is fabricated in substantially the same method as used in the first embodiment.

[0147] With the TFT array substrate 30D according to the fifth embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, any light traveling toward the channel region 7c' and the LDD regions 7b' and 7d' of the TFTs 31 in the substrate 30D is effectively blocked. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality. Moreover, the substrate 30D can be fabricated easily without complicated process steps.

[0148] The substrate 30D has an additional advantage that an improved on/off characteristic of the TFTs 31 is obtainable, because the TFTs 31 serve as dual-gate FETs. This is the same as the second embodiment.

SIXTH EMBODIMENT

[0149] Fig. 19 shows the structure of a TFT array substrate 30E according to the sixth embodiment of the invention, in which only one pixel is illustrated for simplification.

[0150] The substrate 30E of the sixth embodiment has the same configuration as the substrate 30C of the fourth embodiment, except that a second light-shielding layer 5E has conductivity and is applied with a constant voltage V_c. Therefore, the explanation about the same configuration is omitted here for the sake of simplification by attaching the same reference symbols as used in the fourth embodiment of Figs. 15 and 16A to 16B to the same or corresponding elements in the sixth embodiment of Fig. 19.

[0151] In the substrate 30E, the second light-shielding layer 5E, which is made of an impurity-doped polysilicon, is formed on the SiO_2 layer 4. The second light-shielding layer 5E has strip-shaped first parts 5Ea extending along the rows of the matrix (i.e., in the X direction), rectangular second parts 5Eb, and strip-shaped third parts 5Ec extending along the columns of the matrix (i.e., in the Y direction). The first and third parts 5Ea and 5Ec are intersected with each other to thereby constitute a lattice-like plan shape. The second parts 5Eb are located at the respective intersections of the parts 5Ea and 5Ec and protruded over the pixel regions 20. The layer 5E is formed in such a way as to overlap with the first light-shielding layer 3'. The second parts 5Eb are overlapped with the polysilicon active layers 7'.

[0152] The second light-shielding layer 5E is electrically connected to an external terminal 51 through which a constant voltage V_c is supplied to the layer 5E, like the substrate 30B of the third embodiment. Thus, the layer 5E is biased at the voltage V_c. By adjusting the value of the voltage V_c, the characteristic of the TFT 31 can be controlled as desired.

[0153] The substrate 30E is fabricated in substantially the same method as used in the first embodiment.

[0154] With the TFT array substrate 30E according to the sixth embodiment, the same advantages as those in the first embodiment are obtainable. Specifically, any light traveling toward the active layers 7 (especially, the channel region 7c' and the LDD regions 7b' and 7d') of

the TFTs 31 in the substrate 30E is effectively blocked. As a result, the optically induced current leakage in the TFTs 31 is suppressed, thereby improving the contrast and uniformity of image quality. Moreover, the substrate 30E can be fabricated easily without complicated process steps.

[0155] The substrate 30E has an additional advantage that the characteristic of the TFTs 31 is controllable by adjusting the value of the voltage VC applied to the second light-shielding layer 5B, like the substrate 30B of the third embodiment.

SEVENTH EMBODIMENT

[0156] In the above-described first to sixth embodiments, the second light-shielding layer 5 is provided between the first light-shielding layer 3 and the TFTs 31, in addition to the first light-shielding layer 3 and the third light-shielding layer (i.e., the black matrix layer) 13, thereby enhancing the light-shielding effect.

[0157] In the following seventh to tenth embodiments of the invention, a fourth light-shielding layer 16 or 16' is provided between the TFTs 31 and the third light-shielding layer (black matrix layer) 13 to enhance the light-shielding effect. As seen from these embodiments, even if the fourth light-shielding layer 16 or 16' is provided on the opposite side to the plate 1 with respect to the TFTs 31, any light traveling toward the active layers 7 of the TFTs 31 is effectively blocked or suppressed, similar to the case of the second light-shielding layer 5.

[0158] Figs. 21A and 21B show the structure of a TFT array substrate 30F according to the seventh embodiment of the invention, which are along the lines VA-VA and VB-VB in Fig. 4, respectively.

[0159] The substrate 30F of the seventh embodiment is obtained by canceling the second light-shielding layer 5 from the TFT array substrate 30 of the first embodiment of Figs. 4, 5A and 5B and by adding the fourth light-shielding layer 16 thereto. The other structure of the substrate 30F is the same as the substrate 30. Since the second light-shielding layer 5 is canceled, the SiO_2 layer 4 or 6 may be canceled in the TFT array substrate 30.

[0160] The pattern or plan shape of the fourth light-shielding layer 16 is the same as the second light-shielding layer 5 shown in Fig. 4, which covers almost all the polysilicon active layer 7 of each TFT 31. The layer 16 does not cover the part of the layer 7 near the contact hole 22.

[0161] The fourth light-shielding layer 16 is buried in the first interlayer dielectric layer 10. This is easily realized if the layer 10 has a two-layer structure. Specifically, after the lower part of the layer 10 is formed, an amorphous silicon layer for the layer 16 is formed on the lower part. Then, the amorphous silicon layer is patterned to form the layer 16. Finally, the upper part of the layer 10 is formed.

[0162] However, the invention is not limited to the structure shown in Figs. 21A and 21B. For example, the fourth light-shielding layer 16 may be formed on the first interlayer dielectric layer 10 and then, an additional dielectric layer may be formed to cover the layer 16. Finally, the second interlayer dielectric layer 12 may be formed to cover the additional dielectric layer.

EIGHTH EMBODIMENT

[0163] Figs. 22A and 22B show the structure of a TFT array substrate 30G according to the eighth embodiment of the invention, which are along the lines VA-VA and VB-VB in Fig. 4, respectively.

[0164] The substrate 30G of the eighth embodiment is obtained by adding the fourth light-shielding layer 16 to the TFT array substrate 30 of the first embodiment of Figs. 4, 5A and 5B. The other structure of the substrate 30G is the same as the substrate 30. It may be said that the substrate 30G is obtained by adding the second light-shielding layer 5 to the substrate 30F of the seventh embodiment of Figs. 21A and 21B.

[0165] Since the fourth and second light-shielding layers 16 and 5 are provided at each side (i.e., at the top and bottom) of the TFTs 31, the light-shielding effect is obtainable at each side of the TFTs 31. Thus, there is an additional advantage that a higher light-shielding effect is obtainable than the first and seventh embodiments.

NINTH EMBODIMENT

[0166] Figs. 23A and 23B show the structure of a TFT array substrate 30H according to the ninth embodiment of the invention, which are along the lines XVIA-XVIA and XVIB-XVIB in Fig. 15, respectively.

[0167] The substrate 30H of the ninth embodiment is obtained by canceling the second light-shielding layer 5C from the TFT array substrate 30C of the fourth embodiment of Figs. 16A and 16B and by adding the fourth light-shielding layer 16' thereto. The other structure of the substrate 30H is the same as the substrate 30C. Since the second light-shielding layer 5C is canceled, the SiO_2 layer 4 or 6 may be canceled in the TFT array substrate 30C.

[0168] The pattern or plan shape of the fourth light-shielding layer 16' is the same as the second light-shielding layer 5C shown in Fig. 15, which covers almost all the polysilicon active layer 7 of each TFT 31. The layer 16' does not cover the part of the layer 7 near the contact hole 22.

[0169] The fourth light-shielding layer 16' is buried in the second interlayer dielectric layer 12. This is easily realized if the layer 12 has & two-layer structure. Specifically, after the lower part of the layer 12 is formed, an amorphous silicon layer for the layer 16' is formed on the lower part. Then, the amorphous silicon layer is patterned to form the layer 16'. Finally, the upper part of the layer 12 is formed.

[0170] However, the invention is not limited to the structure shown in Figs. 23A and 23B. For example, the fourth light-shielding layer 16' may be formed on the second interlayer dielectric layer 12 and then, an additional dielectric layer may be formed to cover the layer 16'. Finally, the third interlayer dielectric layer 14 may be formed to cover the additional dielectric layer.

TENTH EMBODIMENT

[0171] Figs. 24A and 24B show the structure of a TFT array substrate 30I according to the tenth embodiment of the invention, which are along the lines VA-VA and VB-VB in Fig. 4, respectively.

[0172] The substrate 30I of the tenth embodiment is obtained by adding the fourth light-shielding layer 16' to the TFT array substrate 30C of the fourth embodiment of Figs. 15, 16A and 16B. The other structure of the substrate 30I is the same as the substrate 30C. It may be said that the substrate 30I is obtained by adding the second light-shielding layer 5C to the substrate 30H of the ninth embodiment of Figs. 23A and 23B.

[0173] Since the fourth and second light-shielding layers 16' and 5C are provided at each side (i.e., at the top and bottom) of the TFTs 31, the light-shielding effect is obtainable at each side of the TFTs 31. Thus, there is an additional advantage that a higher light-shielding effect is obtainable than the first and seventh embodiments.

[0174] Fig. 25 shows the relationship of the optically induced current leakage of the TFTs 31 provided in the pixel matrix section with the dielectric layer thickness between the active layer and the second light-shielding layer, which was obtained under a specific irradiation condition of projection light.

[0175] As seen from Fig. 25, with the prior-art TFT array substrate 100 (see Figs. 1, 2A and 2B) having only the first and third light-shielding layers, the optically induced current leakage is 4 pA. On the other hand, with the TFT array substrate 30C (see Figs. 15, 16A and 16B) having the second light-shielding layer along with the first and third light-shielding layers according to the fourth embodiment of the invention, the optically induced current leakage decreases gradually as the dielectric layer thickness between the active layer and the second light-shielding layer is reduced from 500 nm. At the maximum, the value of the leakage decreases to approximately (1/3) of the value of the prior-art substrate 100.

[0176] Moreover, as seen from Fig. 25, the effect to decrease the current leakage had a correlation with the dielectric layer thickness between the active layer and the second light-shielding layer. As this thickness was decreased from 500 nm, this effect increased. However, although not shown in Fig. 25, the thickness was set at values less than 100 nm, the ON characteristic of the TFTs 31 and the crystallinity of the active layers 7 in the laser annealing process were affected largely and as a result, the TFTs 31 were unable to operate normally due to deterioration of the ON characteristic of the TFTs 31. According to this test result, it was found that the dielectric layer thickness in question was preferably set at values in the range from 500 nm to 100 nm.

[0177] With the TFT array substrate 30I (see Figs. 24A and 24B) having the second and fourth light-shielding layers along with the first and third light-shielding layers according to the tenth embodiment of the invention, the value of the optically induced current leakage decreased to approximately (1/2) of the value of the substrate 30C according to the fourth embodiment. Thus, by adding the fourth light-shielding layer along with the second light-shielding layer, it was confirmed that a higher effect to suppress the leakage was obtained.

ELEVENTH EMBODIMENT

[0178] In general, when laser light is irradiated to an amorphous silicon layer to form a polysilicon active layer (in other words, when a polysilicon active layer is obtained from an amorphous silicon layer by the laser annealing process), the heating and cooling process by the laser light irradiation will change from its desired one, if a substance with a high thermal conductivity exists directly below the amorphous silicon layer. As a result, there arises a problem that the crystallization process of the amorphous silicon layer is fairly affected. To avoid this problem, conventionally, it was typical that a dielectric layer with a sufficient thickness is located between the amorphous silicon layer and the thermally conductive substance, thereby keeping them sufficiently apart.

[0179] On the other hand, it is known that pixel matrix section 61 and the driver circuit section 62 may be formed on the same substrate, like a TFT array substrate 60 shown in Fig. 26. In this case, the TFTs in the driver circuit section 62 necessitate high mobility in transistor characteristics. Unlike this, the TFTs in the pixel matrix section 61 do not necessitate high mobility; they necessitate low current leakage in transistor characteristics. To decrease the optically induced current leakage, it is preferred that the silicon material contains comparatively many traps that serve as the recombination centers. Taking this into consideration, it is preferred for the TFTs in the pixel matrix section 61 that the polysilicon material has low crystallinity.

[0180] Accordingly, with the TFT array substrate 60 according to the eleventh embodiment of the invention, the TFTs 31 having the second and/or fourth light-shielding layer(s) according to the first to tenth embodiments are used for the pixel matrix section 61. At the same time, for the driver circuit section 62, TFTs not having the second and/or fourth light-shielding layer(s) are used. In this way, with the TFTs in the section 61, the laser-inducing heat can be propagated quickly with the second and/or fourth light-shielding layer(s). As a result, the polysilicon layers with low crystallinity are formed for only the active layers of the TFTs in the pixel matrix sec-

tion 61. This means that the optically induced current leakage can be suppressed further, because of not only the existence of the second and/or fourth light-shielding layer(s) but also the crystallinity level of the polysilicon layer.

VARIATIONS

[0181] Needless to say, the present invention is not limited to the above-described first to eleventh embodiments, because these embodiments are preferred ones of the invention. Any change or modification may be added to them within the spirit of the invention.

[0182] For example, in the first to sixth embodiments, the first light-shielding layer 3 is formed over the transparent plate 1 by way of the SiO_2 layer 2. However, the first light-shielding layer 3 may be formed directly on the transparent plate 1 without the SiO_2 layer 2, according to the material of the plate 1. In the third and sixth embodiments, the second light-shielding layers 5B and 5E may be made of amorphous Si, and at the same time, the constant voltage V_c may not be applied to the layers 5B and 5E. In the first and fourth embodiments, the second light-shielding layers 5 and 5C may be made of polysilicon. In the second, third, fifth, and sixth embodiments, the second light-shielding layers 5A, 5B, 5D and 5E may be made of impurity-doped amorphous Si. These are applicable to the seventh to eleventh embodiments.

[0183] The second and fourth light-shielding layers may be made of any other material than the above-described material if it absorbs light to be applied to the TFT array substrate.

[0184] While the preferred forms of the present invention have been described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the spirit of the invention. The scope of the present invention, therefore, is to be determined solely by the following claims.

Claims

1. A TFT array substrate comprising:

(a) a transparent plate;
(b) TFTs arranged on the plate in a matrix array with rows and columns;
each of the TFTs having a first source/drain region, a second source/drain region, and an active layer;
(c) gate lines formed on the plate in such a way as to extend along the rows of the matrix;
(d) data lines formed on the plate in such a way as to extend along the columns of the matrix;
each of the data lines being electrically connected to corresponding ones of the TFTs at their first source/drain regions;
(e) pixel electrodes formed in pixel areas on the plate;
each of the pixel electrodes being electrically connected to corresponding ones of the TFTs at their second source/drain regions;
(f) a patterned first light-shielding layer formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs;
(g) a patterned second light-shielding layer formed between the first light-shielding layer and the TFTs;
the second light-shielding layer having light-absorbing properties;
(h) a patterned third light-shielding layer formed to cover the TFTs on an opposite side to the plate with respect to the TFTs;
the third light-shielding layer having first parts extending along the rows of the matrix and second parts extending along the columns thereof.

2. The substrate according to claim 1, wherein each of the TFTs has a channel region and a LDD region;
the second light-shielding layer having first parts covering the channel regions of the TFTs and second parts covering the LDD regions thereof.

3. The substrate according to claim 1, wherein the second light-shielding layer is made of a material including silicon.

4. The substrate according to claim 1, wherein the second light-shielding layer has conductivity;
the second light-shielding layer having a structure that allows application of a constant voltage.

5. The substrate according to claim 1, wherein the second light-shielding layer has conductivity and is connected electrically to the gate lines.

6. The substrate according to claim 1, wherein the second light-shielding layer is made of silicon doped with an impurity.

7. The substrate according to claim 1, wherein the gate lines are arranged in such a way as to overlap with the channel regions of the corresponding TFTs;
and wherein the gate lines have a function of gate electrodes of the TFTs at their overlapping parts.

8. The substrate according to claim 1, further comprising gate electrodes formed for the respective TFTs separately from the gate lines;
wherein the gate lines are electrically connected to the corresponding gate electrodes.

9. The substrate according to claim 1, wherein a dielectric sandwiched by the second light-shielding layer and the active layers of the TFTs has a thickness ranging from 100 nm to 500 nm.

10. The substrate-according to claim 1, wherein a dielectric sandwiched by the second light-shielding layer and the active layers of the TFTs has a thickness ranging from 150 nm to 300 nm.

11. The substrate according to claim 1, wherein a driver circuit section including TFTs is provided in addition to a pixel matrix section where the TFTs are arranged in a matrix array;

and wherein the second light-shielding layer is provided for the TFTs in the pixel matrix section while the second light-shielding layer is not provided for the TFTs in the driver circuit section.

12. An active-matrix addressing LCD device comprising:

(a) a TFT array substrate according to claim 1;
(b) an opposite substrate located to be opposite to the TFT array substrate; and
(c) a liquid-crystal layer formed between the TFT array substrate and the opposite substrate.

13. A TFT array substrate comprising:

(a) a transparent plate;
(b) TFTs arranged on the plate in a matrix array with rows and columns?

each of the TFTs having a first source/drain region, a second source/drain region, and an active layer;
(c) gate lines formed on the plate in such a way as to extend along the rows of the matrix;
(d) data lines formed on the plate in such a way as to extend along the columns of the matrix;

each of the data lines being electrically connected to corresponding ones of the TFTs at their first source/drain regions;
(e) pixel electrodes formed in pixel areas on the plate;

each of the pixel electrodes being electrically connected to corresponding ones of the TFTs at their second source/drain regions;
(f) a patterned first light-shielding layer formed between the plate and the TFTs in such a way as to overlap with the active layers of the TFTs;
(g) a patterned third light-shielding layer formed to cover the TFTs on an opposite side to the plate with respect to the TFTs;

the third light-shielding layer having first parts extending along the rows of the matrix and second parts extending along the columns thereof; and
(h) a patterned fourth light-shielding layer formed between the TFTs and the third light-shielding layer;

the fourth light-shielding layer having light-absorbing properties.

14. The substrate according to claim 13, wherein each of the TFTs has a channel region and a LDD region;

and wherein the fourth light-shielding layer has first parts covering the channel regions of the TFTs and second parts covering the LDD regions thereof.

15. The substrate according to claim 13, wherein the fourth light-shielding layer is made of a material including silicon.

16. The substrate according to claim 13, wherein the fourth light-shielding layer has conductivity; the fourth light-shielding layer having a structure that allows application of a constant voltage.

17. The substrate according to claim 13, wherein the fourth light-shielding layer has conductivity and is connected electrically to the gate lines.

18. The substrate according to claim 13, wherein the fourth light-shielding layer is made of silicon doped with an impurity.

19. The substrate according to claim 13, wherein the gate lines are arranged in such a way as to overlap with the channel regions of the corresponding TFTs;

and wherein the gate lines have a function of gate electrodes of the TFTs at their overlapping parts.

20. The substrate according to claim 13, wherein gate electrodes are formed for the respective TFTs separately from the gate lines;

and wherein the gate lines are electrically connected to the corresponding gate electrodes.

21. The substrate according to claim 13, further comprising a patterned second light-shielding layer formed between the first light-shielding layer and the TFTs;

wherein the second light-shielding layer has a light-absorbing property.

22. The substrate according to claim 21, wherein a dielectric sandwiched by the second light-shielding layer and the active layers of the TFTs has a thickness ranging from 100 nm to 500 nm.

23. The substrate according to claim 21, wherein a dielectric sandwiched by the second light-shielding

layer and the active layers of the TFTs has a thickness ranging from 150 nm to 300 nm.

24. The substrate according to claim 21, wherein a driver circuit section including TFTs is provided in addition to a pixel matrix section where the TFTs are arranged in a matrix array;

and wherein the second light-shielding layer is provided for the TFTs in the pixel matrix section while the second light-shielding layer is not provided for the TFTs in the driver circuit section.

25. An active-matrix addressing LCD device comprising:

(a) a TFT array substrate according to claim 13;
(b) an opposite substrate located to be opposite to the TFT array substrate; and
(c) a liquid-crystal layer formed between the TFT array substrate and the opposite substrate.

FIG. 1 PRIOR ART

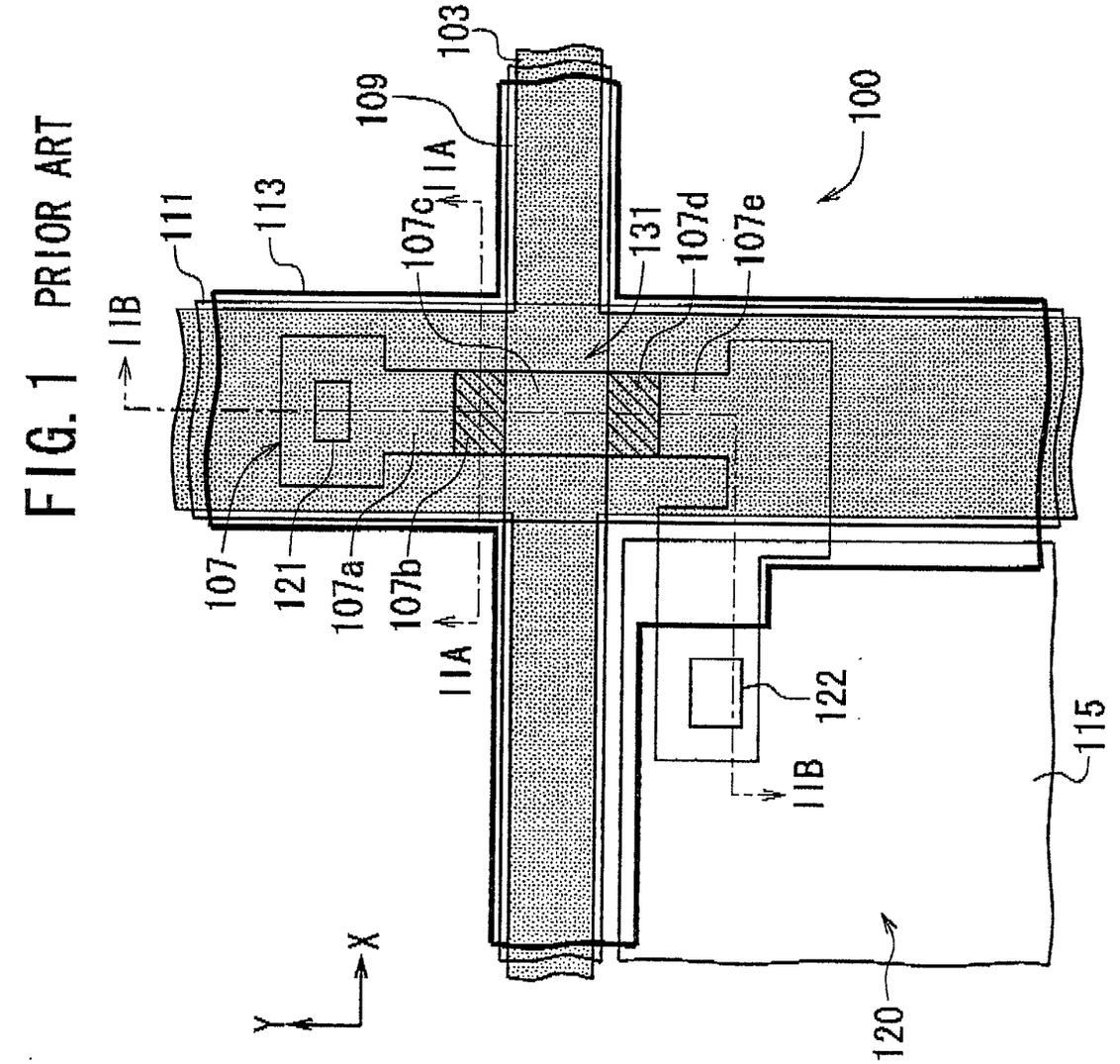


FIG. 2A PRIOR ART

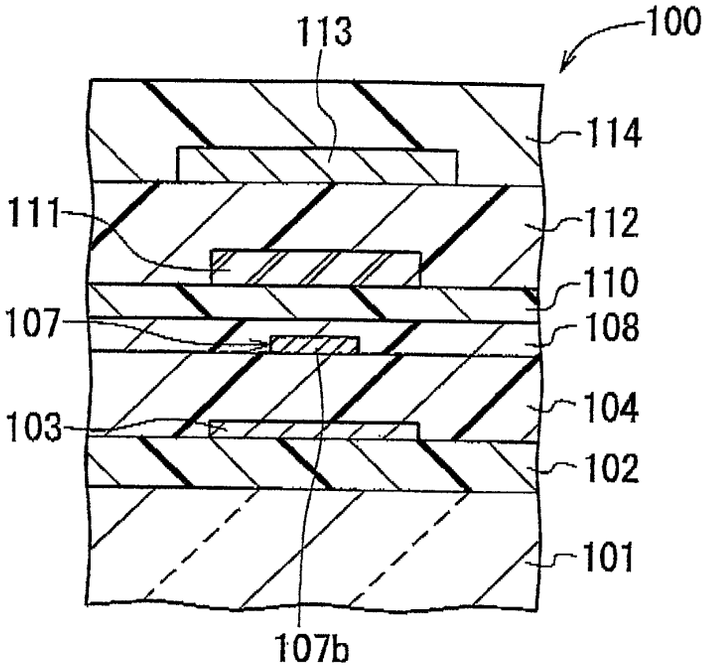


FIG. 2B PRIOR ART

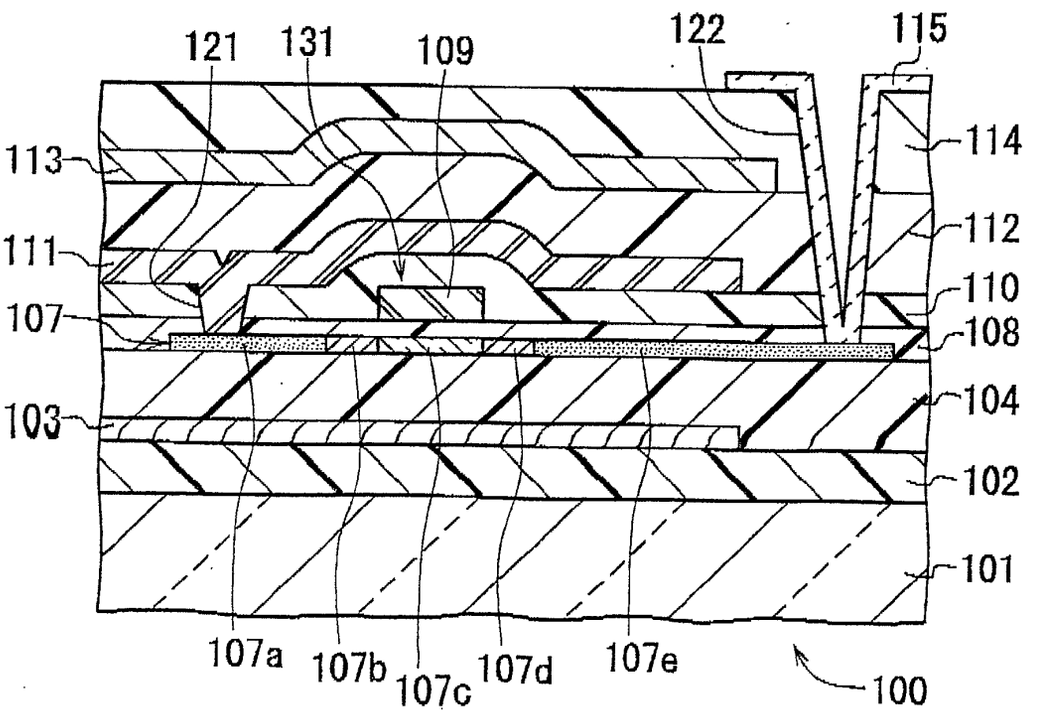


FIG. 3
PRIOR ART

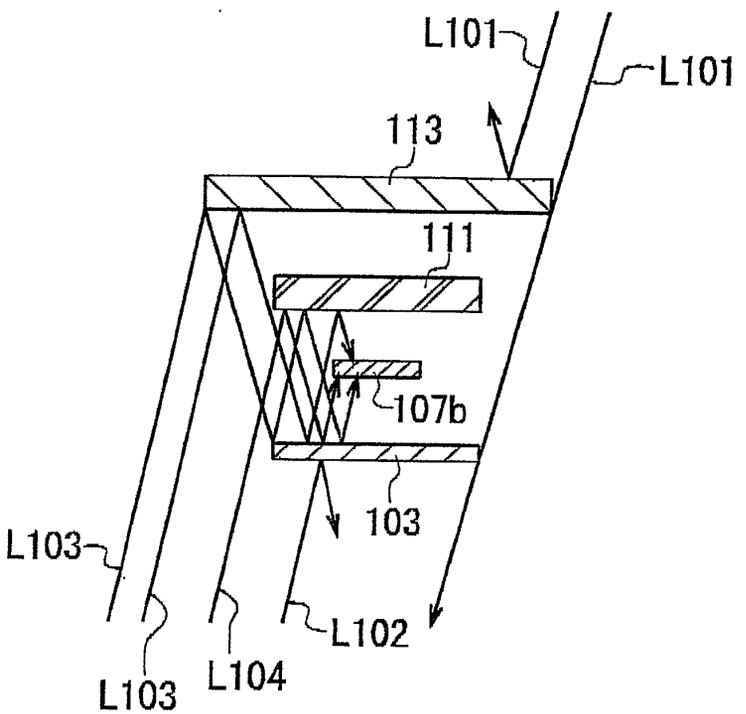


FIG. 4

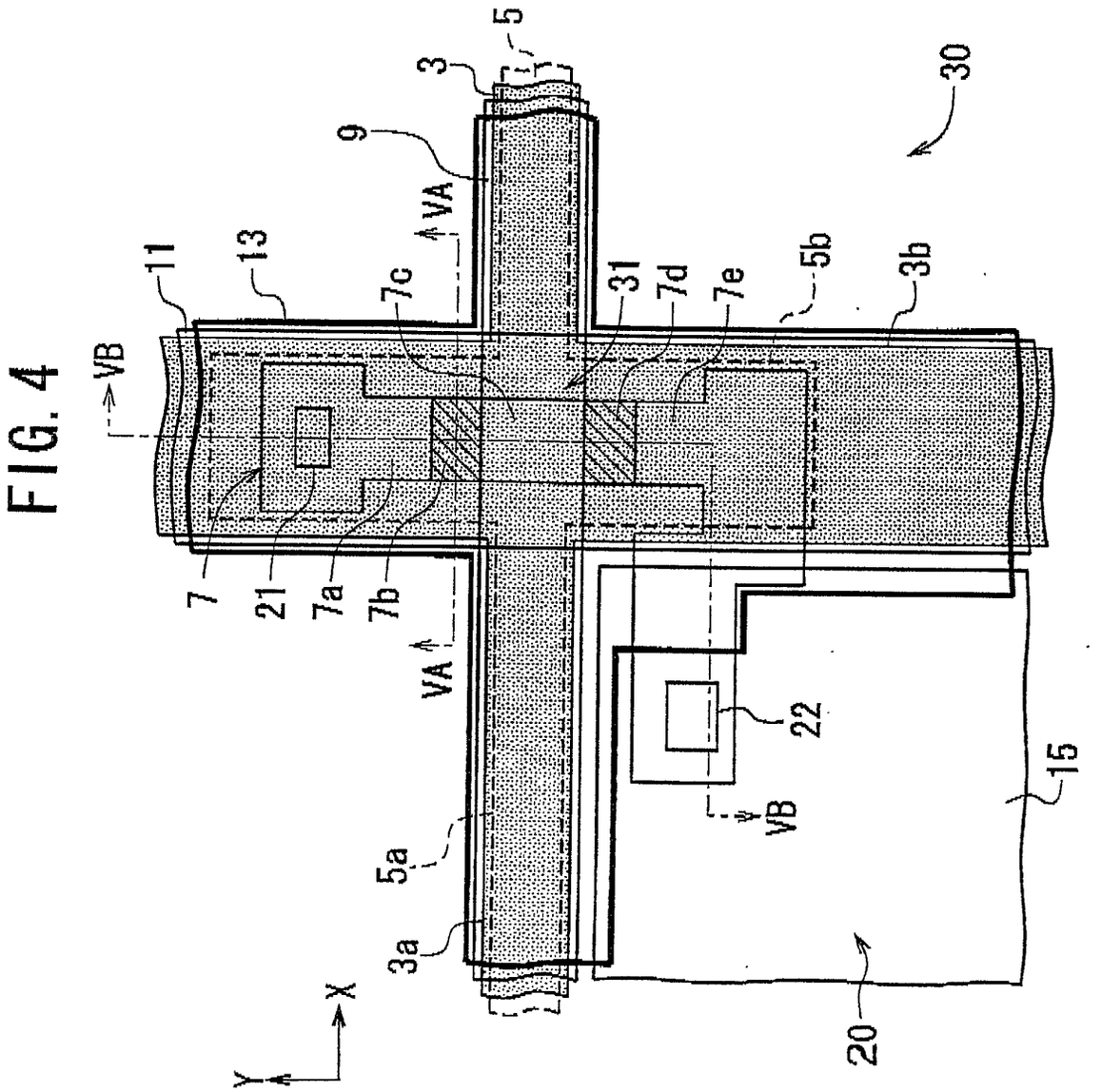
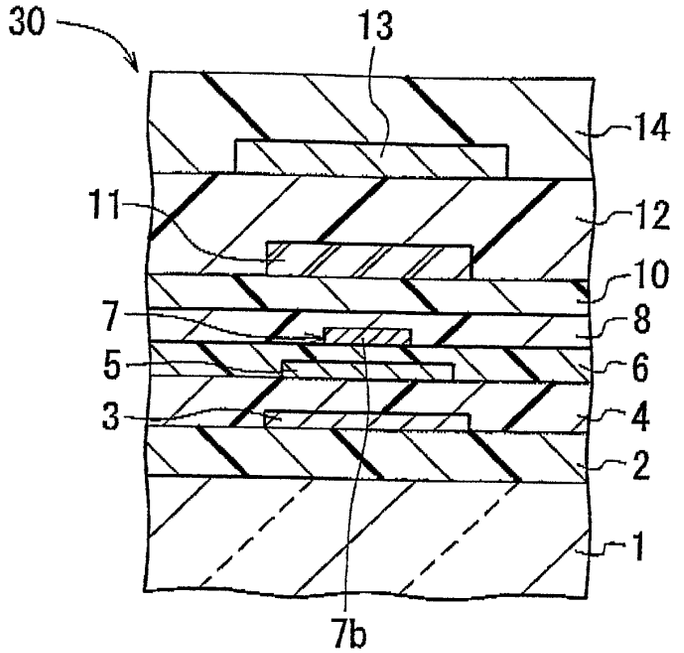


FIG. 5A


30
13
14
11
12
10
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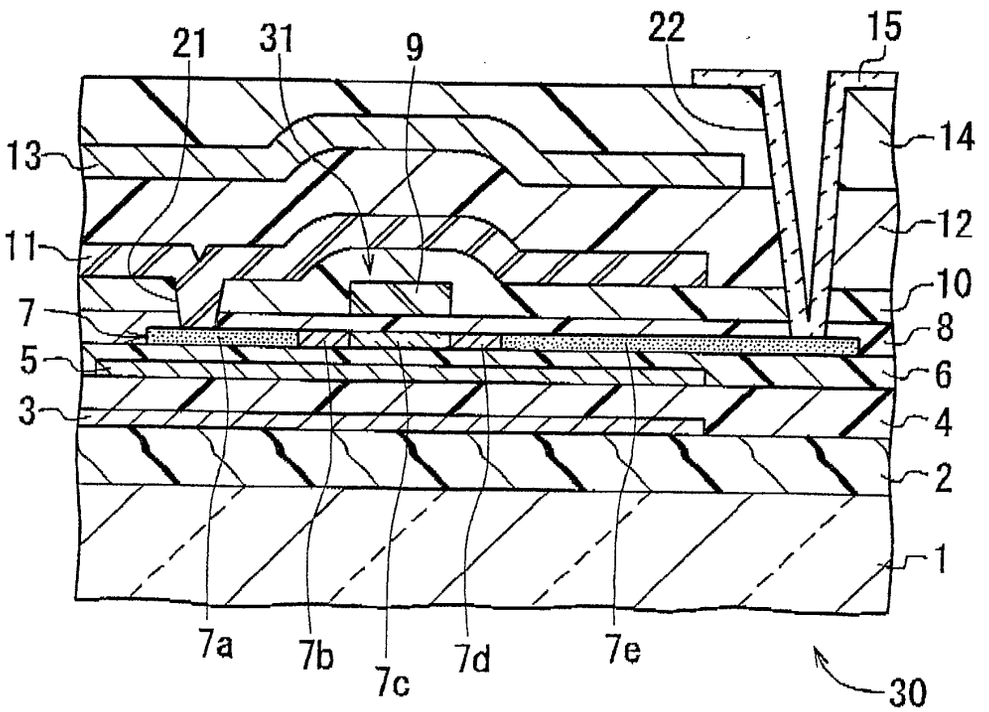
8
5
6
3
4
2
1
7b

FIG. 5B


21
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14
11
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5
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7a
7b
7c
7d
7e
30

FIG. 6

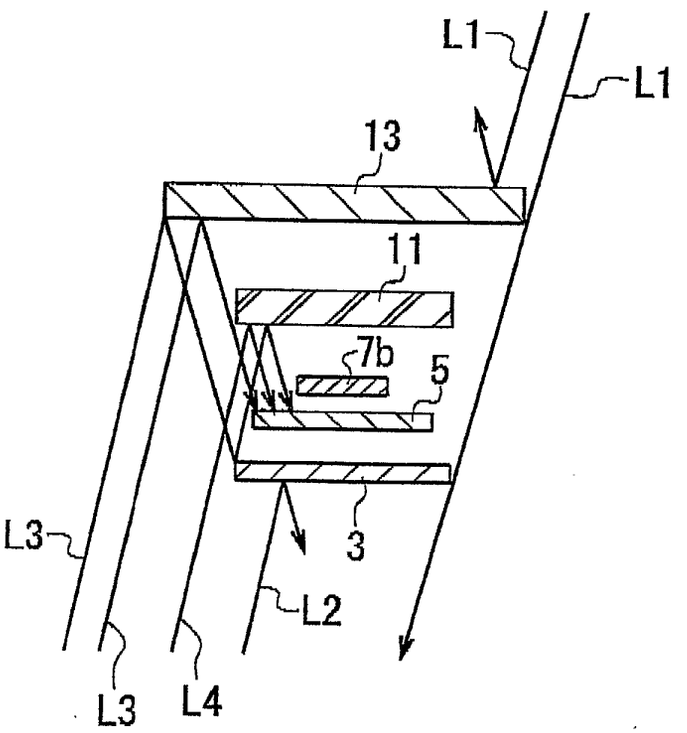


FIG. 7A

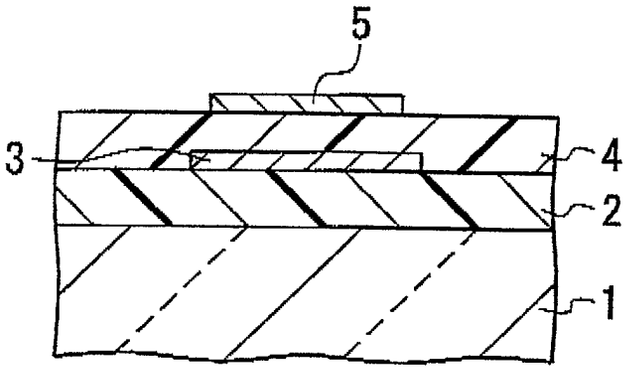


FIG. 7B

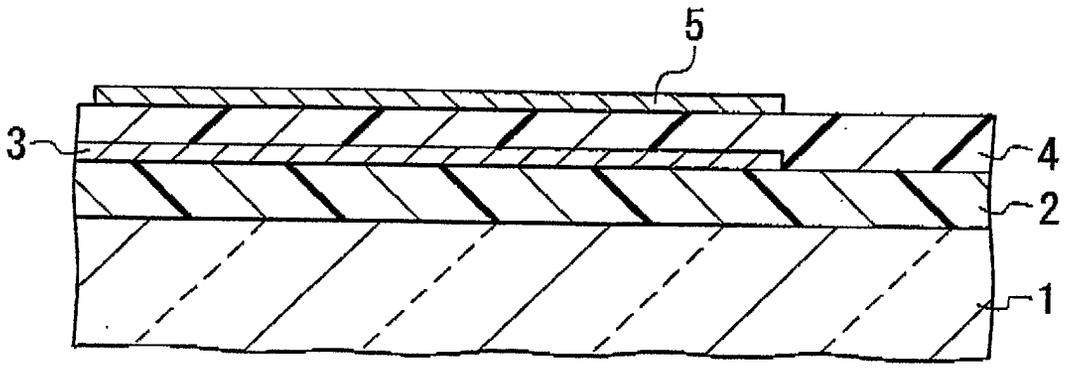


FIG. 8A

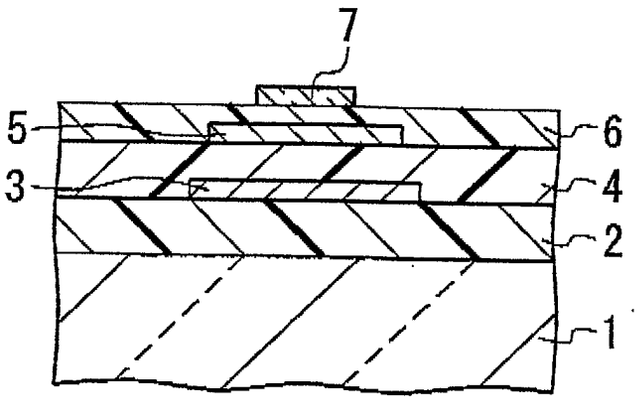


FIG. 8B

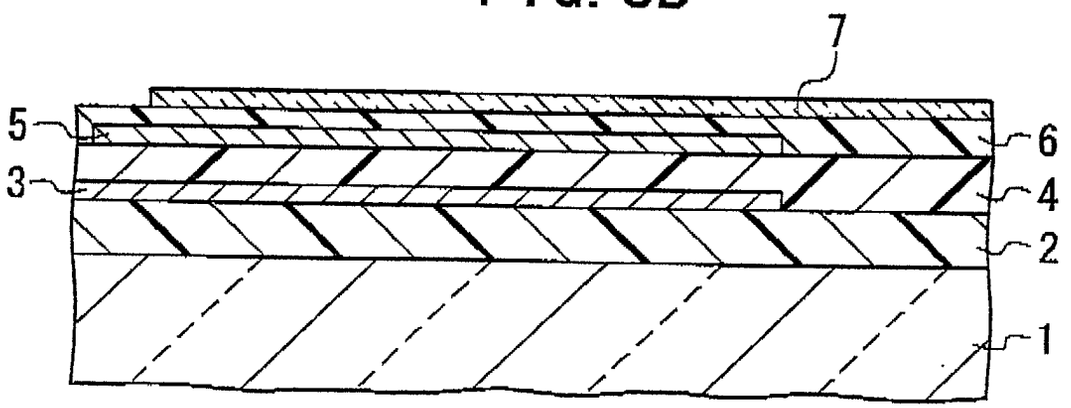


FIG. 9A

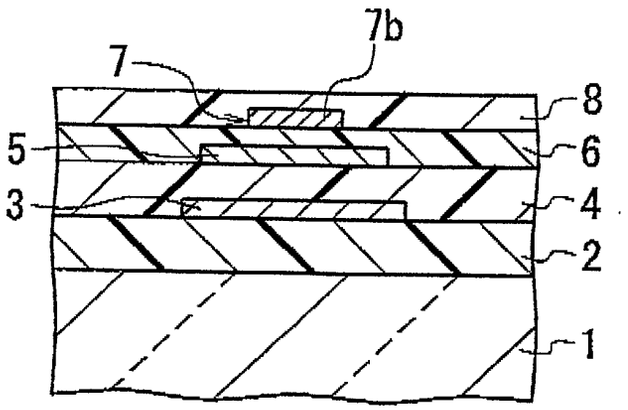


FIG. 9B

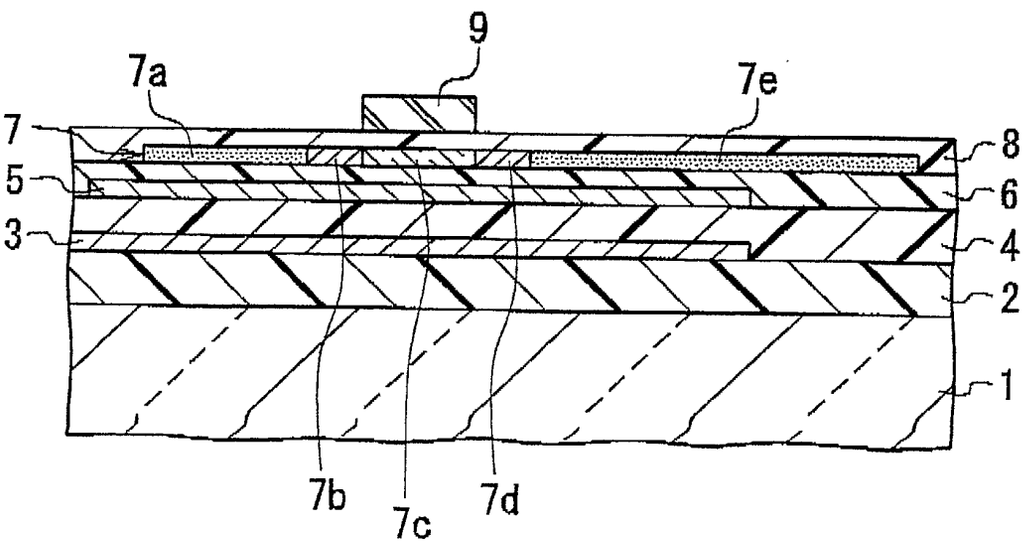


FIG. 10A

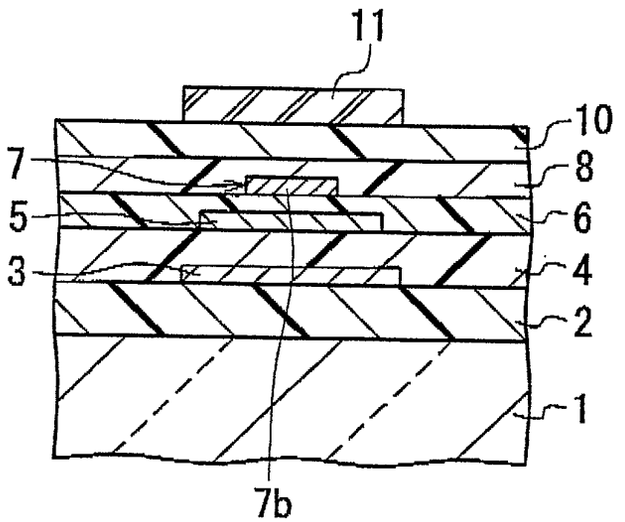


FIG. 10B

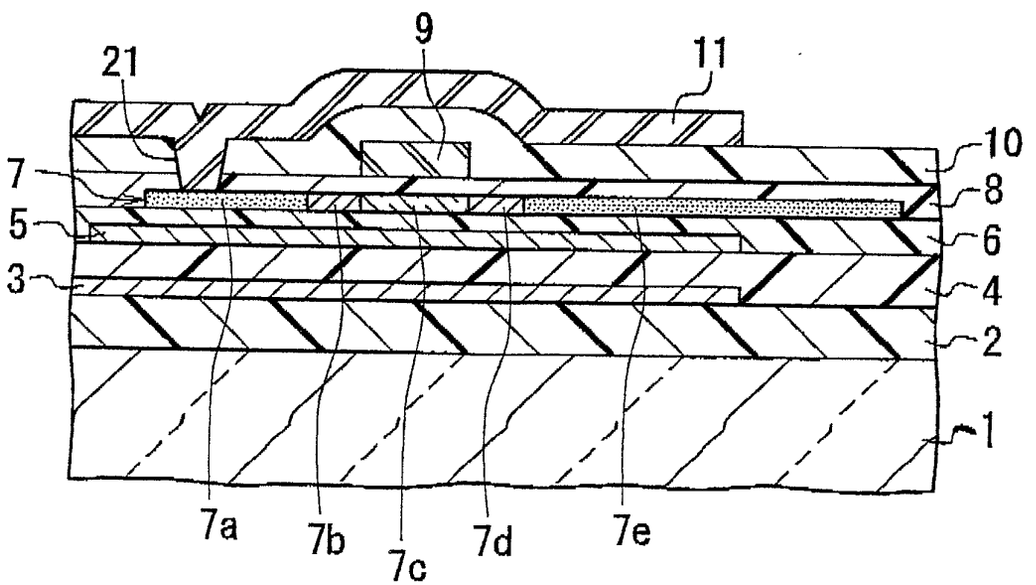


FIG. 11A

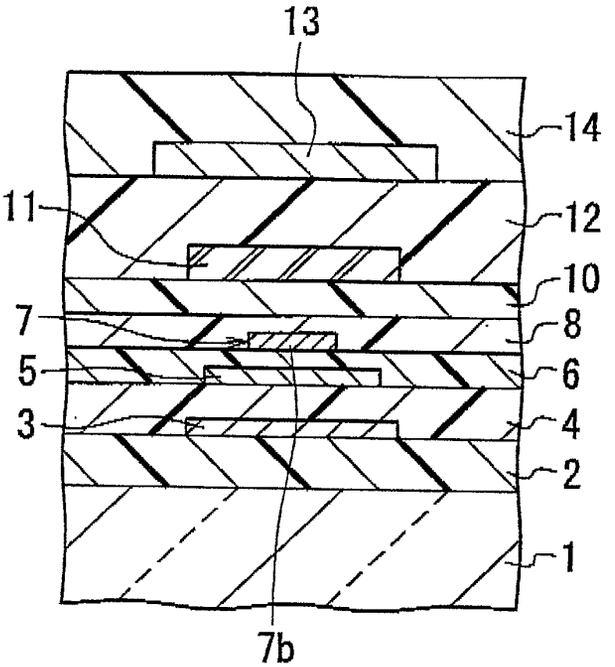


FIG. 11B

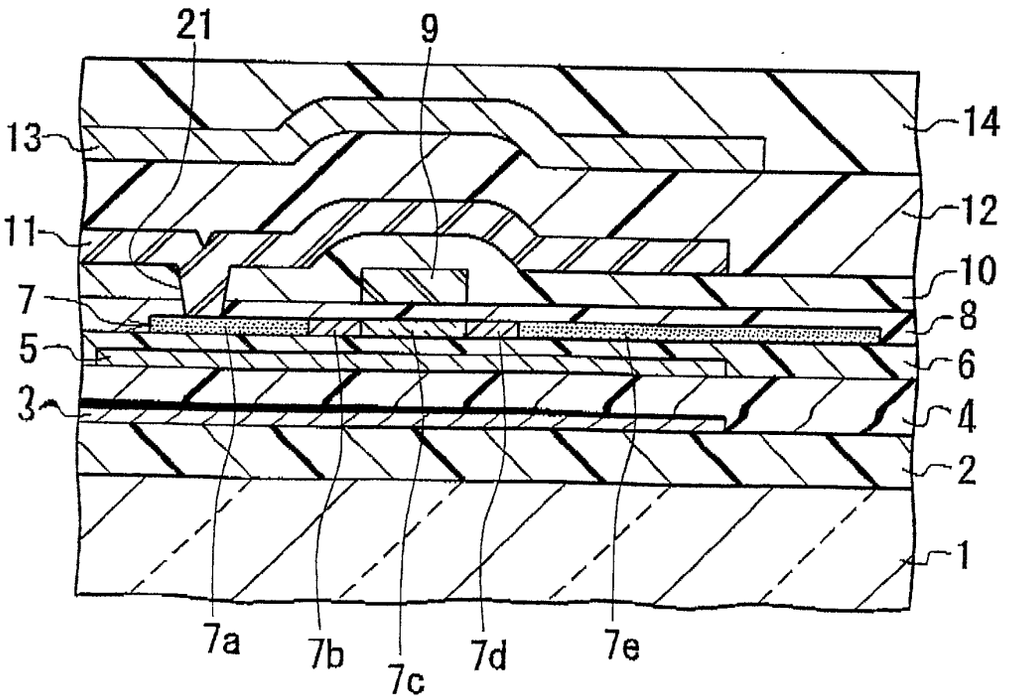


FIG. 12

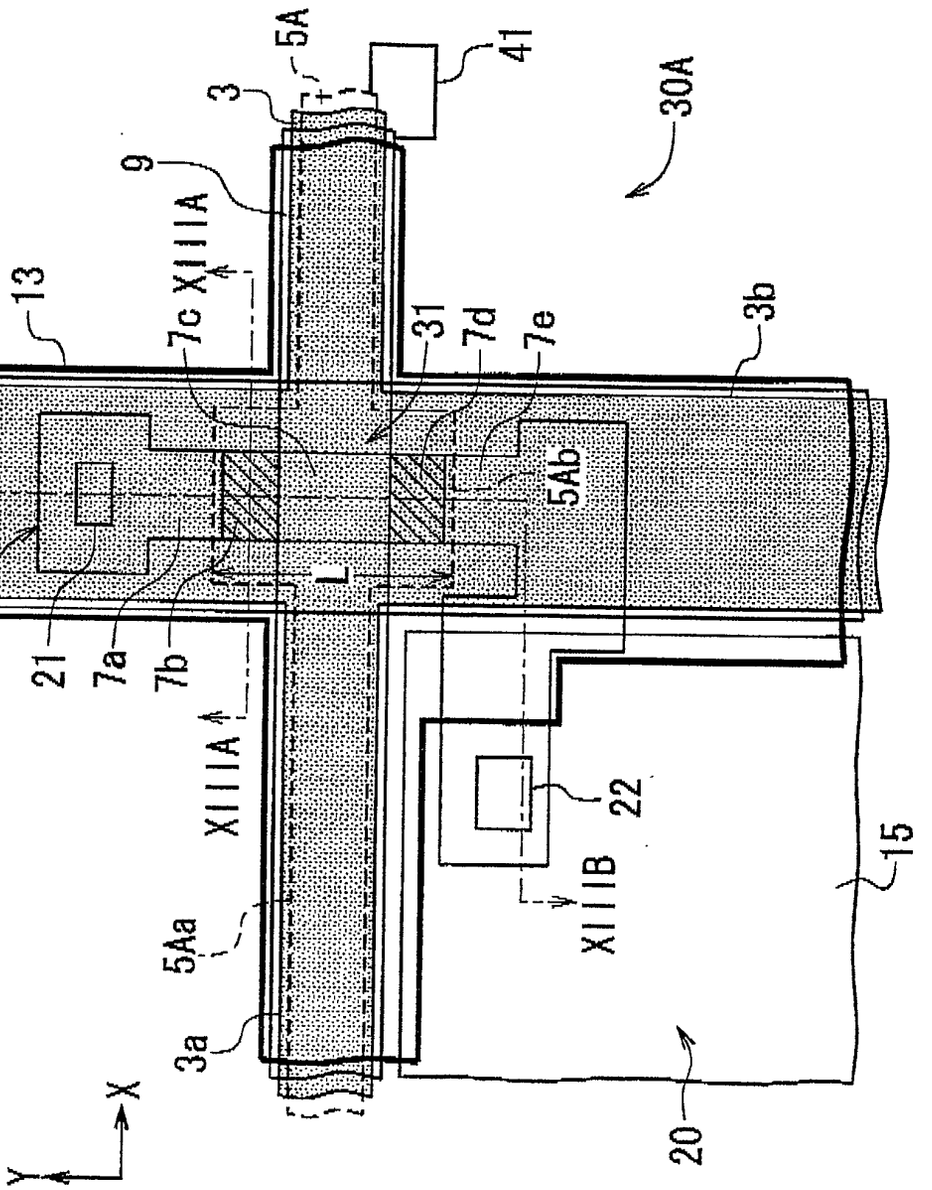

XIIIB
11
13
9
XIIIA
7c
31
7d
7e
3b
5A
41
3
30A
5Ab
L
7
21
7a
7b
XIIIA
22
XIIIB
15
5Aa
3a
20
X
Y

FIG. 13A

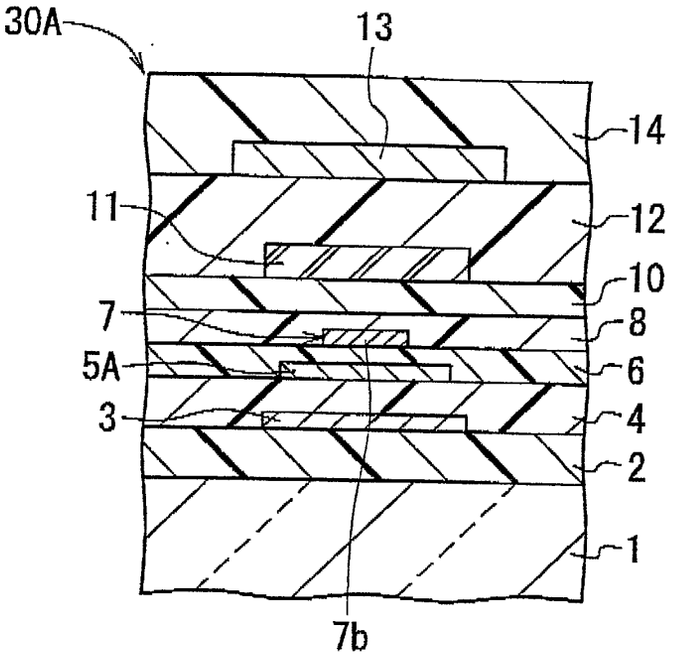


FIG. 13B

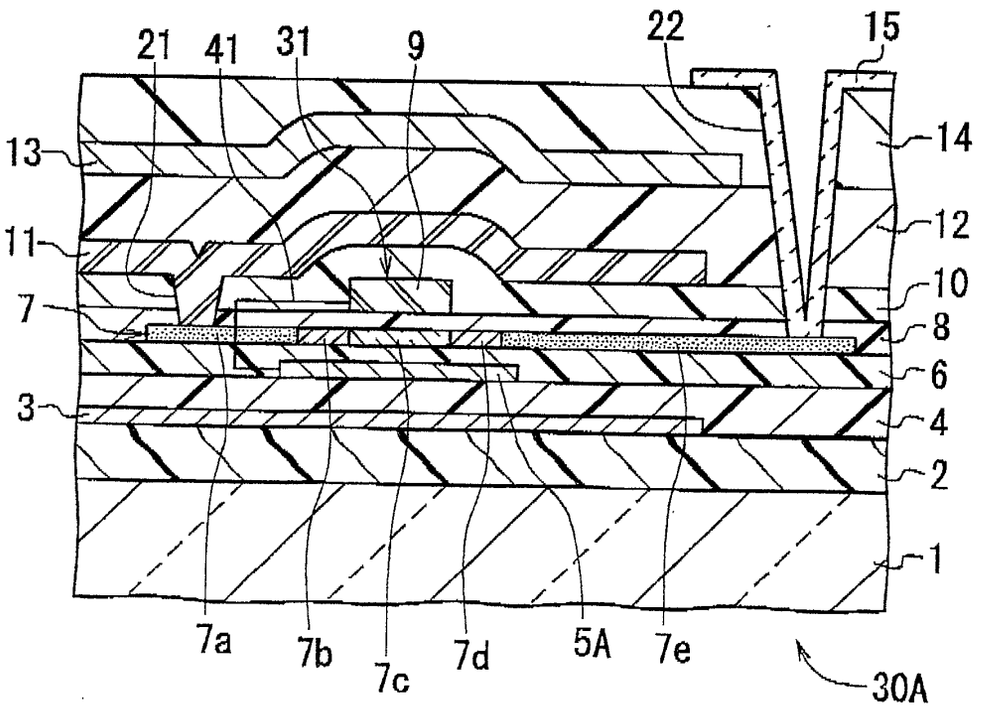


FIG. 14

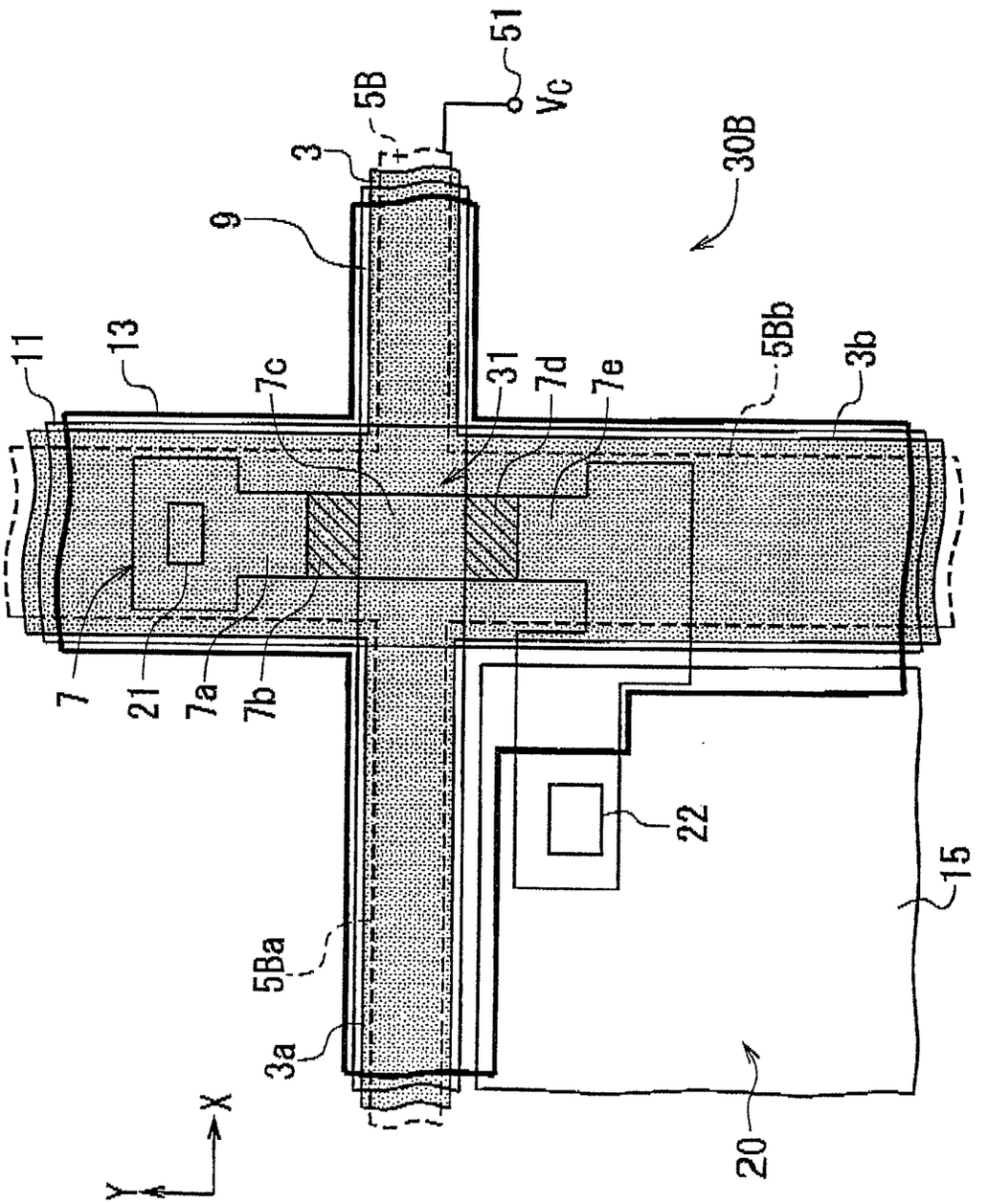


FIG. 15

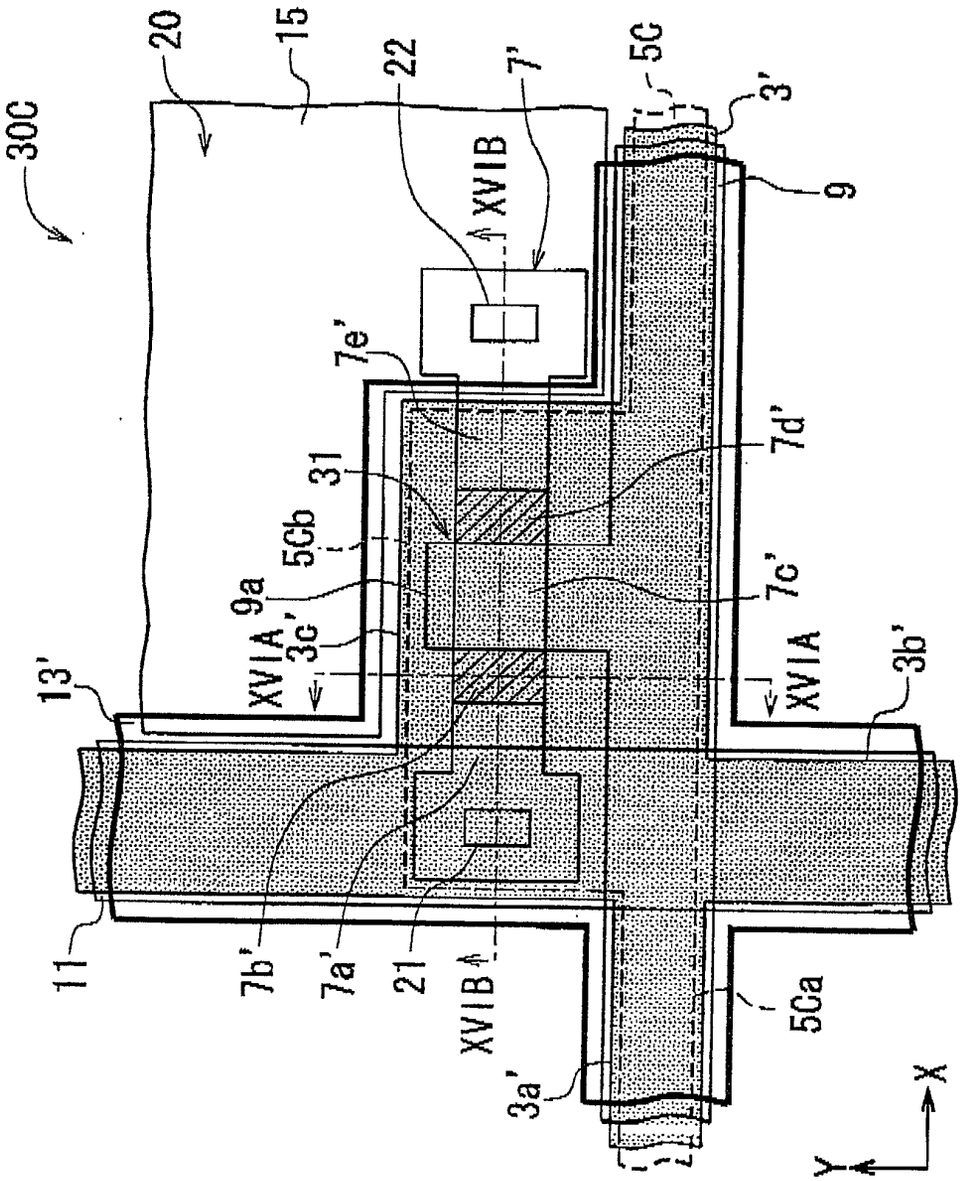

30C
20
15
22
7'
5C
3'
9
XVIB
7e'
7d'
31
5Cb
9a
3c'
XVIA
7c'
13'
3b'
11
7b'
7a'
21
XVIB
5Ca
3a'
X
Y

FIG. 16A

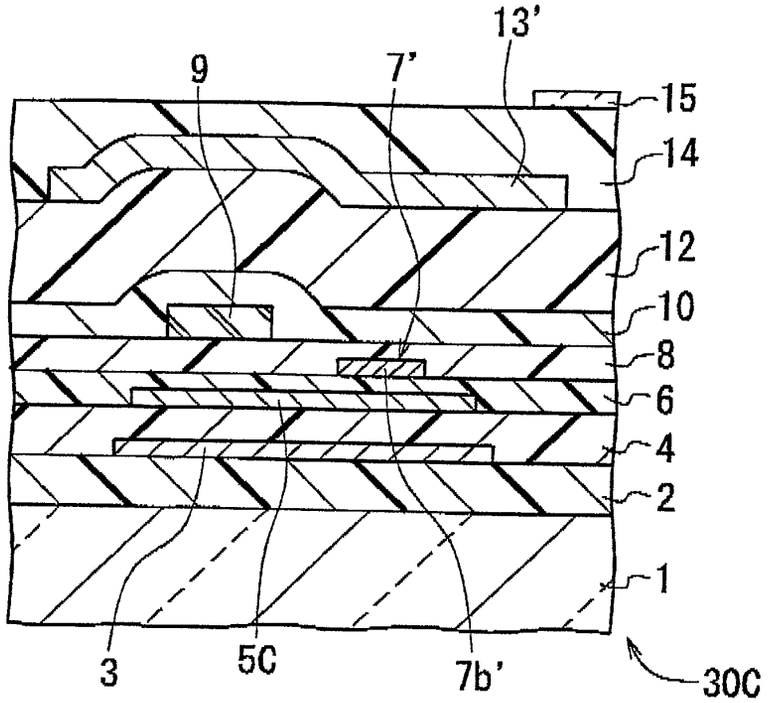


FIG. 16B

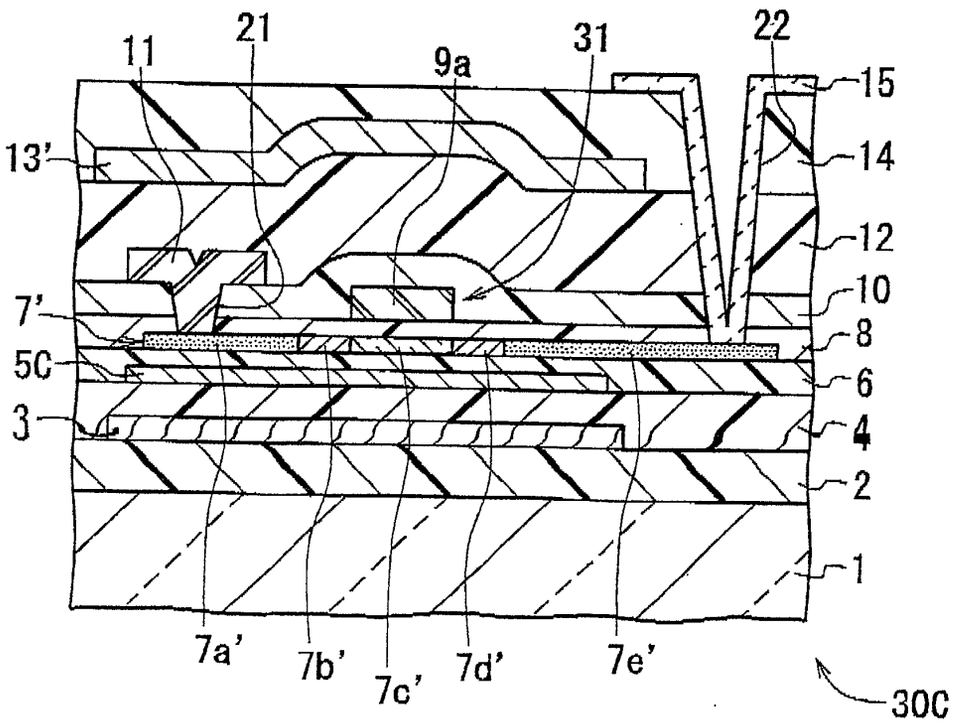


FIG. 17

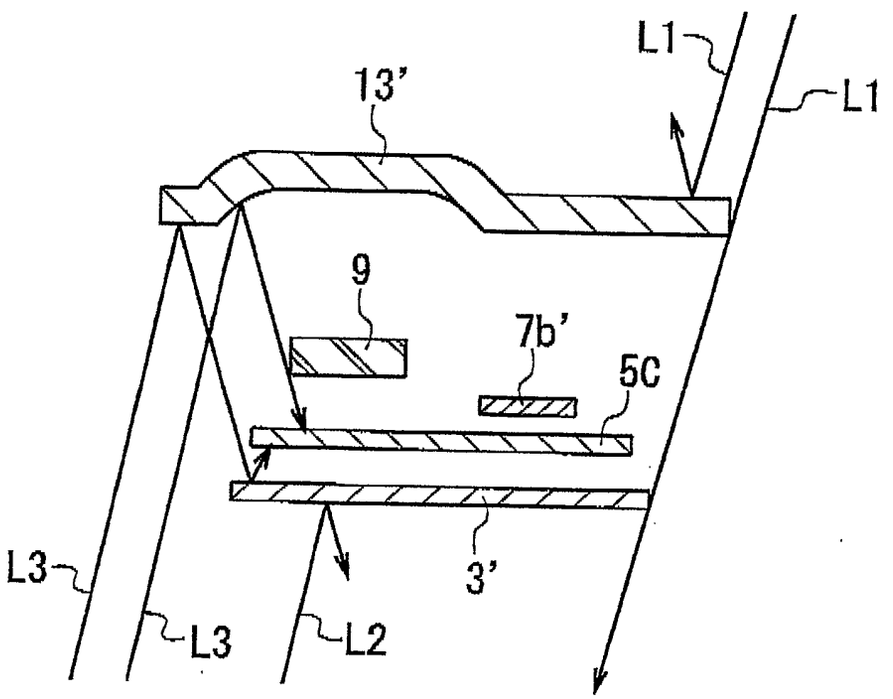


FIG. 18

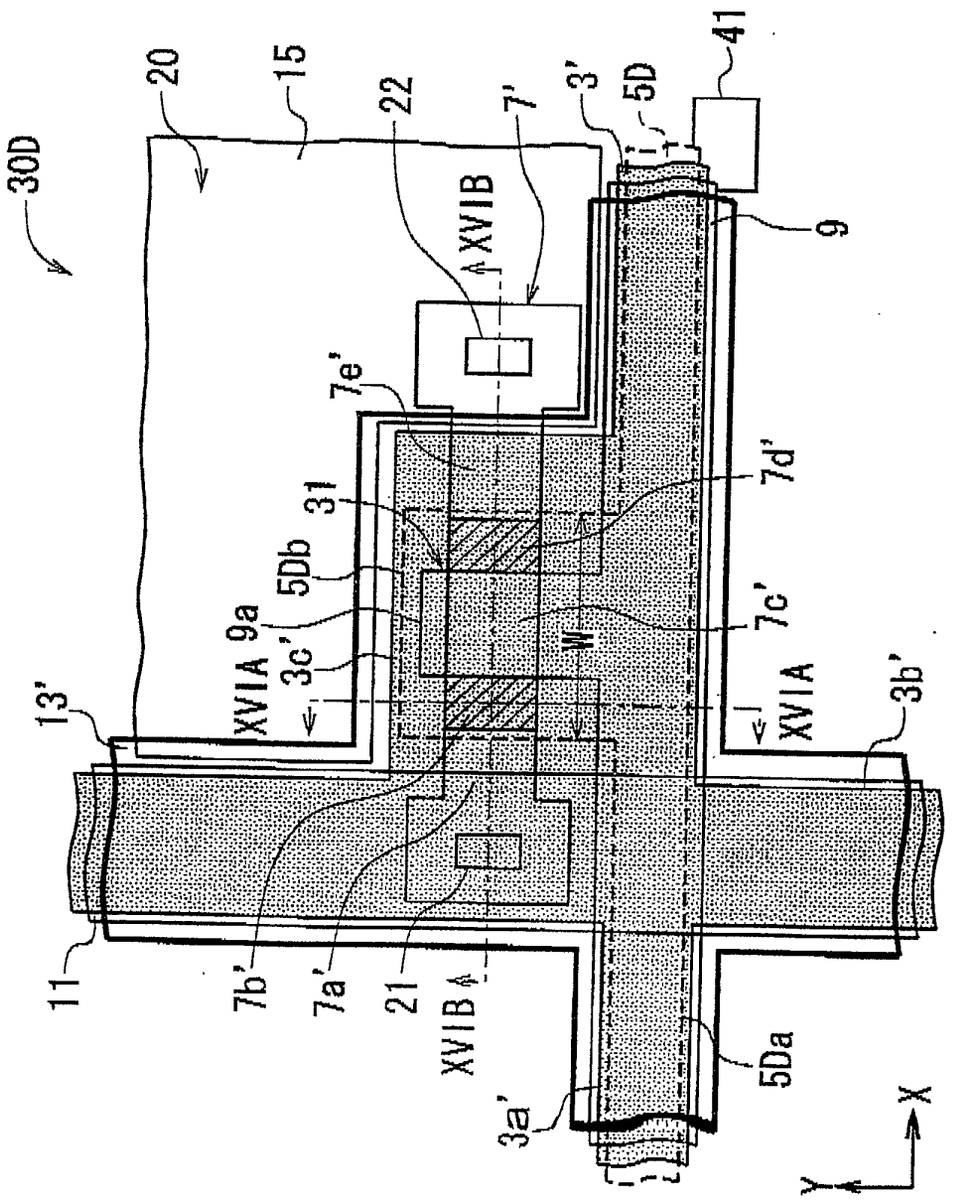

30D
20
15
22
7'
3'
5D
41
XVIB
9
7e'
7d'
31
5Db
9a
XVIA
3c'
7c'
W
13'
XVIA
3b'
11
7b'
7a'
21
XVIB
5Da
3a'
X
Y

FIG. 19

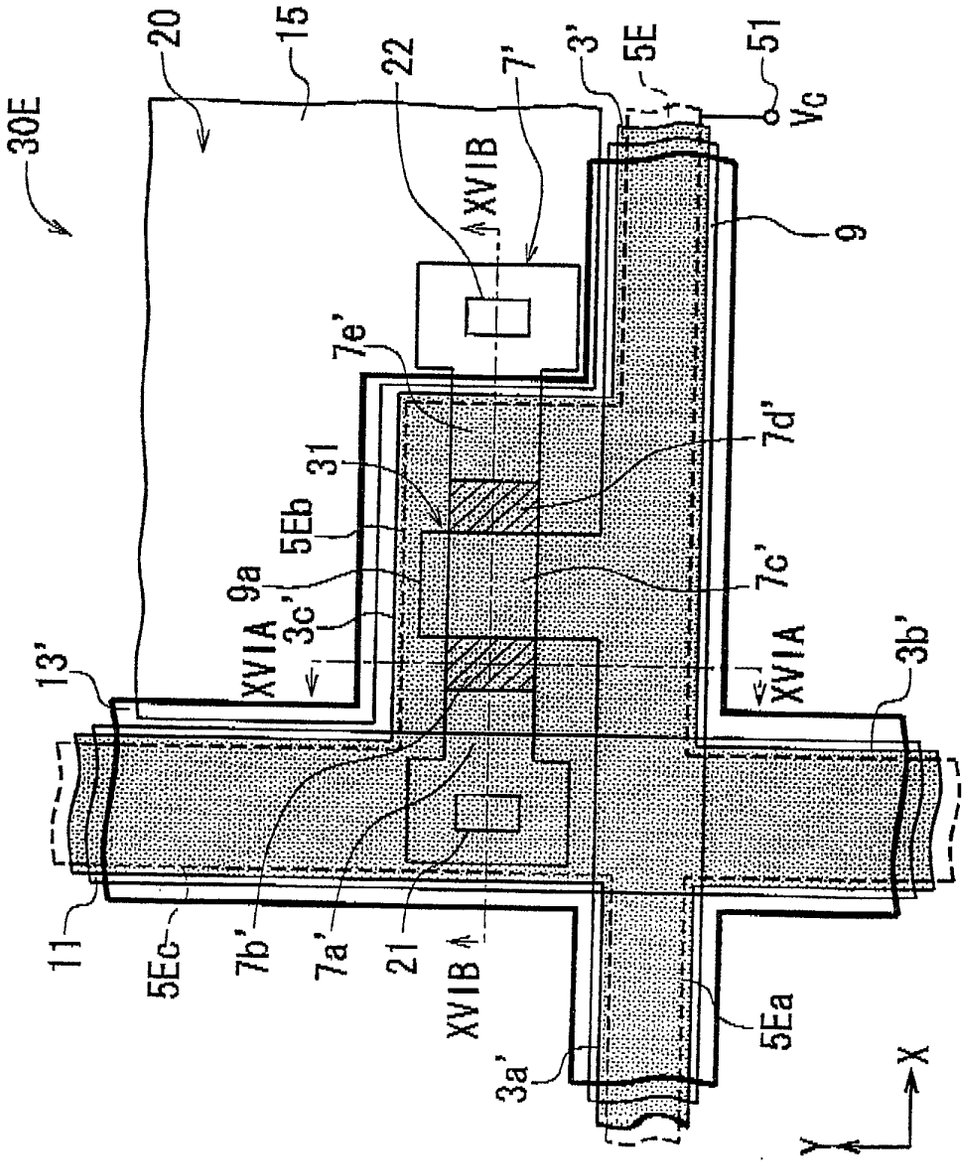

30E
20
15
22
7'
3'
5E
51
Vc
XVIB
9
7e'
7d'
31
5Eb
9a
3c'
XVIA
7c'
13'
3b'
11
5Ec
7b'
7a'
21
XVIB
3a'
5Ea
X
Y

FIG. 20

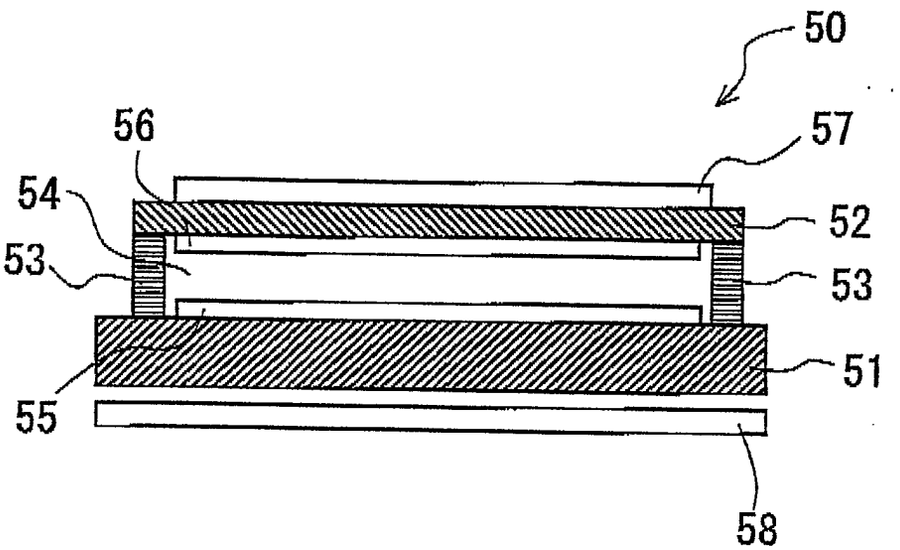


FIG. 21A

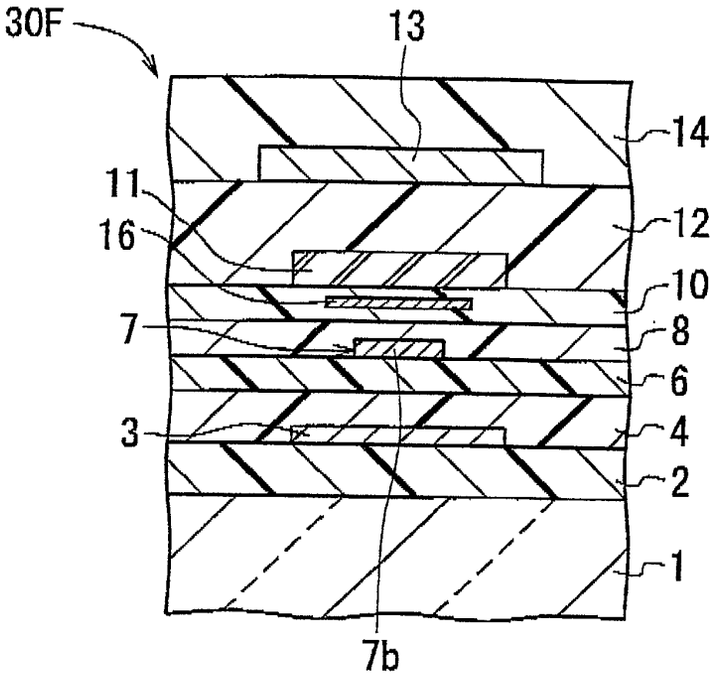


FIG. 21B

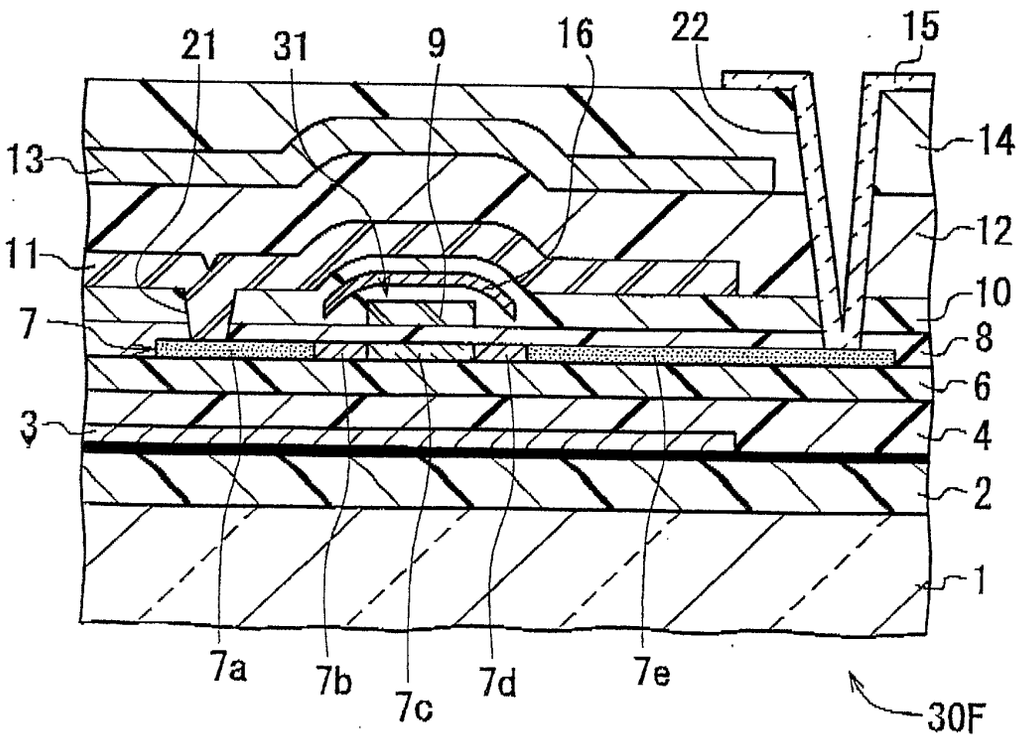


FIG. 22A

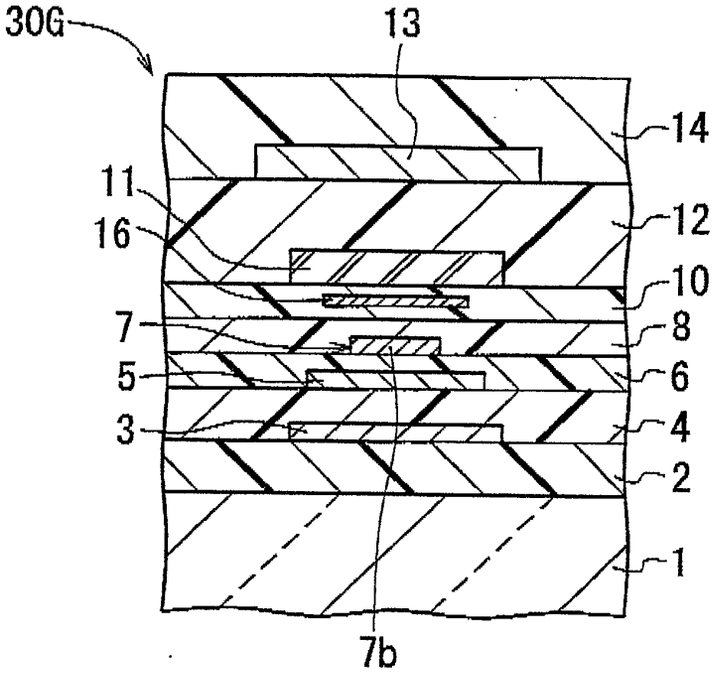


FIG. 22B

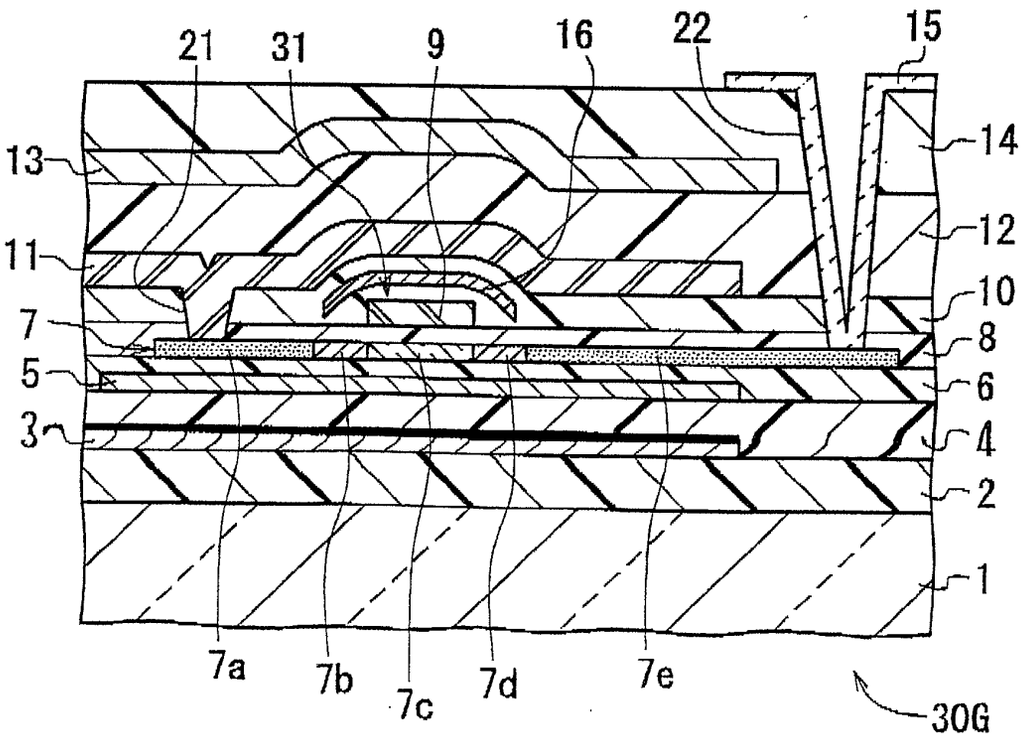


FIG. 23A

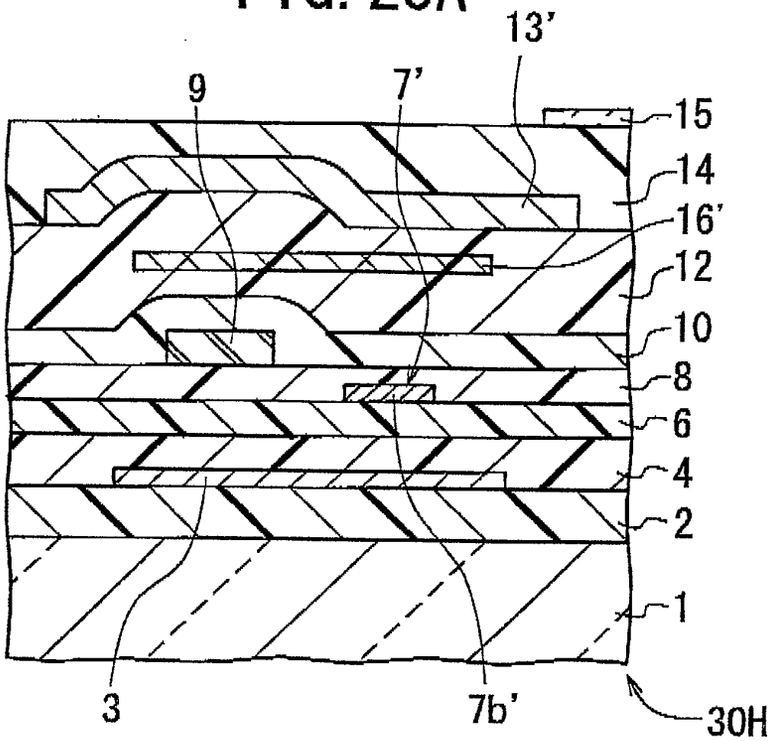


FIG. 23B

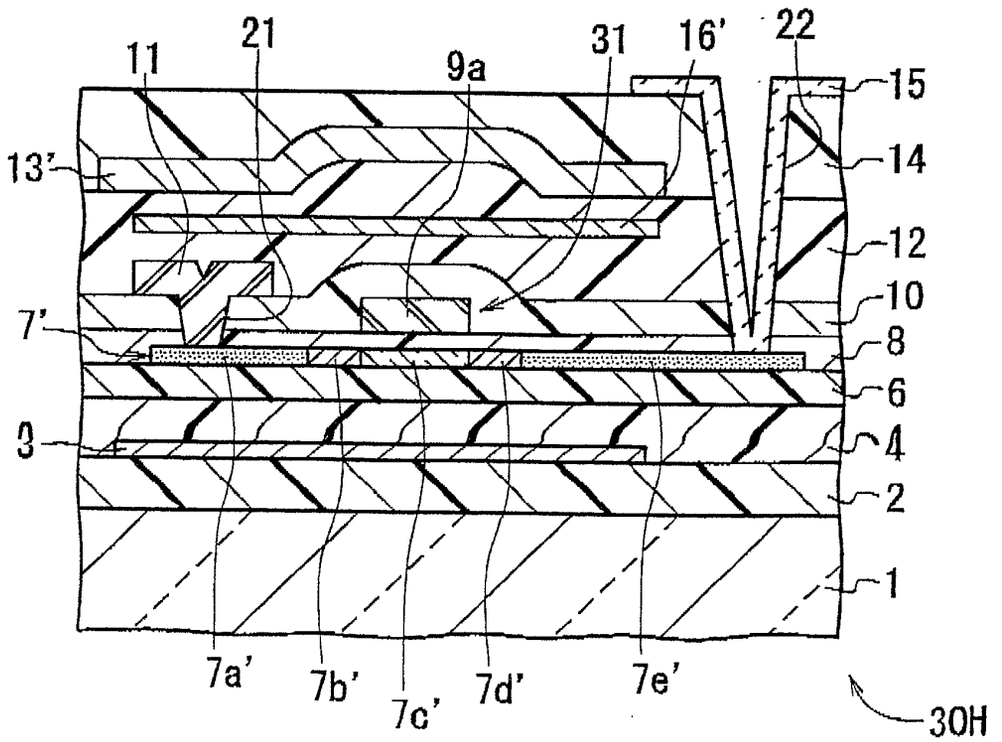


FIG. 24A

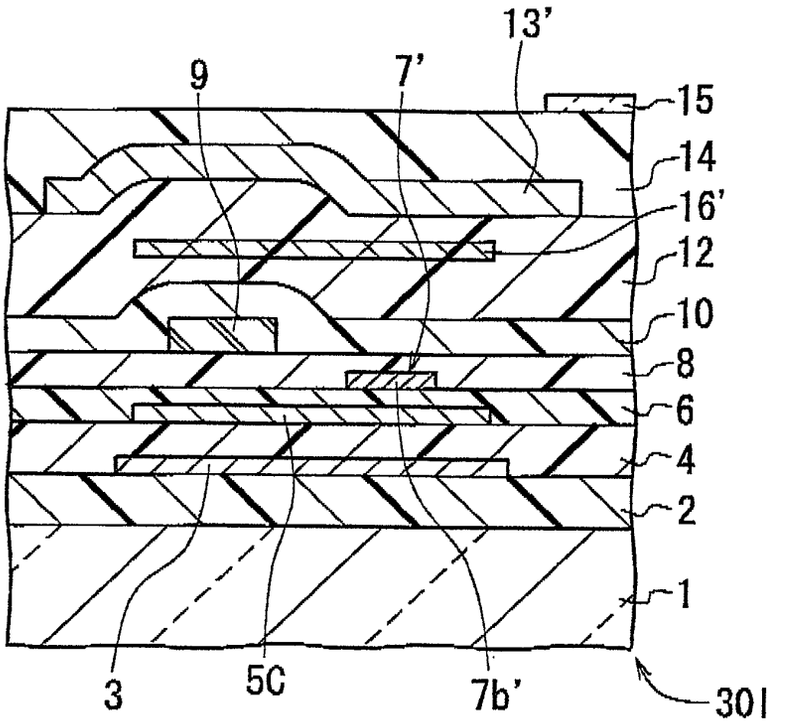


FIG. 24B

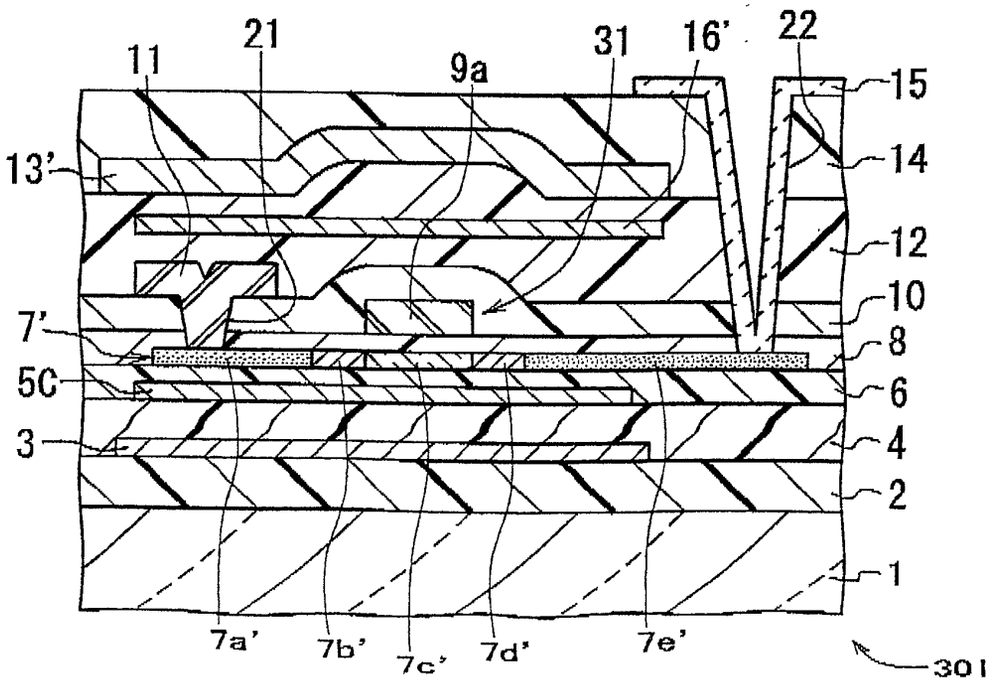


FIG. 25

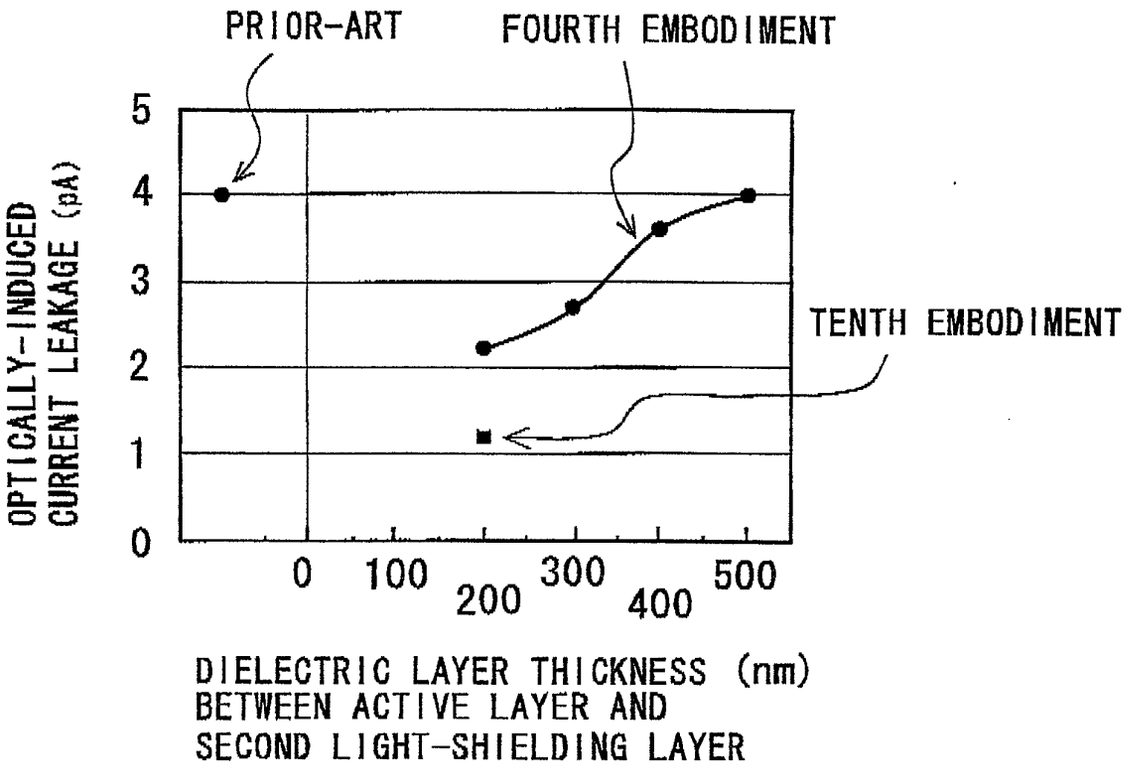
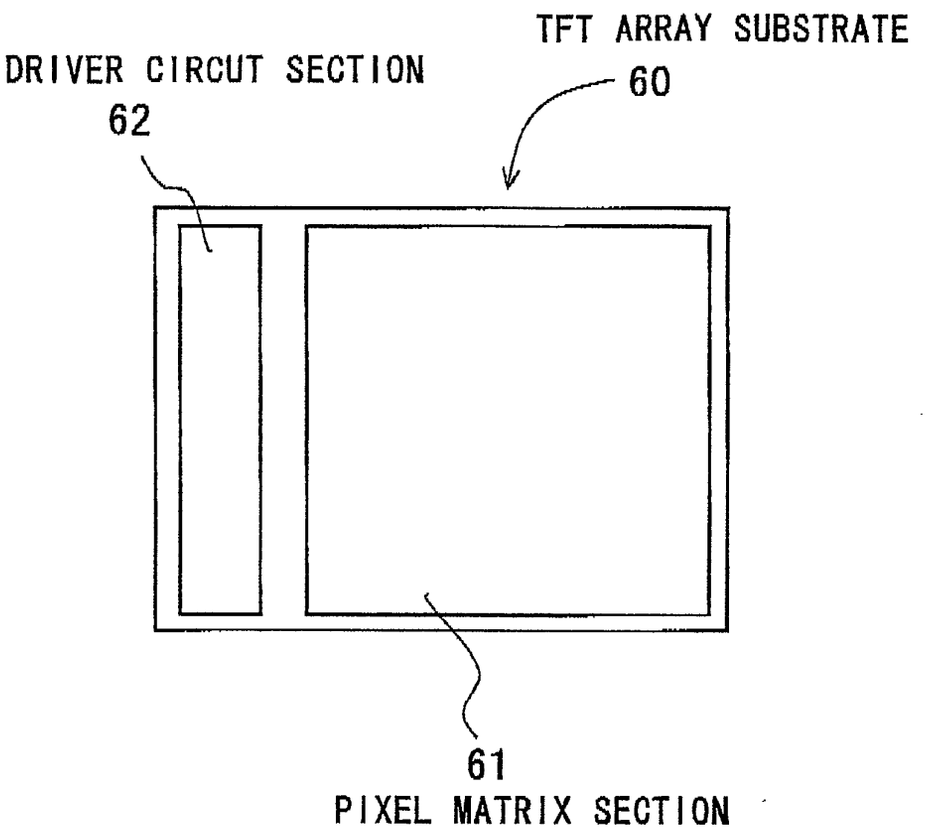

PRIOR-ART
FOURTH EMBODIMENT
TENTH EMBODIMENT
OPTICALLY-INDUCED CURRENT LEAKAGE (pA)
5
4
3
2
1
0
0
100
200
300
400
500
DIELECTRIC LAYER THICKNESS (nm) BETWEEN ACTIVE LAYER AND SECOND LIGHT-SHIELDING LAYER

FIG. 26


TFT ARRAY SUBSTRATE
DRIVER CIRCUT SECTION
60
62
61
PIXEL MATRIX SECTION