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(54) Panel driving device

Einrichtung zum Steuern einer Anzeigetafel

Dispositif de commande d'un panneau d'affichage

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EP-A- 1 085 493
US-A- 6 081 303
US-A- 6 130 657
US-B1- 6 191 768

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Description

[0001] The present invention relates to devices for driving a display panel such as a plasma display panel, and more particularly to a panel driving device capable of displaying correct video images which are in accord with address data.

[0002] As shown in FIG. 7, a driving device for a plasma display panel 21 is provided with: a shift register 115; an address driver section 118 having a latch circuit 116 and a driver 117; a Y sustain driver 119 that outputs Y sustain pulses; and an X sustain driver 120 that outputs X sustain pulses. The output terminals of the driver 117 of the address driver section 118, Y sustain driver 119, and X sustain driver 120 are coupled to predetermined electrodes of the panel 21, respectively.

[0003] As shown in FIG. 8, address data (i.e., data items a to z) for each line are sequentially loaded to the shift register 115 according to respective clock pulses. Also, upon rise of a clock pulse for loading the last data (data item z) for the line, a latch enable signal for activating the latch circuit 116 is risen, so that the address data (data items a to z) for the line are latched and then supplied to the driver 117 simultaneously. Then, scan pulses are selectively applied to any one of the electrodes Y1 to Yn of the panel 21, and simultaneously therewith, data pulses DP1 to DPn corresponding to predetermined address data are applied to its column electrodes D1 to Dm, to illuminate certain cells (where wall charges are stored) and leave other cells nonilluminated (where no wall charges are stored). Successively, sustain pulses are applied through the Y sustain driver 119 and the X sustain driver 120, to selectively allow only the illuminating cells to repetitively emit light.

[0004] However, as shown in FIG. 9, when noise from large power circuitry within the device enters the latch enable signal through small signal circuitry, the noise causes the latch circuit 116 to latch erroneous data. For example, as shown in FIG. 9, a stream of address data erroneously starts with a data item c to have all the data items latched as shifted, hence producing noise spots in the picture displayed on the screen of the plasma display panel 21.

SUMMARY OF THE INVENTION

[0005] US-B1-6191768 (D1) discloses a display drive apparatus comprising a shift register for storing data based on a shift clock, a latch circuit for latching the stored data, a drive circuit for driving a display panel, a control apparatus for intermittent operation of the clock pulses after a regular , timing for causing the latch circuit to latch predetermined data stored in the register.

[0006] An object of the invention is to provide a panel driving device which prevents production of noise spots in the picture displayed on the screen of a display panel even when noise enters small signal circuitry within the device.

[0007] A panel driving device according to the invention is provided with: a shift register (15) for sequentially storing address data according to shift clock pulses; a latch circuit (16) for latching the address data stored in the shift register (15); a drive circuit (17) for driving a display panel (21) based on the address data output from the latch circuit (16); and a clock interrupting device (12, etc.) for interrupting supply of the shift clock pulses to the shift register (15) after a regular timing for causing the latch circuit (16) to latch predetermined address data stored in the shift register (15).

[0008] According to this panel driving device, supply of the shift clock pulses to the shift register is interrupted after the regular timing for latching predetermined address data. Thus, even if predetermined address data are latched by noise after any regular timing, the predetermined address data can be latched as correctly as those latched at the regular timing. As a result, the display panel (21) can provide a display which is in accord with correct address data, without production of noise spots in the displayed picture.

[0009] There may be provided a storage device (3, 4) for storing the address data to be supplied to the shift register (15), a reading device (8) for reading the address data stored in the storage device (3, 4) to load the read address data to the shift register (15). The clock interrupting device (12, etc.) may be provided with a detecting device (12) for detecting an event in which the predetermined address data are not being read by the reading device (8), and while the detecting device (12) detects the event in which the predetermined address data are not being read, supply of the shift clock pulses to the shift register (15) may be interrupted.

[0010] In this case, supply of the shift clock pulses is interrupted while the event is detected in which the predetermined address data are not being read. Thus, even if predetermined address data are latched by noise after any regular timing, the predetermined address data can be latched as correctly as those latched at the regular timing.

[0011] The reading device (8) may output a predetermined signal indicative of the event in which the predetermined address data are not being read, and the detecting device (12) may detect the event in which the predetermined address data are not being read, based on the predetermined signal.

[0012] The clock interrupting device (12, etc.) may include a gate device (12) for selectively triggering passage of another group of clock pulses supplied to the clock interrupting device (12, etc.), as the shift clock pulses, so that the gate device (12) may select passage or non-passage of the shift clock pulses depending on a result of detection performed by the detecting device (12).

[0013] In this case, various logic circuits may be employed as the gate device and the detecting device.

[0014] The clock interrupting device (12, etc.) may include a delay device (13) for adjusting output timing of the shift clock pulses from the gate device (12).

[0015] In this case, through timing adjustment by the delay device, the shift clock pulses can be supplied to the shift register at proper timings, respectively.

[0016] The display panel may be a plasma display panel (21).

[0017] In this case, a plasma display panel driving device which incorporates both large power circuitry and small signal circuitry together can effectively eliminate damage to any displayed picture which would be caused by the entrance of noise from the large power circuitry to the small signal circuitry.

[0018] An address driver (18) for applying data pulses to the plasma display panel (21) may also be provided to select pixels to emit light based on the address data.

[0019] In this case, the panel driving device can effectively eliminate damage to any displayed picture which would be caused by the entrance of noise to the small signal circuitry due to application of sustain pulses.

[0020] Although reference numerals are added in parentheses to the above description to facilitate the understanding of the invention, this should not be construed to limit the invention to the embodiments shown in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

FIG. 1 is a block diagram showing a panel driving device according to an embodiment of the invention;
FIG. 2 is a diagram showing a drive sequence in one field interval;
FIG. 3 is a diagram showing drive waveforms in one subfield;
FIG. 4 is a diagram showing write and read operations to and from frame memories;
FIG. 5 is a diagram showing the read operation from a selected one of the frame memories during an address phase of a subfield;
FIG. 6 is a diagram showing an operation performed by the panel driving device of FIG. 1 when noise enters a latch enable signal;
FIG. 7 is a block diagram showing a prior-art panel driving device;
FIG. 8 is a diagram showing how address data are latched; and
FIG. 9 is a diagram showing an operation performed by the prior-art panel driving device when noise enters a latch enable signal.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0022] Referring now to FIG. 1, a panel driving device 100 according to a preferred embodiment of the invention is provided with: an analog-to-digital (A/D) converter 1 that converts an analog video signal to input video image data; a sync separator 2 that separates a sync signal from the analog video signal and outputs the separated sync signal; first and second frame memories 3 and 4 each of which stores the video image data; a write switch 5 that selects one of the frame memories to which the video image data are to be written; a read switch 6 that selects one of the frame memories from which the video image data are to be read; a write controller 7 that controls the write switch 5; a read controller 8 that controls the read switch 6; a controller 11 that controls various parts of the device; an AND circuit 12 that computes the AND of a first clock pulse from the controller 11 with a signal HA from the read controller 8; and a delay section 13 that adjusts output timing of pulses from the AND circuit 12.

[0023] The panel driving device 100 is further provided with: a shift register 15 that stores address data (pixel data) for each line; an address driver section 18 having a latch circuit 16 and a driver 17; a Y sustain driver 19 that applies Y sustain pulses to sustain electrodes Y1 to Yn simultaneously, and an X sustain driver 20 that applies X sustain pulses to sustain electrodes X1 to Xn simultaneously. The latch circuit 16 of the driver section 18 latches, after address data for each line have been loaded to the shift register 15, the address data for the line, and the driver 17 of the driver section 18 generates data pulses corresponding to the latched address data and applies the generated data pulses to column electrodes D1 to Dm simultaneously.

[0024] In operation, the panel driving device 100 drives a plasma display panel 21 on a field interval basis. A single field interval consists of a plurality of subfields SF1 to SFN. As shown in FIG. 2, each subfield includes an address phase for selecting cells 22 to be illuminated, and a sustain phase for continuously illuminating the selected cells 22. Additionally, a reset phase precedes the first subfield SF1 to completely stop the illumination of the previous field. The durations of the sustain phases of the respective subfields are gradually increased in order of the subfields SF1 to SFN, for gray scale display.

[0025] Referring next to FIG. 3, during the address phase of each subfield, address scanning is performed one line at a time. That is, a scan pulse is applied to the electrode Y1 constituting a first line, and simultaneously therewith, data pulses DP1 corresponding to the address data for cells belonging to the first line are applied to the column electrodes D1 to Dm. Then, a scan pulse is applied to the electrode Y2 constituting a second line, and simultaneously therewith, data pulses DP2 corresponding to the address data for cells belonging to the second line are applied to the column electrodes D1 to Dm. Scan and data pulses are similarly applied to the third and subsequent lines, and finally, a scan pulse is applied to the electrode Yn constituting an nth line, and simultaneously therewith, data pulses DPn corresponding to the address data for cells belonging to the nth line are applied to the column electrodes D 1 to Dm.

[0026] Upon completion of the above address scanning, all the cells in a subfield are either illuminating (wall charges are stored) or nonilluminating (no wall charges

are stored). Every time sustain pulses are applied in the succeeding sustain phase, only the illuminating cells repeat light emission. As shown in FIG. 3, in the sustain phase, X sustain pulses and Y sustain pulses are repetitively applied to the electrodes X1 to Xn and electrodes Y1 to Yn at predetermined timings, respectively.

[0027] Referring now to FIG. 4, how data pulses are generated based on address data will be described. The address data from the A/D converter 1 are written, field by field, alternately to the first frame memory 3 and the second frame memory 4 as selected by the write switch 5. The input video image data in the first and second frame memories 3 and 4 are read alternately from the first and second frame memories 3 and 4 as selected by the read switch 6 one field behind that of their write timing.

[0028] The address data read from the first or second frame memory 3 or 4 are sequentially loaded to the shift register one line at a time according to respective second clock (shift clock) pulses. As shown in FIG. 6, a latch enable signal to be input to the latch circuit 16 rises upon rise of a second clock pulse for loading the last data item z for each line, and thus the address data for the line (e.g., data items a to z) are latched and then supplied to the driver 17 simultaneously. Then, a scan pulse is applied to the corresponding one of the electrodes Y1 to Yn as mentioned above, and at the same time, data pulses DP1 to DPn corresponding to the read line-based address data are applied to the corresponding column electrodes D 1 to Dm.

[0029] As shown in FIG. 5, the signal HA is output from the read controller 8 while the address data are read one line at a time from the first or second frame memory 3 or 4. Referring back to FIG. 1 here, both the signal HA and each first clock pulse from the controller 11 are fed to the AND circuit 12 to trigger passage of the first clock pulse so that each of second clock pulses is output only while the signal HA is being output (the level of the signal HA is high). That is, while the address data are not read from the first or second frame memory 3 or 4, no second clock pulses are output. Each second clock pulse passes through the delay section 13 to have its timing adjusted before output to the shift register 15.

[0030] Thus, in this embodiment, there is a pause in the supply of second clock pulses whenever there is a pause in reading address data for each line from one of the frame memories, and this means that the shift register 15 keeps its data unupdated during each pause, to keep therein the address data which have been correctly read upon rise of the last regular latch enable signal. As a result, as shown in FIG. 6, even if noise from large power circuitry is accidentally superimposed upon the latch enable signal, the data latched by the noise is as correct as address data read by the regular latch enable signal. Therefore, even if address data are latched at an abnormal timing by noise, the address data can be read correctly, to supply the plasma display panel 21 with data pulses which are in accord with the correctly read address data, and hence the picture displayed on the panel 21 includes no noise marks.

[0031] As described in the foregoing, according to the panel driving device of the invention, supply of shift clock pulses to the shift register is interrupted after each regular latch timing for reading predetermined address data. Thus, even if the latching of address data is triggered by noise after a regular timing, the device keeps latching correct address data. As a result, the display panel provides a display which is in accord with the correct address data on its screen, with no noise marks present in the picture displayed on its screen.

Claims

1. A display panel driving device comprising:

a shift register (15) adapted to sequentially store address data according to shift clock pulses;
a latch circuit (16) adapted to latch the address data stored in the shift register;
a drive circuit (17) adapted to drive a display panel (21) based on the address data output from the latch circuit; **characterised in that** said display panel further comprises
a clock interrupting device (12) adapted to interrupt supply of the shift clock pulses to the shift register after a regular timing for causing the latch circuit to latch predetermined address data stored in the shift register,

wherein said clock interrupting device (12) includes a detecting device (12) adapted to detect an event in which the predetermined address data are not being read by a reading device, and said clock interrupting device (12) being also adapted to interrupt supply of the shift clock pulses to the shift register while said detecting device adapted to detect the event in which the predetermined address data are not being read.

2. The panel driving device according to claim 1, wherein said display panel driving device further comprises:

a storage device (3, 4) adapted to store the address data to be supplied to the shift register; and the reading device (8) is adapted to read the address data stored in the storage device to load the read address data to the shift register.

3. The display panel driving device according to claim 2, wherein said reading device (8) is adapted to output a predetermined signal indicative of the event in which the predetermined address data are not being read, and said detecting device is adapted to detect the event based on the predetermined signal.

4. The display panel drive device according to claim 2 or 3, wherein said clock interrupting device (12) includes a gate device (12) adapted to selectively trigger passage of another group of clock pulses supplied to said clock interrupting device, as the shift clock pulses, so that said gate device is adapted to select passage or nonpassage of the shift clock pulses depending on a result of detection performed by said detecting device (12).

5. The display panel driving device according to claims 4 wherein said clock interrupting device (12) includes a delay device (13) adapted to adjust output timing of the shift clock pulses from the gate device.

6. The display panel driving device according to any one of claims 1 to 5,
wherein said display panel is a plasma display panel (21).

7. The display panel driving device according to claim 6, further comprising a light emission maintenance device adapted to apply sustain pulses to the plasma display panel to cause selected pixels to continuously emit light, the pixels being selected based on the address data.

Patentansprüche

1. Ansteuereinrichtung für ein Anzeigefeld, mit:

einem Schieberegister (15), das zur sequenziellen Speicherung von Adressendaten entsprechend Schiebetakt-Impulsen ausgebildet ist;
einer Signalspeicherschaltung (16), die zum Speichern der in dem Schieberegister gespeicherten Daten ausgebildet ist;
einer Ansteuerschaltung (17), die zur Ansteuerung des Anzeigefeldes (21) auf der Grundlage des Adressendaten-Ausganges von der Signalspeicherschaltung ausgebildet ist;

dadurch gekennzeichnet, dass das Anzeigefeld weiterhin Folgendes umfasst:

eine Taktunterbrechungseinrichtung (12), die zur Unterbrechung der Zuführung der Schiebetaktimpulse an das Schieberegister nach einer regulären Zeitsteuerung ausgebildet ist, um zu bewirken, dass die Signalspeicherschaltung vorgegebene Adressendaten speichert, die in dem Schieberegister gespeichert sind,

wobei die Taktunterbrechungseinrichtung (12) eine Detektoreinrichtung (12) einschließt, die zur Feststellung eines Ereignisses ausgebildet ist, bei dem die vorgegebenen Adressendaten nicht von einer Leseeinrichtung gelesen werden, und
wobei die Taktunterbrechungseinrichtung (12) weiterhin so ausgebildet ist, dass sie die Zuführung der Schiebetaktimpulse an das Schieberegister unterbricht, während die Detektoreinrichtung so ausgebildet ist, dass sie das Ereignis feststellt, bei dem die vorgegebenen Adressendaten nicht gelesen werden.

2. Ansteuereinrichtung für ein Anzeigefeld nach Anspruch 1, wobei die Ansteuereinrichtung für das Anzeigefeld weiterhin Folgendes umfasst:

eine Speichereinrichtung (3, 4), die zur Speicherung der an das Schieberegister zu liefernden Adressendaten ausgebildet ist; und

wobei die Leseeinrichtung (8) so ausgebildet ist, dass sie die in der Speichereinrichtung gespeicherten Adressendaten liest, um die Adressendaten in das Schieberegister zu laden.

3. Ansteuereinrichtung für ein Anzeigefeld gemäß Anspruch 2, bei der die Leseeinrichtung (8) so ausgebildet ist, dass sie ein vorgegebenes Signal abgibt, das das Ereignis anzeigt, bei dem die vorgegebenen Adressendaten nicht gelesen werden, und dass die Detektoreinrichtung so ausgebildet ist, dass sie das Ereignis auf der Grundlage des vorgegebenen Signals feststellt.

4. Ansteuereinrichtung für ein Anzeigefeld nach Anspruch 2 oder 3, bei der die Taktunterbrechungseinrichtung (12) eine Gattereinrichtung (12) einschließt, die so ausgebildet ist, dass sie selektiv das Hindurchlaufen einer anderen Gruppe von der Taktunterbrechungseinrichtung zugeführten Taktimpulsen triggert, als die Schiebetakt-Impulse, so dass die Gattereinrichtung so ausgebildet ist, dass sie das Hindurchlaufen oder Nicht-Hindurchlaufen der Schiebetakt-Impulse in Abhängigkeit von einem Ergebnis der Detektion auswählt, die von der Detektoreinrichtung (12) ausgeführt wird.

5. Ansteuereinrichtung für ein Bedienfeld nach Anspruch 4, bei der die Taktunterbrechungseinrichtung (12) eine Verzögerungseinrichtung (13) einschließt, die so ausgebildet ist, dass sie die Ausgangs-Zeitsteuerung der Schiebetakt-Impulse von der Gattereinrichtung einstellt.

6. Ansteuereinrichtung für ein Anzeigefeld nach einem der Ansprüche 1-5, bei der das Anzeigefeld ein Plasma-Anzeigefeld (21) ist.

7. Ansteuereinrichtung für ein Anzeigefeld nach Anspruch 6, die weiterhin eine Lichtemissions-Aufrechterhaltungseinrichtung umfasst, die zur Auf-

rechterhaltung von Impulsen an das Plasma-Anzeigefeld ausgebildet ist, um zu bewirken, dass ausgewählte Pixel kontinuierlich Licht aussenden, wobei die Pixel auf der Grundlage der Adressendaten ausgewählt sind.

Revendications

1. Dispositif de commande d'un écran d'affichage, comprenant :

un registre à décalage (15) conçu pour mémoriser successivement des données d'adresses conformément à des impulsions d'horloge à décalage ;
un circuit à verrouillage (16) conçu pour verrouiller les données d'adresses mémorisées dans le registre à décalage ;
un circuit d'entraînement (17) conçu pour entraîner un écran d'affichage (21) en se basant sur les données d'adresses émises par le circuit à verrouillage ; **caractérisé en ce que** ledit écran d'affichage comprend en outre :

un dispositif d'interruption d'horloge (12) conçu pour interrompre l'acheminement des impulsions d'horloge à décalage au registre à décalage à des intervalles de temps réguliers pour faire en sorte que le circuit à verrouillage verrouille les données d'adresses prédéterminées mémorisées dans le registre à décalage ;
ledit dispositif d'interruption d'horloge (12) englobant un dispositif de détection (12) conçu pour détecter un événement dans lequel les données d'adresses prédéterminées ne sont pas lues par un dispositif de lecture, et ledit dispositif d'interruption d'horloge (12) étant également conçu pour interrompre l'acheminement des impulsions d'horloge à décalage au registre à décalage lorsque ledit dispositif de détection détecte l'événement dans lequel les données d'adresses prédéterminées ne sont pas lues.

2. Dispositif de commande d'écran d'affichage selon la revendication 1, dans lequel ledit dispositif d'entraînement d'écran d'affichage comprend en outre :

un dispositif de stockage (3, 4) conçu pour stocker les données d'adresses à acheminer au registre à décalage ;
le dispositif de lecture (8) étant conçu pour lire les données d'adresses mémorisées dans le dispositif de stockage afin de charger le registre à décalage avec les données d'adresses lues.

3. Dispositif de commande d'écran d'affichage selon la revendication 2, dans lequel ledit dispositif de lecture (8) est conçu pour émettre un signal prédéterminé signalant l'événement dans lequel les données d'adresses prédéterminées ne sont pas lues, ledit dispositif de détection étant conçu pour détecter l'événement en se basant sur le signal prédéterminé.

4. Dispositif de commande d'écran d'affichage selon la revendication 2 ou 3, dans lequel ledit dispositif d'interruption d'horloge (12) englobe un dispositif faisant office de porte logique (12) qui est conçu pour déclencher de manière sélective le passage d'un autre groupe d'impulsions d'horloge acheminé audit dispositif d'interruption d'horloge, au titre des impulsions d'horloge à décalage, si bien que ledit dispositif faisant office de porte logique est conçu pour opérer une sélection entre le passage et le non passage des impulsions d'horloge à décalage en fonction du résultat de la détection mise en oeuvre par ledit dispositif de détection (12).

5. Dispositif de commande d'écran d'affichage selon la revendication 4, dans lequel ledit dispositif d'interruption d'horloge (12) englobe un dispositif de retardement (13) conçu pour régler le moment correspondant à l'émission des impulsions d'horloge à décalage à partir du dispositif faisant office de porte logique.

6. Dispositif de commande d'écran d'affichage selon l'une quelconque des revendications 1 à 5, dans lequel ledit écran d'affichage est un écran d'affichage à plasma (21).

7. Dispositif de commande d'écran d'affichage selon la revendication 6, comprenant en outre un dispositif de maintien de l'émission de lumière, conçu pour appliquer des impulsions d'entretien à l'écran d'affichage à plasma pour faire en sorte que des pixels sélectionnés émettent de la lumière en continu, les pixels étant sélectionnés sur base des données d'adresses.

FIG. 1

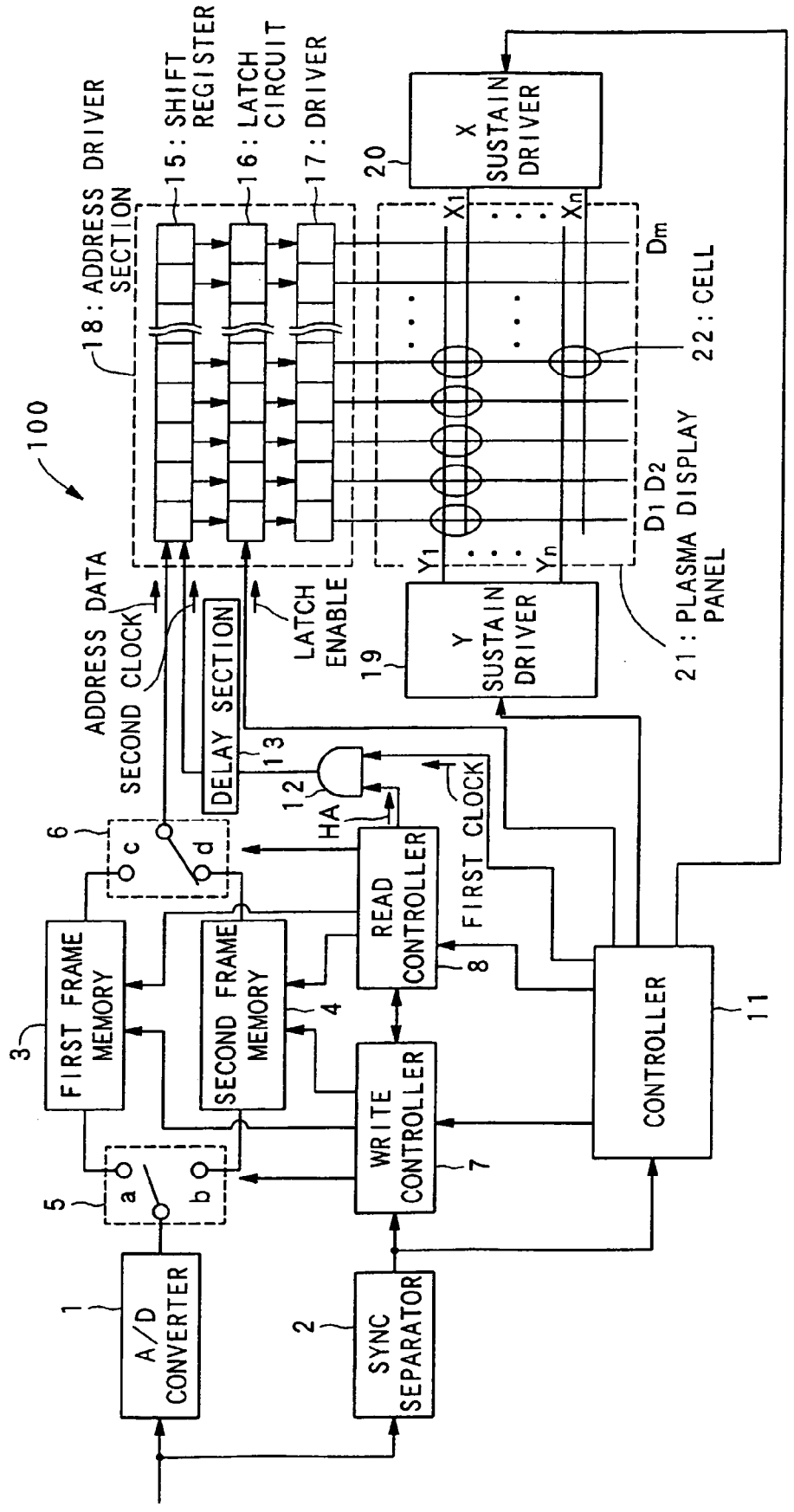

100
1 A/D CONVERTER
2 SYNC SEPARATOR
3 FIRST FRAME MEMORY
4 SECOND FRAME MEMORY
5
6
7 WRITE CONTROLLER
8 READ CONTROLLER
11 CONTROLLER
12 HA
13 DELAY SECTION
15: SHIFT REGISTER
16: LATCH CIRCUIT
17: DRIVER
18: ADDRESS DRIVER SECTION
19 Y SUSTAIN DRIVER
20 X SUSTAIN DRIVER
21: PLASMA DISPLAY PANEL
22: CELL
ADDRESS DATA
SECOND CLOCK
LATCH ENABLE
FIRST CLOCK
a
b
c
d
X1
Xn
Y1
Yn
D1 D2
Dm

FIG. 2

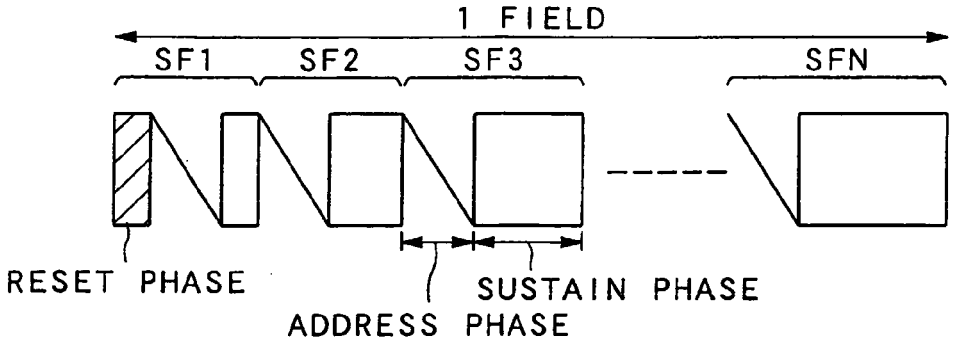

1 FIELD
SF1
SF2
SF3
SFN
RESET PHASE
ADDRESS PHASE
SUSTAIN PHASE

FIG. 3

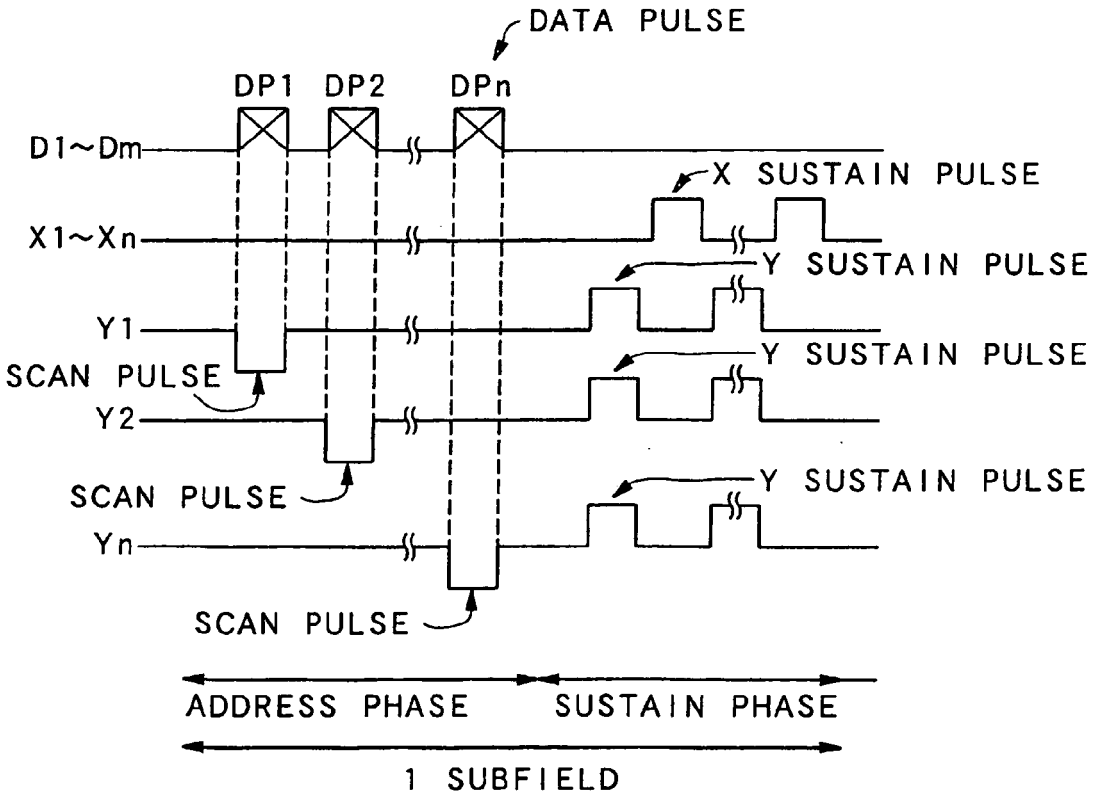

DATA PULSE
DP1
DP2
DPn
D1~Dm
X1~Xn
Y1
SCAN PULSE
Y2
SCAN PULSE
Yn
SCAN PULSE
X SUSTAIN PULSE
Y SUSTAIN PULSE
Y SUSTAIN PULSE
Y SUSTAIN PULSE
ADDRESS PHASE
SUSTAIN PHASE
1 SUBFIELD

FIG. 4

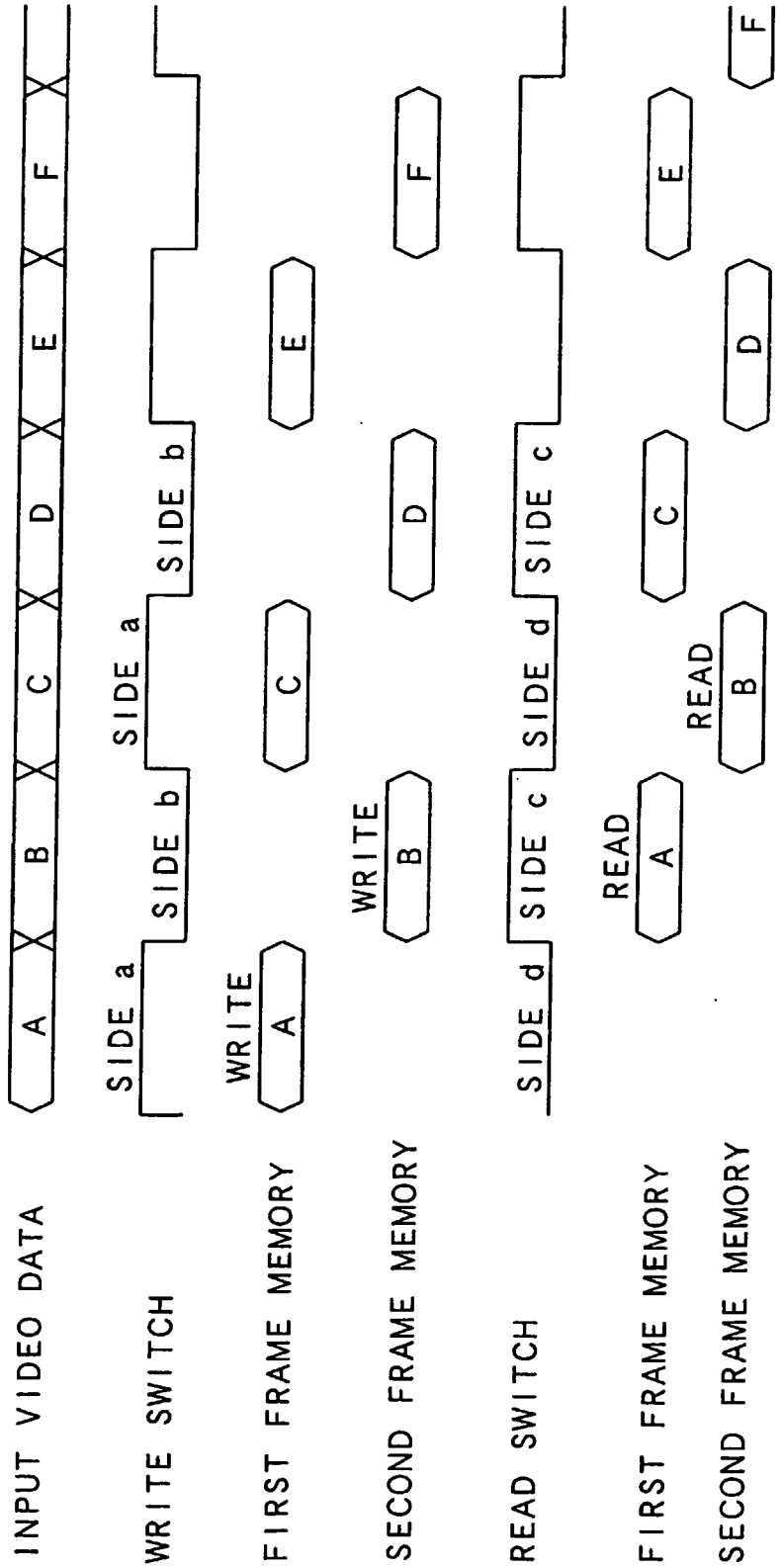

1 FIELD
INPUT VIDEO DATA
A
B
C
D
E
F
WRITE SWITCH
SIDE a
SIDE b
SIDE a
SIDE b
FIRST FRAME MEMORY
WRITE
A
C
E
SECOND FRAME MEMORY
WRITE
B
D
F
READ SWITCH
SIDE d
SIDE c
SIDE d
SIDE c
FIRST FRAME MEMORY
READ
A
C
E
SECOND FRAME MEMORY
READ
B
D
F

FIG. 5

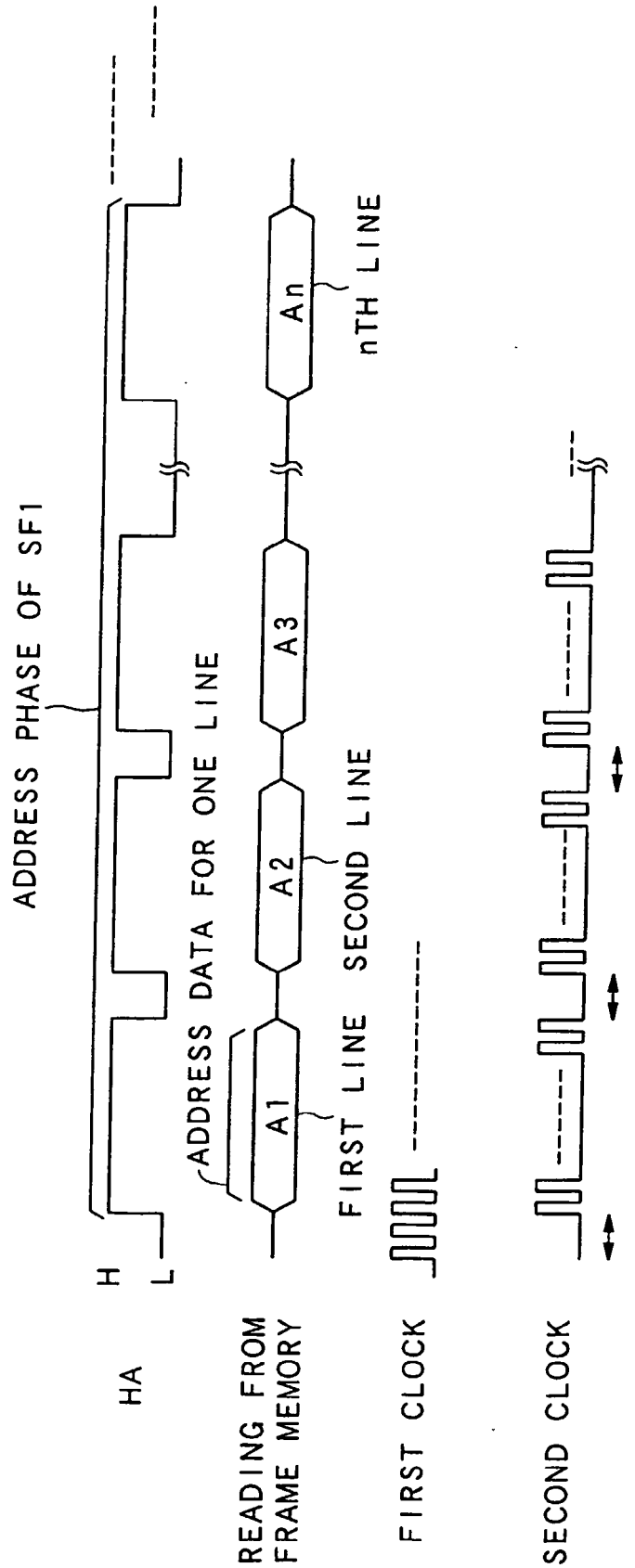

ADDRESS PHASE OF SF1
ADDRESS DATA FOR ONE LINE
A1
A2
A3
An
nTH LINE
FIRST LINE
SECOND LINE
H
L
HA
READING FROM FRAME MEMORY
FIRST CLOCK
SECOND CLOCK

FIG. 6

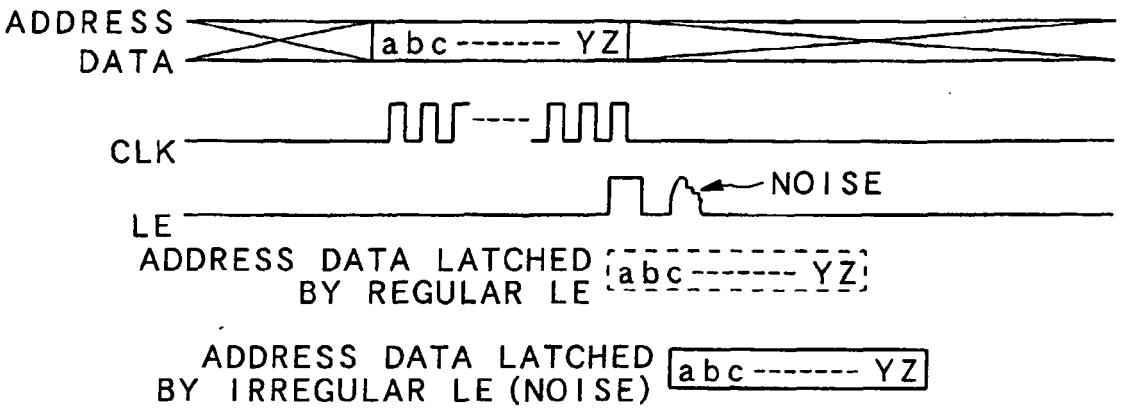

ADDRESS DATA
abc------- YZ
CLK
NOISE
LE
ADDRESS DATA LATCHED BY REGULAR LE
abc------- YZ
ADDRESS DATA LATCHED BY IRREGULAR LE (NOISE)
abc------- YZ

FIG. 7

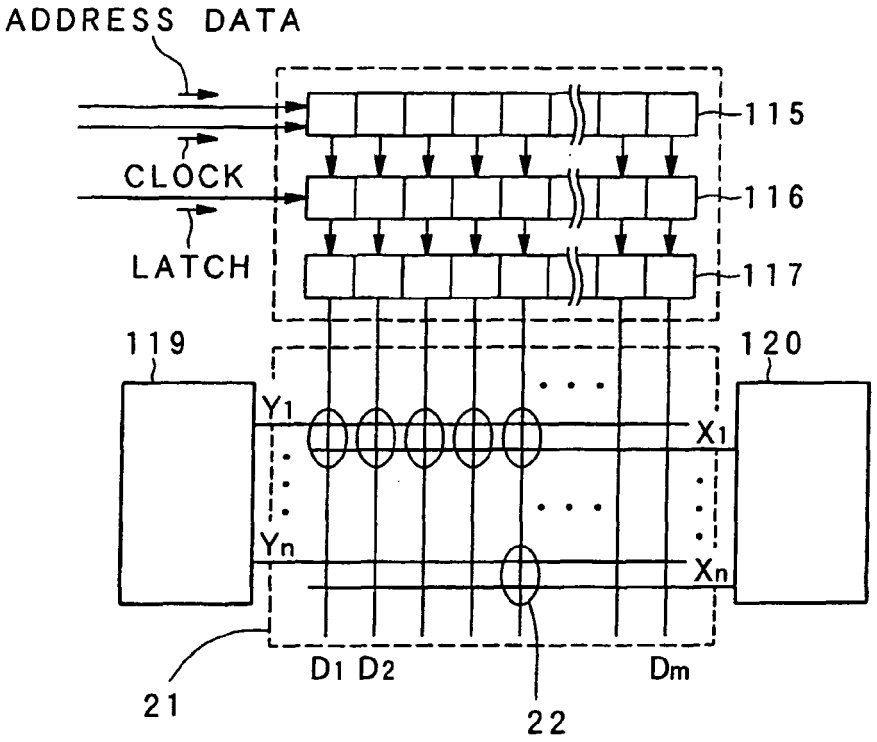

ADDRESS DATA
CLOCK
LATCH
115
116
117
119
120
Y1
Yn
X1
Xn
D1 D2
Dm
21
22

FIG. 8

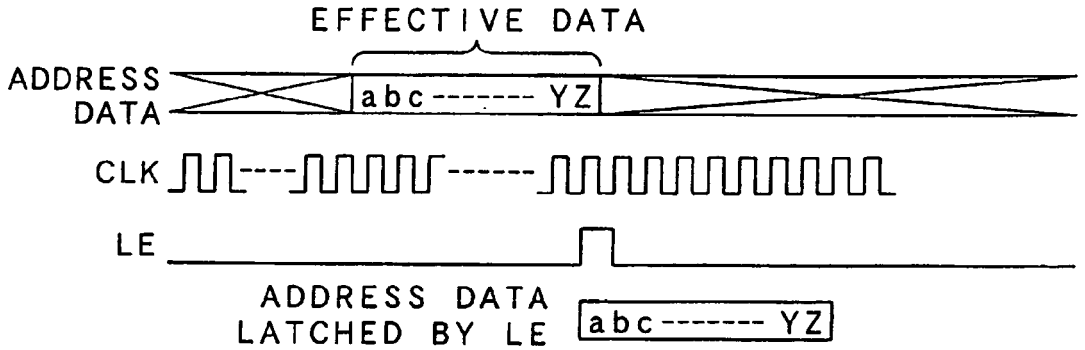
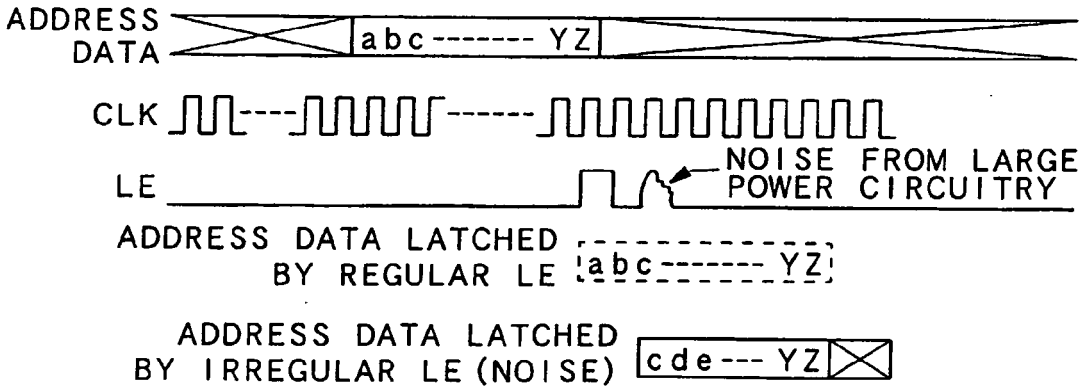

EFFECTIVE DATA
ADDRESS DATA
abc------- YZ
CLK
LE
ADDRESS DATA LATCHED BY LE
abc------- YZ

FIG. 9


ADDRESS DATA
abc------- YZ
CLK
LE
NOISE FROM LARGE POWER CIRCUITRY
ADDRESS DATA LATCHED BY REGULAR LE
abc------- YZ
ADDRESS DATA LATCHED BY IRREGULAR LE (NOISE)
cde--- YZ

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 6191768 B1 **[0005]**