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(54) **Solid state memory**

(57) A level (412) of a solid state memory device (410) includes main memory (10) and address logic (12, 14). The address logic (12, 14) includes first and second groups of address elements (26a, 26b). Current-carrying capability of the first group of address elements (26b) is greater than current-carrying capability of the

second group of address elements (26a). Current flowing through the address elements (26a, 26b) during programming causes the resistance states of only the second group of address elements (26a) to change.

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Description

[0001] The present invention relates to information storage devices and in particular to programmable address logic for solid state diode-based memory devices. More specifically, the present invention relates to one-time programmable (OTP) solid state memory.

[0002] Portable devices such as PDAs, handheld computers, digital cameras and digital music players include memory for storing data, digital images and MP3 files. Different types of memory are available for these portable devices. Conventional memory types include flash memory, mini-hard drives, mini-compact discs, and magnetic tape. However, each of these memory types has one or more of the following limitations: large physical size, low storage capacity, relatively high cost, poor robustness, slow access time and high power consumption.

[0003] A solid state diode-based OTP memory is disclosed in European patent application 02253896.1. Compared to the conventional memory, the diode-based memory has a high shock tolerance, low power consumption, fast access time, moderate transfer rate and good storage capacity. The diode-based memory can fit into a standard portable interface (e.g., PCMCIA, CF) of a portable device.

[0004] Address logic of the diode-based memory device is formed on the same level as main memory. In a multi-level diode-based memory device, each level has main memory and address logic (unlike conventional solid state memory such as DRAM). Moreover, the address logic of the diode-based memory device is programmable. The address logic may be programmed after each layer has been fabricated. Since no masking is required, physical processing is simplified.

[0005] According to one aspect of the present invention, a solid state memory device includes a decoder having first and second groups of address elements, the address elements of the first group having been assigned a first logic value and the address elements of the second group having been assigned a second logic value. Current-carrying capability of the first group of address elements is greater than current-carrying capability of the second group of address elements. Current flowing through the address elements during programming causes the resistance states of only the second group of address elements to change.

[0006] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

[0007] Figure 1 is a block diagram of a level of a solid state memory device.

[0008] Figures 2a-2c are illustrations of different types of programmable elements in the level.

[0009] Figure 3 is another illustration of a programmable element.

[0010] Figure 4 is an illustration of a method of changing the resistance states of address elements.

[0011] Figures 5a-5c are illustrations of different layouts for selected and unselected address elements of a decoder.

[0012] Figures 6a and 6b are illustrations of a level of a solid state memory device that allows for defect management.

[0013] Figure 7 is an illustration of a method of avoiding defects in a multi-level solid state memory device.

[0014] Figure 8 is an illustration of a multi-level solid state memory device.

[0015] Reference is made to Figure 1, which shows a level 8 of a solid state memory device. The level 8 includes main memory 10 and programmable address logic 12, 14. The main memory 10 includes a cross point resistive array of OTP memory elements 16, traces functioning as word lines 18 extending along rows of the memory elements 16, and traces functioning as bit lines 20 extending along columns of the memory elements 16. There may be one word line 18 for each row of the memory elements 16 and one bit line 20 for each column of memory elements 16. Each memory element 16 is located at a cross point of a word line 18 and a bit line 20. Only a relatively small number of memory elements 16 is shown to simplify the illustration of the level 8. In practice, arrays of any size may be used.

[0016] The address logic 12, 14 uses combinational diode logic for addressing the memory elements 16 during read and write operations. The address logic 12, 14 includes an OTP row decoder 12 for selecting the word lines 18. The row decoder 12 selects the word lines 18 by decoding addresses supplied on row address lines 22 (the addresses may be supplied by external row address drivers 24). The row decoder 12 includes a plurality of OTP address elements 26. Each address element 26 of the row decoder 12 is at a cross point of a word line 18 and a row address line 22.

[0017] The address logic 12, 14 also includes an OTP column decoder 14 for selecting the bit lines 20. The column decoder 14 selects the bit lines 20 by decoding addresses supplied on column address lines 28 (the addresses may be supplied by external column address drivers 30). The column decoder 14 also includes a plurality of OTP address elements 26. Each address element 26 of the column decoder 14 is at the cross point of a bit line 20 and a column address line 28.

[0018] One end of each word line 18 terminates at row sense logic 34. The row sense logic 34 includes multiple sense resistors 36, each sense resistor 36 connected between a row power line 38 and an end of a word line 18. A row sense line 40 crosses the word lines 18. The row sense logic 34 also includes multiple sense elements 42, each sense element 42 connected between the row sense line 40 and a word line 18.

[0019] One end of each bit line 20 terminates at column sense logic 44. The column sense logic 44 includes multiple sense resistors 36, each sense resistor 36 con-

nected between a column power line 46 and an end of a bit line 20. A column sense line 48 crosses the bit lines 20. The column sense logic 44 also includes multiple sense elements 42, each sense element 42 connected between the column sense line 48 and a bit line 20.

[0020] A row programming line 50, between the main memory 10 and the row decoder 12, crosses the word lines 18. Programming elements 52 are connected between the row programming line 50 and the word lines 18.

[0021] A column programming line 54, between the main memory 10 and the column decoder 14, crosses the bit lines 20. Programming elements 52 are connected between the column programming line 54 and the bit lines 20.

[0022] The memory elements 16, the address elements 26, the sense elements 42 and the programming elements 52 may all be diode based. This simplifies the fabrication of the level 8.

[0023] Different types of programmable elements 16/26/42/52 are shown in Figures 2a-2c. The programmable element of Figure 2a includes a fuse 110 coupled in series with a diode 112. Prior to programming, the resistance state of such an element is low, with the fuse 110 intact. During programming, the resistance state of the element can be changed from low to high by "blowing" the fuse 110.

[0024] The programmable element of Figure 2b includes a resistor 120 coupled in series with a diode 122. Prior to programming, the resistance state of such an element is low, with the resistor 120 intact. During programming, the resistance state of the element can be changed from low to high by "blowing" the resistor 120.

[0025] The programmable element of Figure 2c includes only a diode 132. Prior to programming, the diode 132 is intact, whereby its resistance state is low. During programming, the diode 132 can be opened to change its resistance state from low to high. Such a diode 132 functions as a fuse. In the alternative, the diode 132 can function as an anti-fuse, going from a high resistance state to a low resistance state during programming.

[0026] The programmable elements 16/26/42/52 are not limited to the types shown in Figures 2a-2c. For example, the programmable elements 16/26/42/52 could include transistors instead of diodes.

[0027] Returning now to Figure 1, the level 8 may be fabricated as follows. Column lines 20 are formed on a substrate, a multi-layer film of silicon is formed on the column lines 20, and word lines 18 are formed on the film. Each programmable element 16/26/42/52 may be formed as that portion of the film (F) between two crossing traces (T) (see Figure 3). The size of the programmable element 16/26/42/52 is determined by the overlapping area between crossing traces and the thickness of the film. For example, a diode in main memory 10 is formed as that portion of the film between crossing word and bit lines 18 and 20.

[0028] The different layers of the film have appropri-

ate dopings (and/or a combination of crystalline and amorphous silicon) to form the diodes 112, 122, 132. Additional layers with appropriate dopings can be added to form resistors 120, fuses 110, or anti-fuses. The sense resistors 36 may be formed by modifying the ends of the word and bit lines 18 and 20. The row and column address drivers 24 and 30 may be formed on the substrate.

[0029] The row and column decoders 12 and 14 may be programmed during device fabrication, after the level 8 has been fabricated. The decoders 12 and 14 are programmed by changing the resistance states of selected address elements from a low resistance state to a high resistance state (or vice versa). Details of the combinational logic for addressing the main memory (that is, the details about which address elements are selected) are disclosed in European patent application 02253896.1. Various ways of programming the decoders 12 and 14 will be described below,

[0030] Data may be written to the main memory 10 by supplying row and column addresses to the row and column decoders 12 and 14. A write current flows through a selected word line 18 and a selected bit line 20 and, therefore, flows through the memory element 16 at the cross point of the selected word and bit lines 18 and 20. Magnitude of the write current is sufficient to change the resistance state of the selected element (e.g., by opening the fuse 110 of Figure 2a, opening the resistor 120 of Figure 2b, opening the diode 132 of Figure 2c, shorting the anti-fuse).

[0031] The resistance state of a memory element 16 may be sensed by supplying row and column addresses to the row and column decoders 12 and 14. A voltage is applied to the second row sense line 40 and a voltage of opposite polarity is applied to the second column sense line 48. A sense current flows through a selected word line 18 and a selected bit line 20 and, therefore, flows through the memory element 16 at the cross point of the selected word and bit lines 18 and 20. Magnitude of the sense current indicates the resistance state of the selected memory element 16.

[0032] Each address element 26 has a link that may be broken during programming. For example, the fuse 110 is the link for the address element shown in Figure 2a, the resistor 120 for the address element of Figure 2b, and the diode 132 for the address element of Figure 2c. Each link is made of a photosensitive material typically used for solar cells and displays. For example, the links may be made of amorphous silicon with a P-doped layer. The conductivity of intrinsic amorphous silicon is typically 10^6 times lower than the doped amorphous silicon. However, when irradiated with light, the conductivity of the intrinsic region increases to a level similar to that of the doped region. By irradiating an address element 26, density of current flowing through the address element 26 is increased to the point that the link blows.

[0033] Reference is now made to Figure 4, which illustrates a method of changing the resistance state of

"selected" address elements 26. Address elements that are selected are indicated by X's. These selected elements will have their resistance states changed during programming. Unselected address elements are indicated by O's. These unselected address elements will not have their resistance states changed during programming.

[0034] During programming of the row decoder 12, a voltage (-V) is applied across the row programming line 50, and a voltage of opposite polarity (+V) is applied to the row sense line 40. (During programming of the column decoder 14, a voltage is applied across the column programming line 54, and a voltage of opposite polarity is applied to the column sense line 48.) This will effectively apply a voltage across two diodes connected back-to-back. The voltage is applied in such a manner that the diodes in the programming elements 52 are forward biased and the diodes in the address elements 26 are reverse biased. The voltages can be applied by the row and column address drivers 24 and 30.

[0035] Electromagnetic radiation (EM) is applied to the selected address elements 26. The electromagnetic radiation is of sufficient intensity to significantly increase the conductivity of the selected address elements. Consequently, the density of the current flowing through the selected address elements is increased. This increase in current density causes the links of the selected address elements to open. The links of the unselected address elements remain unbroken.

[0036] The programming elements 52 may have a higher current-carrying capability than the selected address elements 26.

[0037] This optical programming of the address diodes 26 may be performed by using a jig including addressable laser diodes. The laser diodes irradiate only the selected address elements 26. Lenses and other optical elements may be used to focus the EM radiation on the selected address elements 26. All selected elements 26 may be irradiated simultaneously, whereby the resistance states of all selected address elements 26 are changed at the same time.

[0038] In the alternative, the unselected address elements could be masked from the irradiation, and blanket irradiation could be applied to the layer. Resistance states of the masked address elements would not be changed.

[0039] For EM radiation to be applied to selected address elements 26, the traces may be made transparent to the EM radiation. Materials for these transparent traces may be of the type used in liquid crystal displays. As an alternative to making transparent traces, the EM radiation may be guided to the selected address elements 26.

[0040] An alternative approach to changing the resistance states of the selected address elements 26 will now be described. The unselected address elements in each decoder 12 and 14 are formed with a greater current-carrying capability than the selected address ele-

ments 26. During programming of the decoders 12 and 14, all address elements are reversed-biased and the sense elements are forward-biased in the manner described above. Consequently, a current flows through the selected and unselected address elements. This current causes the links of the selected address elements 26 to break, but the current does not cause the links of the unselected selected address elements to break.

[0041] The links may be broken without applying EM radiation to the selected address elements 26. Therefore, the links may be made of a material that is not photoconductive. However, reliability in breaking the links may be increased by making the links from a photoconductive material and irradiating the selected address elements 26 during programming.

[0042] The memory elements 16 and the selected address elements 26 may be made at the minimum resolution, thus allowing the optimal storage capacity. The unselected address elements may be made with larger dimensions by increasing the size of the address lines above the minimum resolution and increasing those portions of the memory lines (i.e., word and bit lines) that cross the address lines.

[0043] Figures 5a-5c show different layouts for selected address elements 26a and enlarged, unselected address elements 26b. If an address protocol can guarantee that no column has adjacent enlarged (unselected) address elements 26b, then the address logic may have the configuration shown in Figure 5a. Figure 5a shows a row decoder 12 in which columns do not contain any adjacent enlarged (unselected) address elements 26b. Although not shown as such, the address elements 26a and 26b may be formed at full contact pitch.

[0044] If the address protocol cannot provide such a guarantee, whereby the address logic could include adjacent enlarged address elements in a column, the distance between word lines 18 may be increased. However, this would reduce the data storage density of the main memory.

[0045] Instead, the row decoder 12 may be divided into two spaced-apart sets 12a and 12b, as shown in Figure 5b. Odd-numbered word lines 18a are interdigitated with even-numbered word lines 18b. A first set of address lines 22a crosses the odd-numbered word lines 18a, and a second set of address lines 22b crosses the even-numbered word lines 18b. The first and second sets of address lines 22a and 22b receive the same address signal.

[0046] This approach allows the size of adjacent memory elements 26b to be increased threefold, yet it still allows the selected memory elements 26a to be fabricated at minimum resolution. If an address protocol can guarantee that no column has adjacent enlarged (unselected) address elements 26b, the size of the non-adjacent enlarged memory elements 26b can be increased fivefold (see Figure 5c).

[0047] Figures 5a-5c were just described in connec-

tion with the row decoder 12. However, the same principles can be applied to the column decoder 14.

[0048] Reference is now made to Figure 6a, which shows portions of a level 208 of a memory device that allows for defect management. The level 208 includes main memory 210, a row decoder 212, and row sense logic 234. The row sense logic 234 includes sense resistors 236. The level 208 further includes word lines 218, bit lines 220, row address lines 222, a power supply line 238, a row sense line 240, and a row programming line 242. Elements for addressing, sensing and programming on the column side are not shown. Selected address elements are indicated by X's and unselected address elements are indicated by O's.

[0049] A defective area in the level 8 is identified by the letter D. For instance, the defective area D might be caused by a short of two adjacent word lines 218. The defective area D renders the two associated rows unusable.

[0050] The row decoder 212 can be programmed to avoid the defective area D. The word lines 218 corresponding to the defective area D are disconnected from main memory 210. For example, breaks (discontinuities) may be formed in these word lines 218. In the alternative, the sense resistors 236 of these word lines 218 may be opened. If the sense resistors 236 are made from a photoconductive material such as amorphous silicon, they can be opened or "blown" by causing a current to flow through the resistors (e.g., by biasing the address and write lines with respect to the drive voltage) and then applying EM radiation. Applying the EM radiation increases the conductivity. The increase in current causes the irradiated sense resistor to be blown

[0051] The disconnected word lines are replaced by spare word lines. Certain word lines and their connected memory, address and sense elements are reserved as spares. Figure 6a shows that the last few word lines of the level 208 are reserved as spares (as indicated by the block 211). However, the location of the spares are not so limited; the spare word lines may be at any location in the level 208. Initially, all address elements connected to the spares are unselected

[0052] The spare word lines have additional logic 252. Each address line 254 is connected to a corresponding spare word line by a spare address element 256. The encoding may be performed by optically programming the selected spare address elements 256.

[0053] Figure 6b shows the decoder 212 re-mapped to avoid the defective area D. The two word lines 218a and 218b associated with the defective area D are disconnected by opening their sense resistors 236.

[0054] Two spare lines 218c and 218d replace the two lines 218a and 218b that were disconnected. The address elements 256 connected to these two replacement spare lines 218c and 218d have been programmed to match the resistance states of selected and unselected address elements for the two disconnected lines 218a and 218b. Thus, these two replacement

spare lines 218c and 218d now have the same addresses as the disconnected word lines 218a and 218b. The spare address elements connected to these two replacement spare lines 218c and 218d are changed to a high resistance state and, thus, effectively removed from the row decoder 212.

[0055] The unused spare line 218e is disconnected by opening its sense resistor 236.

[0056] Reference is now made to Figure 7, which illustrates a method of fabricating a multi-level solid state memory device. After a first level of the device is formed (block 302), defects in the first level are identified (block 304). Such defects include, but are not limited to, discontinuities or defects in one or both cross point wires, and shorts between data lines. The defects may be identified by measuring I-V characteristics of each cross point in main memory.

[0057] After the defects have been identified, the decoders are programmed to avoid a significant number of the defects (block 306). The programming reduces the defect level to zero or an acceptable level for error correction (that is, a level that does not stress or overload error correction).

[0058] Subsequent levels are formed (block 308). Each time a level is formed (block 302), defects in the level are identified (block 304), and the decoders on that level are programmed to avoid the defects (block 306).

[0059] After the levels have been formed, the memory device is completed (block 310). As part of completing the memory device, address lines are connected, interface circuitry is added and the levels are packaged.

[0060] Details of the design and fabrication of the main memory, addressing of multiple levels, packaging of multiple layers into a single chip, reading and writing to main memory, etc. are disclosed in assignee's U.S. Serial No. 09/875,356.

[0061] This method allows defect management to be implemented on individual levels and therefore avoids the problem of a defective area in one level eliminating the use of the same memory area of another level. It also implements defect management in a manner that physically re-positions the defective address location and therefore does not require a defect list for re-mapping. This simplifies use of the memory system.

[0062] Reference is now made to Figure 8, which shows a multi-level solid state memory device 410. Multiple levels 412 are stacked on top of one another. Unlike conventional semiconductor memory, decoders are formed in each layer 412. Each layer 410 is connected to control/interface circuitry 414 by a memory system interface 416. The control/interface circuitry 414 is formed in the substrate. The control/interface circuitry 414 performs error code correction (ECC) and defect management functions, as well as functions for operating the device 410. These functions include setting write voltages, setting write enable lines and controlling power sense striping, addressing the memory by converting logical addresses to address line patterns required to

access physical memory locations, and data read processing of sense line outputs.

[0063] The device 410 is not limited to control/interface circuitry that is shared by the layers. Instead each level 412 may have its own control/interface circuitry. 5

[0064] The main memory could be programmed at the factory, in the same manner and at the same time as the address logic. The main memory might be pre-programmed with microcode, map data, etc.

[0065] The present invention is not limited to the specific embodiments described and illustrated above. Instead, the present invention is construed according to the claims that follow. 10

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Claims

1. A solid state memory device comprising a decoder (12) having first and second groups of address elements (26b, 26a), the address elements (26b) of the first group having been assigned a first logic value and the address elements (26b) of the second group having been assigned a second logic value; current-carrying capability of the first group of address elements (26b) being greater than current-carrying capability of the second group of address elements (26a). 20 25
2. The device of claim 1, wherein the address elements (26a, 26b) include diodes. 30
3. The device of claim 1, further comprising programming logic (50, 52) and sense logic (34), the programming logic (52) including a programming line (50) and programming elements (52), the sense logic including a sense line (40). 35
4. The device of claim 3, wherein the programming elements (52) have same current-carrying capability as the first group of address elements (26b). 40
5. The device of claim 1, wherein the address elements (26a, 26b) are made of photoconductive material. 45
6. The device of claim 1, wherein elements (26b) of the first group are physically larger than elements (26a) of the second group.
7. The device of claim 6, wherein the address elements (26a, 26b) of the decoder (12) are separated into spaced-apart two sets (12a, 12b), each set (12a, 12b) including address elements (26a, 26b) from the first and second groups. 50 55
8. The device of claim 7, wherein the elements (26b) of the first group are about three times larger than the elements (26a) of the second group.

9. The device of claim 1, further comprising main memory (10); wherein the elements of the second group (26a) have the same current-carrying capability as memory elements (16) of the main memory (10).

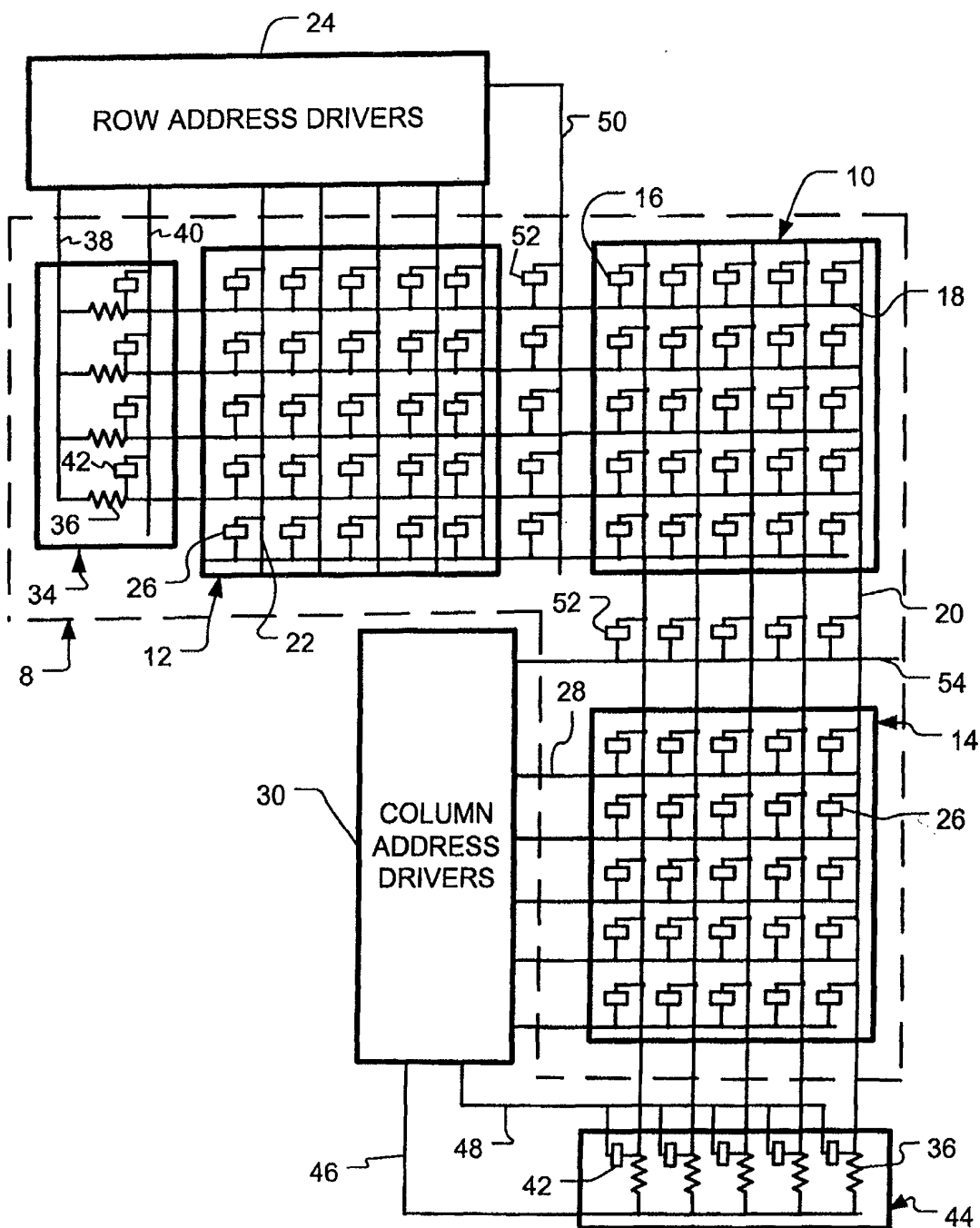
FIG. 1

FIG. 2a

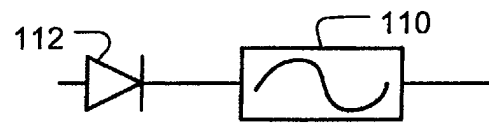


FIG. 2b

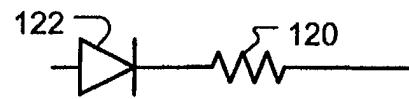


FIG. 2c

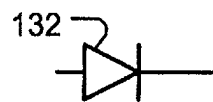
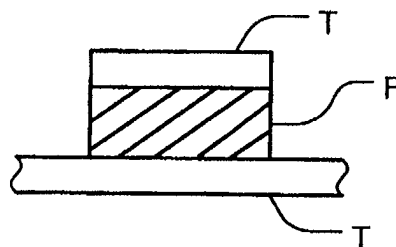


FIG. 3



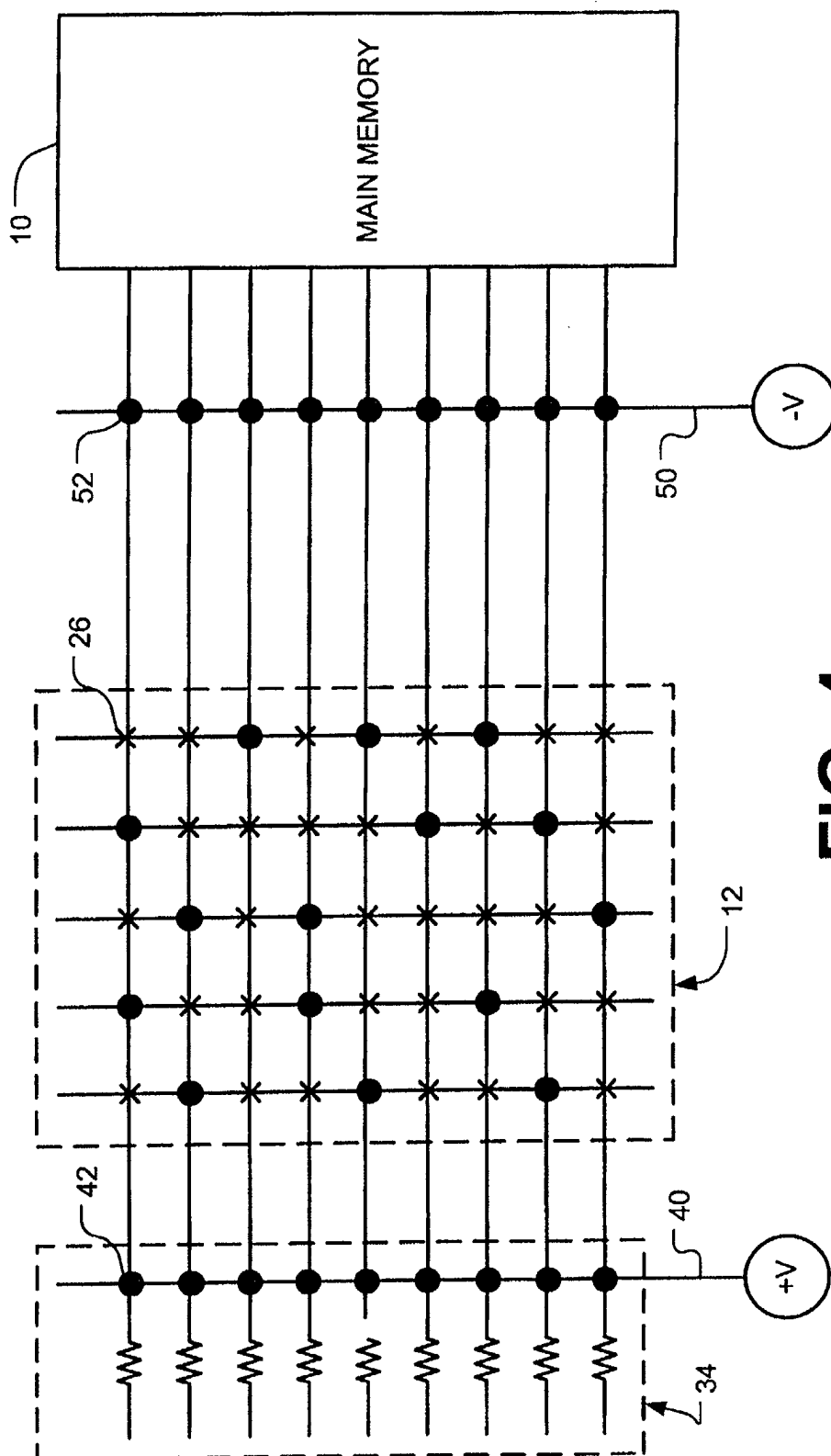


FIG. 4

FIG. 5a

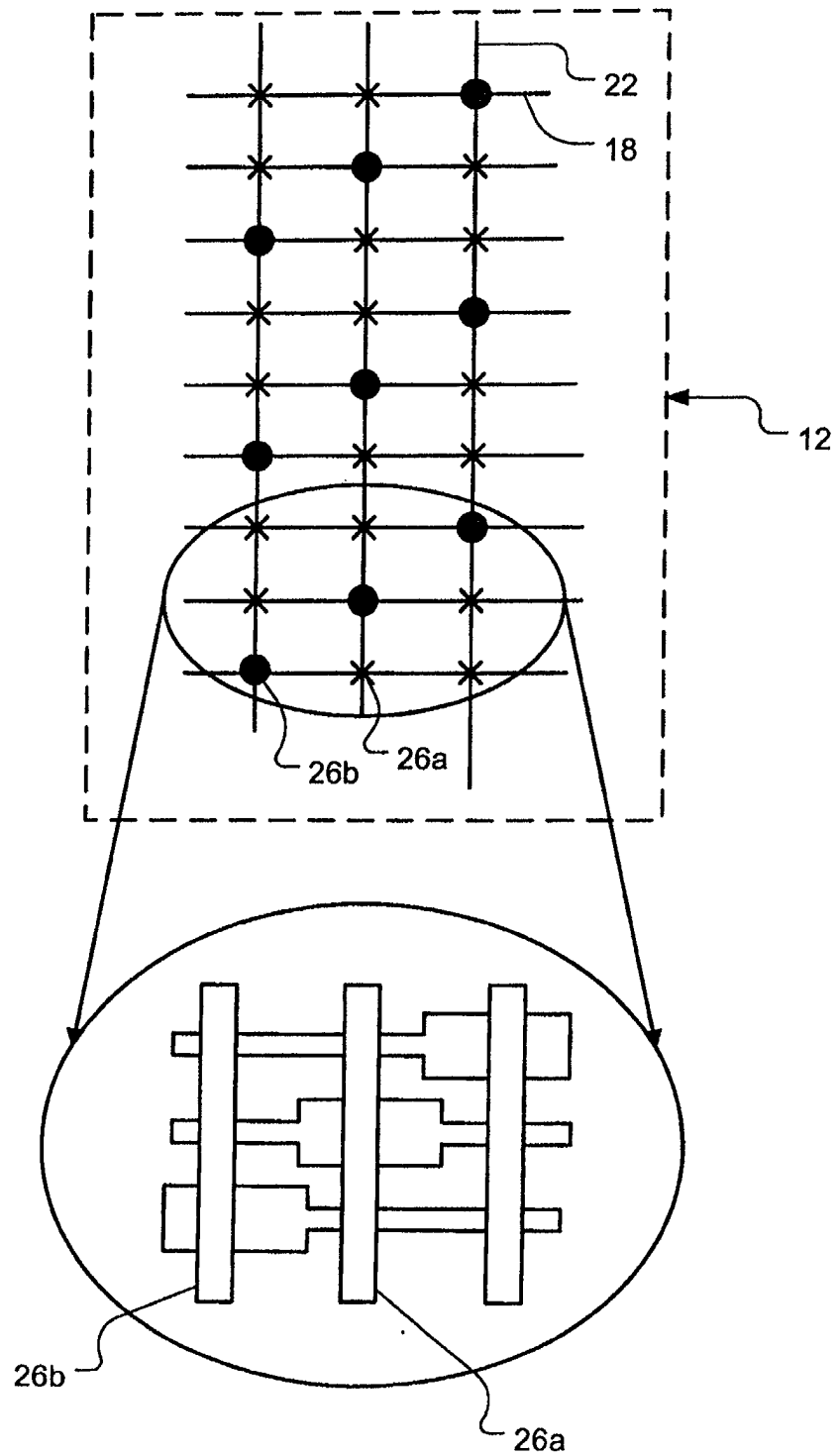


FIG. 5b

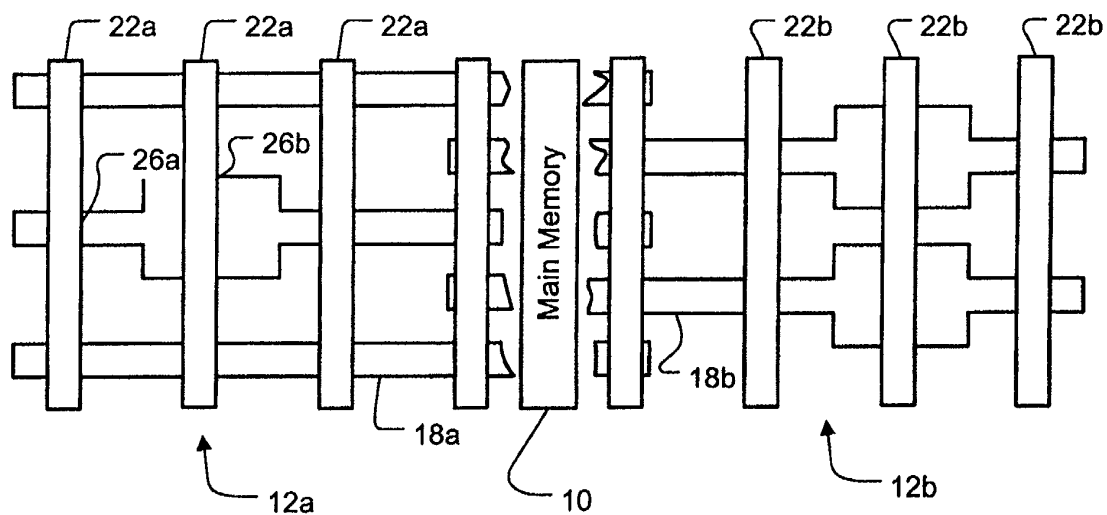
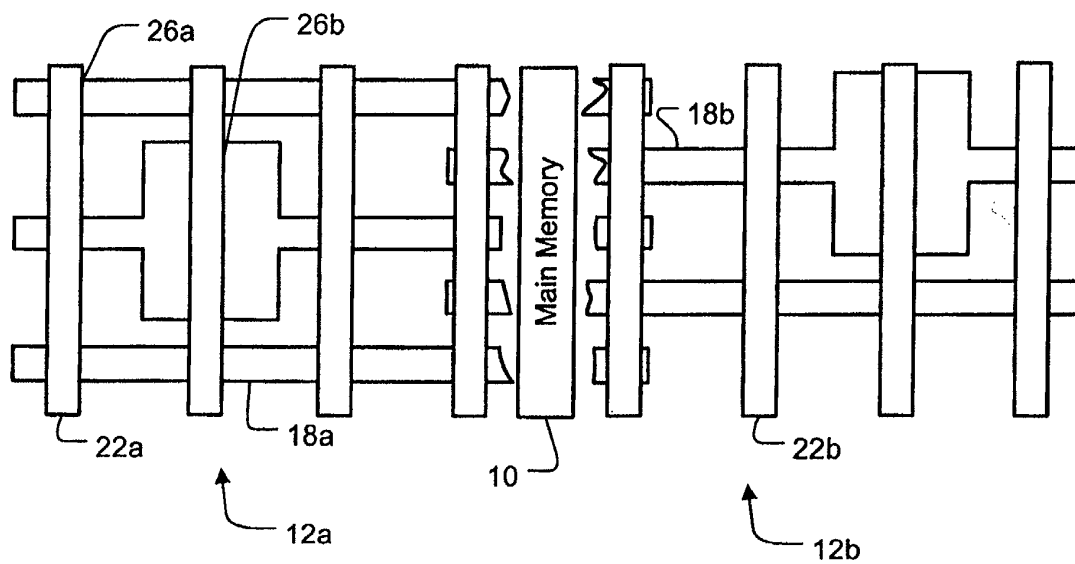


FIG. 5c



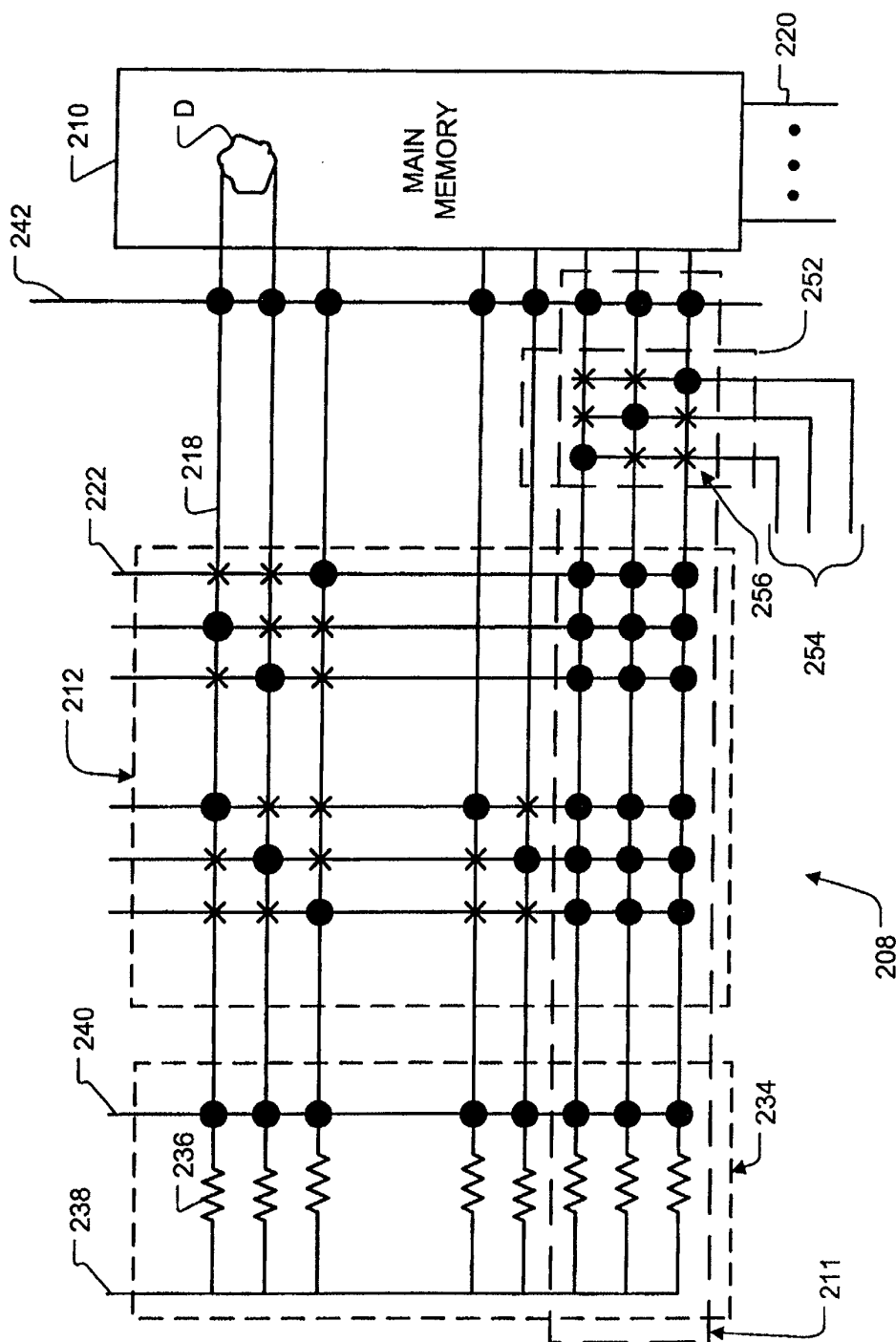


FIG. 6a

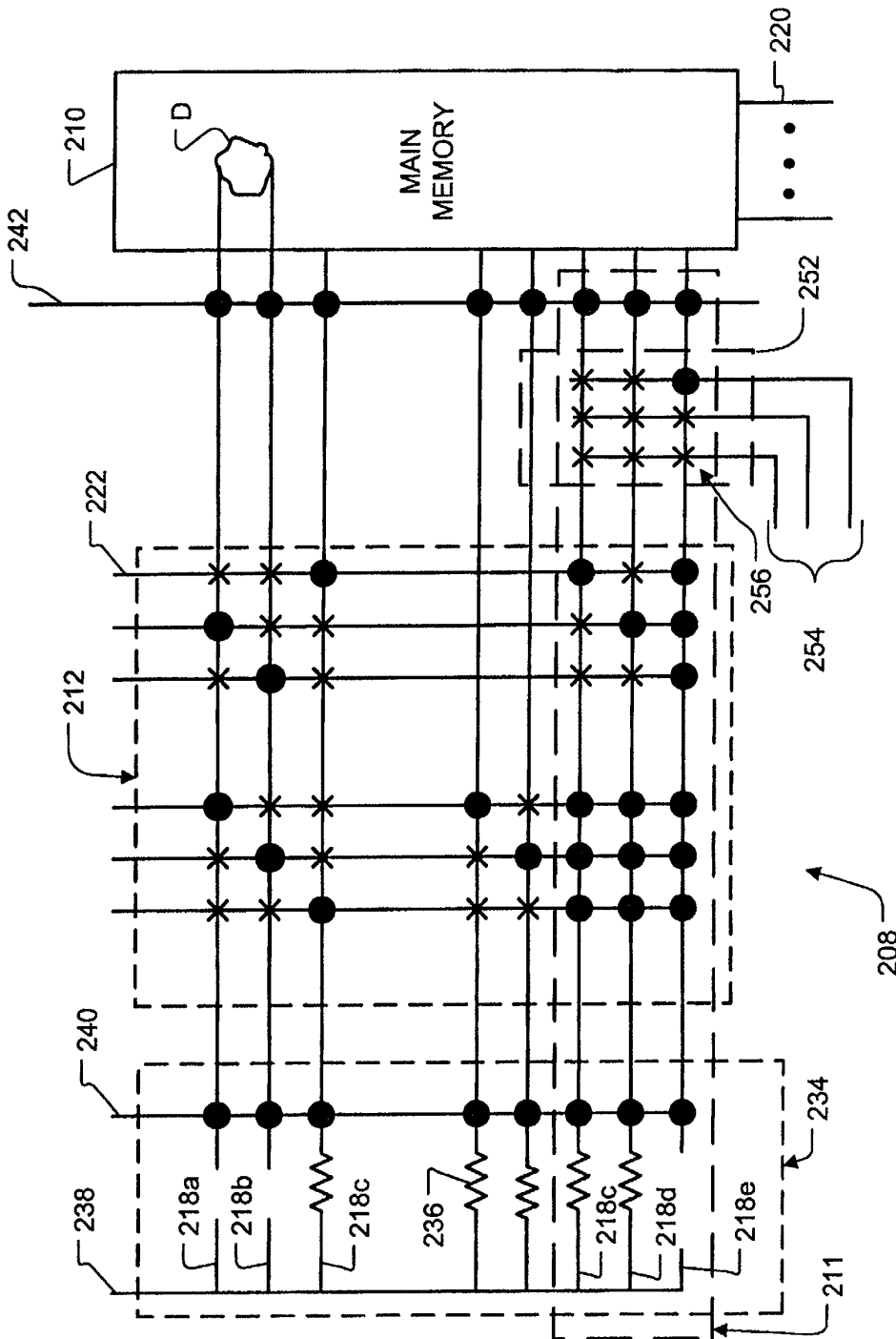


FIG. 6b

FIG. 7

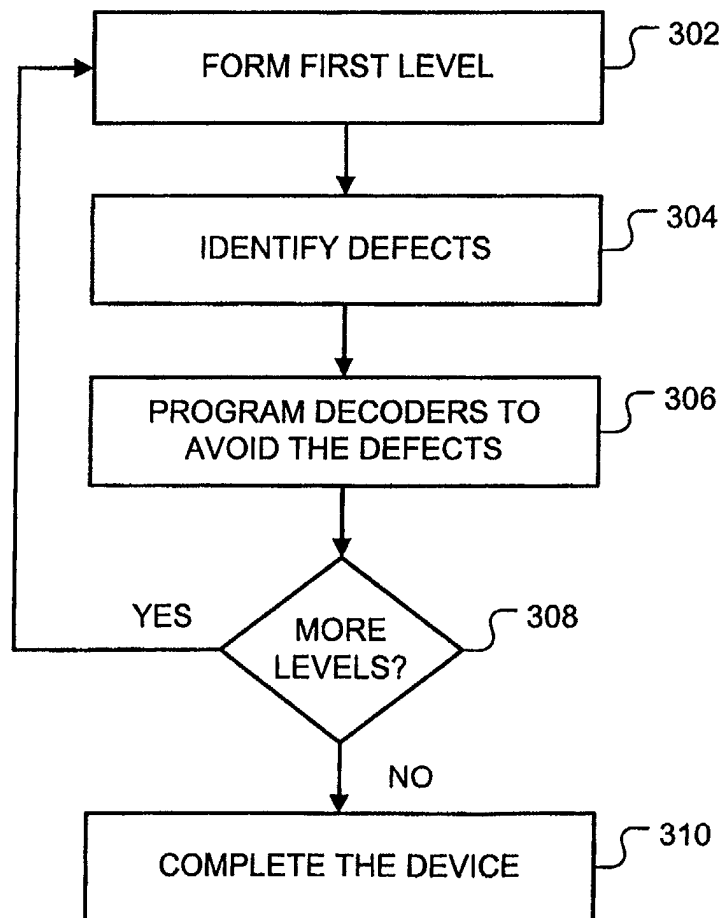


FIG. 8

