



(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
30.03.2005 Bulletin 2005/13

(51) Int Cl.7: G11C 11/56

(43) Date of publication A2:
12.03.2003 Bulletin 2003/11

(21) Application number: 02256128.6

(22) Date of filing: 04.09.2002

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
IE IT LI LU MC NL PT SE SK TR
Designated Extension States:
AL LT LV MK RO SI

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(30) Priority: 06.09.2001 US 947671

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(54) Output sense amplifier for a multibit memory cell

(57) A read circuit for a multibit memory cell is provided to convert a multi-level voltage output from the multibit memory cell into the desired number of binary levels. For example, if the multibit memory cell can be

programmed to have four resistance levels, which produce four output voltages respectively, the read circuit is provided with two binary outputs. For additional resistance levels, and corresponding voltage levels, additional binary outputs may be provided.

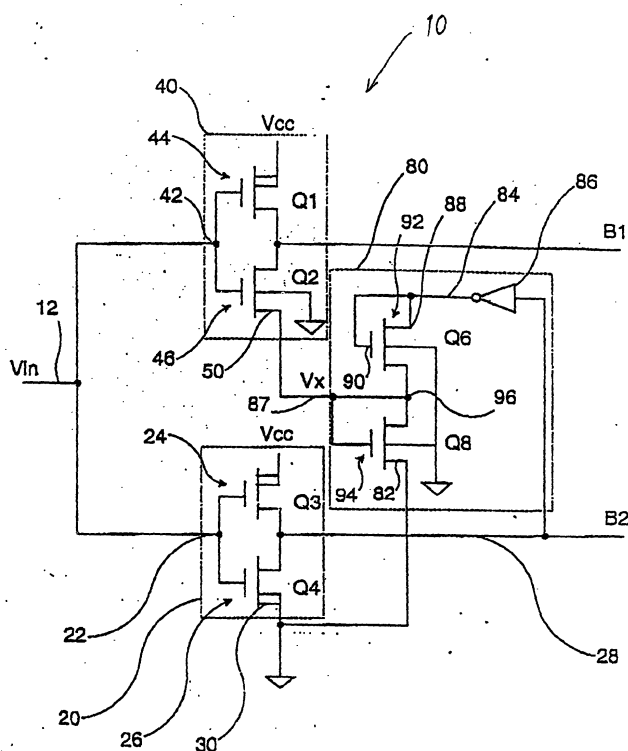


Fig. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 02 25 6128

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A	* page 11, line 21 - page 17, last paragraph * * figures 5,8 *	1,8	
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A	OHKAWA M ET AL: "A 98 MM2 DIE SIZE 3.3-V 64-MB FLASH MEMORY WITH FN-NOR TYPE FOUR-LEVEL CELL" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 31, no. 11, 1 November 1996 (1996-11-01), pages 1584-1589, XP000691442 ISSN: 0018-9200 * page 1586, left-hand column, paragraph IV - right-hand column, paragraph V * * figures 6,7 *	1,8,11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G11C
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 4 February 2005	Examiner Colling, P
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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EPO FORM 1503 03.82 (P04C01)



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EUROPEAN SEARCH REPORT

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