(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 296 542 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
26.03.2003 Bulletin 2003/13

(51) Int Cl.[7]: **H05B 41/282**, H05B 41/285, H05B 41/392, H01L 41/04

(21) Application number: **02256562.6**

(22) Date of filing: **20.09.2002**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **21.09.2001 JP 2001288748**
18.09.2002 JP 2002271547

(71) Applicant: **Minebea Co., Ltd.**
Kitasaku-gun, Nagano-ken (JP)

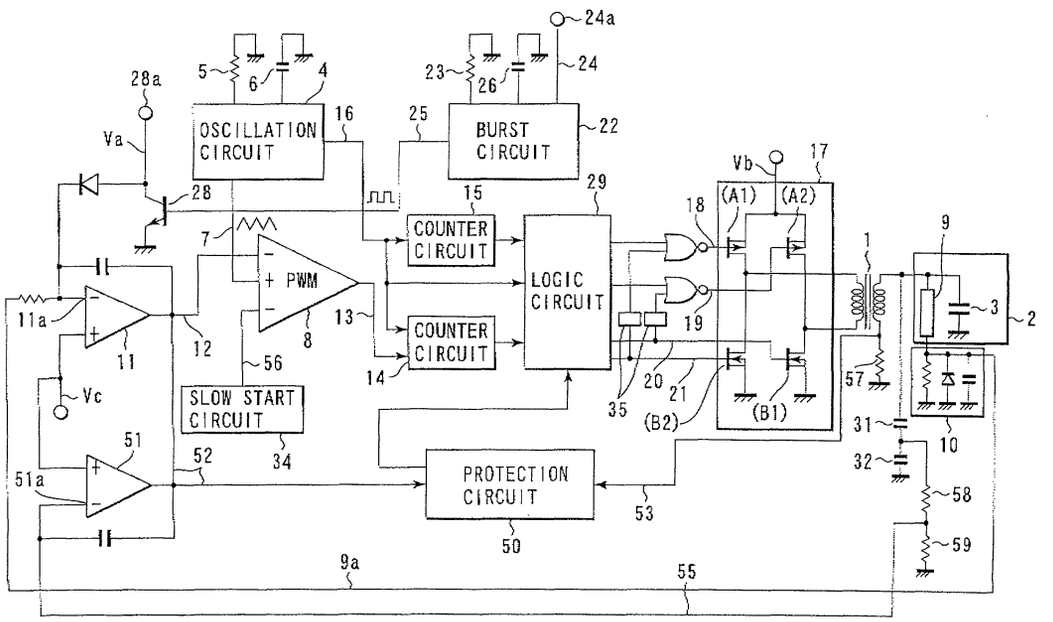
(72) Inventors:
- **Suzuki, Sinichi, c/o Minebea Co., Ltd.**
Asaba-cho, Iwata-gun, Shizuoka-ken (JP)
- **Kamiya, Yasuhiro, c/o Minebea Co., Ltd.**
Asaba-cho, Iwata-gun, Shizuoka-ken (JP)
- **Kawamoto, Koji**
Tokyo (JP)
- **Ushijima, Masakazu**
Tokyo (JP)

(74) Representative: **McCallum, Graeme David et al**
Lloyd Wise, McNeight & Lawrence,
Regent House,
Heaton Lane
Stockport, Cheshire SK4 1BS (GB)

(54) Inverter circuit for a discharge tube

(57) An inverter circuit for a discharge tube of the present invention comprises a transformer in which a resonance circuit is composed of a parasitic capacitance of a discharge tube, and a H-bridge circuit which drives the primary side of the transformer at a frequency that is lower than the resonance frequency of the resonance circuit and that involves a phase difference between the voltage and the current at the primary side of the transformer, the phase difference falling within a predetermined range from its minimum point.

FIG. 6



EP 1 296 542 A1

Description

[0001] The present invention relates generally to an inverter circuit for a discharge tube for use in an LCD unit, and, more specifically, to an inverter circuit for a discharge tube, which ensures high power efficiency.

[0002] Some conventional inverter circuits for a discharge tube operate such that the primary side of a transformer is driven by a resonance frequency of a resonance circuit at the secondary side of the transformer, which comprises a leakage inductance and a parasitic capacitance of a discharge tube connected as a load. Such an inverter circuit is disclosed in US Patent No. 6,114,814.

[0003] This drive by the resonance frequency involves a phase difference between voltage and current at the primary side of the transformer, so that power efficiency of the transformer is not necessarily satisfactory.

[0004] There is another problem that high-order resonance frequencies existing at the secondary side of the transformer cause an accidental operation that influences undesirably its operation, which gives difficulty in designing the transformer.

[0005] The present invention has been made in view of the above problems. It is therefore an object of the present invention to provide an inverter circuit for a discharge tube that has an increased efficiency of a transformer and that is free from the influence of the high-order resonance frequencies.

[0006] In order to achieve the above object, it is noted that an excellent power efficiency can be obtained when the transformer is driven at a specific frequency range where the phase difference is small between voltage and current at the primary side of the transformer.

[0007] According to a first aspect of the present invention, an inverter circuit for a discharge tube comprises: a transformer which includes a resonance circuit composed of a parasitic capacitance of the discharge tube; and a H-bridge circuit which drives a primary side of the transformer at a frequency that is lower than a resonance frequency of the resonance circuit and that involves a phase difference between a voltage and a current at the primary aide of the transformer, the phase difference falling within a predetermined range from its minimum point. Accordingly, the inverter circuit improves the power efficiency of the transformer, and suffers from little influence by the high-order frequencies, easing the transformer design.

[0008] According to a second aspect of the present invention, the predetermined range is preferably below the resonance frequency at the secondary side of the transformer and covers -30° from the minimum point. Accordingly, the inverter circuit improves reliably the power efficiency of the transformer.

[0009] According to a third aspect of the present invention, the inverter circuit for a discharge tube may further comprise a burst circuit that outputs a predetermined burst signal, whereby the primary side of the transformer is driven intermittently. Accordingly, light is modulated easily over a wide range.

[0010] According to a fourth aspect of the present invention, the burst circuit outputs an inputted pulsed signal as a burst signal when a resistance that determines an oscillating frequency is set to be higher than a predetermined value, and outputs a burst signal obtained from a predetermined DC signal and an oscillated triangular wave when the resistance is set to be lower than a predetermined value. Accordingly, the inverter circuit outputs easily a plurality of burst signals.

[0011] According to a fifth aspect of the present invention, when the burst signal goes high, an inverting input terminal of an error amplifier which feedback-controls a current of the discharge tube is pulled up, whereby the primary side of the transformer is inactivated. Accordingly, light is modulated easily and reliably over a wide range.

[0012] According to a sixth aspect of the present invention, the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, and a delay circuit is connected to gate circuits of the PMOSs. Accordingly, the PMOSs and NMOSs in the series circuits are prevented from turning on simultaneously, thereby preventing malfunction and protecting circuits

[0013] According to a seventh aspect of the present invention, the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, and gates of two PMOSs are caused to rise at respective two points which correspond to the maximum peaks of a predetermined triangular wave output and which appear alternately with each other while gates of two NMOSs are caused to rise at respective two points which correspond to the minimum peaks of the triangular wave output and which appear alternately with each other. Accordingly, it is possible to generate an appropriate signal that is effective not to turn on PMOSs and NMOSs of the H-Bridge circuits simultaneously.

[0014] According to an eighth aspect of the present invention, the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, gates of two NMOSs are caused to fall at respective two points which correspond to crossings defined by ascending portions of a predetermined triangular wave output and a voltage output of the error amplifier and which appear alternately with each other, and gates of two PMOSs are caused to fall lagging behind falling of the gates of the two NMOSs. Accordingly it is possible to ensure that PMOSs and NMOSs are not caused to turn on simultaneously.

[0015] According to a ninth aspect of the present invention, a voltage feedback error amplifier is further provided for feedback-controlling an output voltage of the transformer. Accordingly it is possible to provide a con-

stant open voltage of the transformer even in case of no or poor connection of a discharge tube to the output terminal of the transformer.

[0016] According to a tenth aspect of the present invention, a protection circuit is further provided for inactivating the H-bridge circuit when an output voltage of the error amplifier exceeds a predetermined value. According it is possible to prevent an overcurrent from flowing in the discharge tube or an overvoltage from being applied to the discharge tube.

[0017] According to an eleventh aspect of the present invention, a protection circuit is further provided for inactivating the H-bridge circuit when an output of the voltage feedback error amplifier exceeds a predetermined value. Accordingly, it is possible to ensure that any damages to the transformer or any circuits are prevented.

[0018] According to a twelfth aspect of the present invention, a protection circuit is further provided for inactivating the H-bridge circuit when an output of the transformer exceeds a predetermined value.

[0019] According to a thirteenth aspect of the present invention, the predetermined value defined in the eighth aspect of the present invention is a reference voltage of a comparator of the protection circuit.

[0020] The above and other objects, aspects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram of an inverter circuit for a discharge tube of a first embodiment according to the present invention;

Fig. 2 is a block diagram of a burst circuit used in the inverter circuit for a discharge tube;

Fig. 3 shows frequency characteristics of the admittance |Y| at the primary side of a transformer with a resonance circuit formed at the secondary side in the inverter circuit for a discharge tube of the embodiment according to the present invention, and frequency characteristics of the phase difference θ between the voltage and the current;

Figs. 4(A) to 4(E) are timing charts of the operation of the inverter circuit for a discharge tube of the first embodiment according to the present invention;

Figs. 5(A) to 5(F) are timing charts of gate signals in the inverter circuit for a discharge tube of the first embodiment according to the present invention; and

Figs. 6 is a block diagram of an inverter circuit for a discharge tube of a second embodiment according to the present invention.

[0021] The present invention will now be described with reference to the accompanying drawings.

[0022] First of all, an explanation will be given on the first embodiment by reference to Figs. 1 to 5(A) to 5(F).

[0023] Referring to Fig. 1, a resonance circuit is composed of a parasitic capacitance 3 generated between a discharge tube 9 and a reflector at the secondary side of a transformer 1. As shown in Fig. 3, the transformer 1 has a maximum power efficiency at the point A0 where the phase difference θ between the voltage and the current at the primary side is minimum. In the frequency range A to cover -30° from the point A0, the transformer 1 has a power efficiency comparable to the maximum obtained at the point A0, as seen in the measured data. The point B is a resonance frequency of the secondary side, at which the transformer 1 is conventionally driven. The resonance circuit at the secondary side of the transformer 1 may comprise either a choke coil (not shown) provided in series with the transformer 1 and the parasitic capacitance 3, or a part of the transformer 1 (for example, a loose coupling portion of a magnetic-leakage flux-type transformer) and the parasitic capacitance 3.

[0024] The values of a resistance 5 and a capacitor 6 of an oscillation circuit 4 shown in Fig. 1 are set so as to make the frequency fall within the range A.

[0025] The operation of the inverter circuit for a discharge tube of the first embodiment will be described with reference to Figs. 1 to 4(A) to 4(E).

[0026] For better understanding, the description will be made first as for the case where a predetermined voltage Va at a terminal 28a is not inputted to an inverting input terminal 11a of an error amplifier 11, thereby failing to modulate light.

[0027] As shown in Fig. 1, a triangular wave output 7 (see Fig. 4 (A)) of the oscillation circuit 4 is inputted to a PWM circuit 8. A discharge tube 9 for back-lighting a liquid crystal is provided on a liquid crystal display (LCD) unit 2 at the secondary side of the transformer 1, and its voltage 9a is inputted to the inverting input terminal 11a of the error amplifier 11 by a voltage/current conversion circuit 10 which converts a current flowing in the discharge tube 9 into a voltage.

[0028] The error amplifier 11 outputs to the PWM circuit 8 an output voltage 12 corresponding to the current in the discharge tube 9. The PWM circuit 8 compares the triangular wave output 7 with the output voltage 12 and inputs a pulsed signal 13 to a counter circuit 14.

[0029] An output pulsed signal 16 of the oscillation circuit 4 is inputted to the counter circuits 14, 15 and a logic circuit 29. With the output pulsed signal 16 of the oscillation circuit 4 and output pulsed signals of the counter circuits 14, 15, the logic circuit 29 generates gate signals 18, 19, 20 and 21 that are inputted to an H-bridge circuit 17.

[0030] The H-bridge 17 is composed such that a series circuit comprising a PMOS (A1) and an NMOS (B2) and a series circuit comprising a PMOS (A2) and an NMOS (B1) are connected to each other in parallel. The H-bridge 17 operates on the gate signals 18, 19, 20 and 21 so that AC current controlled within the frequency range A flows at the primary side of the transformer 1, whereby the discharge tube 9 in the LCD unit 2 is driven

with a good power efficiency.

[0031] Therefore, a burst circuit 22 (to be described later) does not operate, and if the predetermined voltage Va from the terminal 28a is not inputted to the inverting input 11a, light is not modulated, the current in the discharge tube 9 is inputted to the inverting input 11a of the error amplifier 11, and the discharge tube 9 is feedback-controlled thereby performing a constant-current control within a frequency range for ensuring a good power efficiency.

[0032] The operation of the burst circuit 22 for modulating light of the discharge tube 9 will be described.

[0033] Referring to Fig. 2, the burst circuit 22 comprises a CR oscillator 40, a triangular wave voltage generator 41 and a comparator 42, and can be set to either one mode in which a resistance 23 is set to be higher than a predetermined value whereby a predetermined pulsed signal 24 inputted to a duty terminal 24a is outputted from the burst circuit 22 as a first burst signal 25b (see Fig. 4 (D)) or another mode in which the resistance 23 is set to be lower than a predetermined value whereby a triangular wave voltage 27 (see Fig. 4 (B)) determined by the resistance 23 and a capacitor 26 and oscillated, and a DC current 36 (see Fig. 4 (B)) inputted to the duty terminal 24a are compared with each other and a second burst signal 25a of the pulse wave (see Fig. 4 (C)) is outputted.

[0034] when the burst signal 25b from the burst circuit 22 is "H(High)", a transistor 28 is turned on, the error amplifier 11 outputs to the PWM circuit 8 the output voltage 12 corresponding to the current in the discharge tube 9, and the H-bridge circuit 17 is operated, whereby the discharge tube 9 is activated with the pulse wave shown Fig. 4 (E).

[0035] When the burst signal 25b from the burst circuit 22 is "L(Low)", the transistor 28 is turned off, the inverting input terminal 11a of the error amplifier is pulled up to a predetermined voltage Va applied to a terminal 28a, the error amplifier 11 is inactivated, the operation of the H-bridge circuit 17 is stopped, and the discharge tube is inactivated.

[0036] Thus, the discharge tube 9 is activated intermittently by the first burst signal 25b, and has its light modulated. In the case where the second burst signal 25a is used, the discharge tube 9 has its light modulated in the same way, therefore either of the burst signals can be used selectively.

[0037] In addition, a signal 33 generated by dividing the voltage at the output side of the transformer 1 through capacitors 31 and 32 is inputted to a protection circuit 30. The protection circuit 30 stops the operation of the logic circuit 29 when the voltage of the signal 33 exceeds a predetermined threshold value, preventing an excessive current from flowing to the discharge tube 9. Since it can happen that the PMOS (A1) and the NMOS (B2) connected to each other in series or the PMOS (A2) and the NMOS (B1) connected to each other in series in the H-bridge circuit 17 are turned on simultaneously when the gate signals 18, 19, 20 and 21 fall simultaneously, a delay circuit 35 is provided.

[0038] Figs. 5(A) to 5(F) show timing charts of gate signals in the inverter circuit for a discharge tube.

[0039] Referring to Figs. 5(A) to 5(C), the gate signal 18 to the PMOS(A1) and the gate signal 19 to the PMOS (A2) are caused to rise by the counter circuits 14 and 15 and the logic circuit 29 at points 18u and 19u, respectively, which correspond to the maximum peaks of the triangular wave output 7 and which appear alternately with each other and to fail at points 18d and 19d, respectively, which correspond to the crossings defined by the ascending portions of the triangular wave output 7 and the output voltage 12 of the error amplifier 11 and which appear alternately with each other. The PMOS (A1) and PMOS (A2) are activated by the gate signals 18 and 19, respectively.

[0040] Referring to Figs. 5(A), 5(D) and 5(E), the gate signal 20 to the NMOS(B1) and the gate signal 21 to the NMOS (B2) are caused to rise by the counter circuits 14 and 15 and the logic circuit 29 at points 20u and 21u, respectively, which correspond to the minimum peaks of the triangular wave output 7 and which appear alternately with each other and to fall at points 20d and 21d, respectively, which are equal to the points 18d and 19d, respectively. The NMOS(B1) and NMOS(B2) are activated by the gate signals 20 and 21 respectively.

[0041] As will be seen from Figs. 5(B) to 5(E), the timing of rising of the gate signals 20 and 21 is delayed with respect to that of the gate signals 19 and 18, respectively. On the other hand, the timing of falling of the gate signals 18 and 19 is delayed by a predetermined time t1 by a delay circuit 35 so that the PMOS(A1), PMOS (A2), NMOS(B1) and NMOS(B2) may not turn on simultaneously.

[0042] Therefore it becomes easy to generate appropriate gate signals 18, 19, 20 and 21 that do not make the PMOS(A1), PMOS(A2), NMOS(B1) and NMOS(B2) turn on simultaneously, by association of the triangular wave output 7 and the output voltage 12 of the error amplifier 11.

[0043] As described above, the inverter circuit for a discharge tube of the first embodiment according to the present invention improves the power efficiency of the transformer, and also suffers from little influence of the high-order frequencies due to the frequency being set to be lower than the resonance frequency, whereby the transformer can be designed easily.

[0044] Referring to Fig.6 showing the second embodiment according to the present invention, the inverter circuit for a discharge tube includes a voltage feedback error amplifier 51. The voltage feedback error amplifier 51 compares the application voltage signal 55 of the discharge tube 9 inputted to an inverting input terminal 51a with the predetermined voltage Vc to output to the PWM circuit 8 an output voltage 52 according to the voltage applied to the discharge tube 9. The application voltage signal 55 is obtained by dividing by resistances 58 and

59 the voltage appearing at the connection point between capacitors 31 and 32 connected in series with the secondary side of the transformer 1. The voltage feedback error amplifier 51 also outputs the output voltage 52 to a protection circuit 50. The protection circuit 50 which includes a comparator circuit is connected to a resistance 57 connected in series with the secondary side of the transformer 1 to receive an output current signal 53 from the transformer 1.

[0045] The operation and the circuit arrangement of the inverter for a discharge tube according to the second embodiment is same as those of the inverter circuit according to the first embodiment except the protection circuit 50 and the voltage feedback error amplifier 51 and therefore explanation thereof is omitted.

[0046] Now, operation of the protection circuit 50 and the voltage feedback error amplifier 51 of the inverter circuit according to the second embodiment will be explained.

[0047] As shown in Fig. 6, the voltage feedback error amplifier 51 compares the application voltage signal 55 inputted to its inverting input terminal 51a with the predetermined voltage Vc and outputs an output voltage 52 to the PWM circuit 8, so that feedback control is performed for application of a voltage to the discharge tube 9. With this control, an open voltage to the transformer 1 can be controlled to its predetermined value even in case of, for example, no connection or poor connection of the discharge tube 9 at the output of the transformer 1.

[0048] When the output voltage at the secondary side of the transformer 1 can show an abnormal value in case of, for example, no or poor connection of the discharge tube 9, the output voltage 52 of the voltage feedback error amplifier 51 or the output current signal 53 of the transformer 1 is compared with a reference voltage of the comparator circuit included in the protection circuit 50. And if the output voltage 52 or the current signal 53 exceeds the reference voltage of the comparator, the protection circuit 50 stops the operation of the logic circuit 29, thereby preventing an overcurrent from flowing into the discharge tube 9 or an overvoltage from being generared by the transformer 1.

[0049] A slow start circuit 34 outputs a relatively slowly increasing start drive signal 56 to the PWM circuit 8 in order to prevent an overvoltage from being instantly generated at a time of start of the circuit. In consideration of instant generation of such overvoltage due to some cause at a time of start of the circuit, the protection circuit 50 may be designed in such a manner that the logic circuit 29 is caused to stop its operation, when the output voltage 12 of the error amplifier 11 or the output voltage 52 of the voltage feedback error amplifier 51 exceeds a predetermined value after a predetermined time set by a built-in timer and that the logic circuit 29 is prevented accidentally from ceasing its operation.

[0050] The protection circuit 50 also functions to cease the operation of the logic circuit 29 when the output current signal 53 of the transformer 1 exceeds a predetermined value which falls out of its normal range. In this way, the transformer 1 and these circuits are protected from being damaged.

[0051] According to the second embodiment of the present invention, in addition to the technical advantages obtained by the first embodiment, it is easily possible to prevent an overcurrent from flowing in the discharge tube 9 or an overvoltage from being generated by the transformer 1 and also to prevent any damages to the transformer 1 and all the circuits.

[0052] While the illustrative and presently preferred embodiments of the present invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed and that the appended claims are intended to be construed to include such variations except insofar as limited by the prior art.

Claims

1. An inverter circuit for a discharge tube comprising a transformer which includes a resonance circuit composed of a parasitic capacitance of a discharge tube **characterized by** a H-bridge circuit which drives a primary side of the transformer at a frequency that is lower than a resonance frequency of the resonance circuit and that involves a phase difference between a voltage and a current at the primary side of the transformer, the phase difference falling within a predetermined range from its minimum point.

2. An inverter circuit for a discharge tube according to claim 1, wherein
   the predetermined range is below a resonance frequency at the secondary side of the transformer and covers -30° from the minimum point.

3. An inverter circuit for a discharge tube according to claim 1, further comprising
   a burst circuit for outputting a predetermined burst signal, whereby the primary side of the transformer is driven intermittently.

4. An inverter circuit for a discharge tube according to claim 1, wherein
   the burst circuit outputs an inputted pulsed signal as a burst signal when a resistance that determines an oscillating frequency is set to be higher than a predetermined value, and outputs a burst signal obtained from a predetermined DC signal and an oscillated triangular wave when the resistance is set to be lower than a predetermined value.

5. An inverter circuit for a discharge tube according to claim 1, wherein
   when the burst signal is high, an inverting in-

put of an error amplifier for feedback-controlling a current of the discharge tube is pulled up, whereby the primary side of the transformer is inactivated.

6. An inverter circuit for a discharge tube according to claim 1, wherein

the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, and a delay circuit is connected to gate circuits of the PMOSs.

7. An inverter circuit for a discharge tube according to claim 1, wherein

the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, and gates of two PMOSs are caused to rise at respective two points which correspond to the maximum peaks of a predetermined triangular wave output and which appear alternately with each other while gates of two NMOSs are caused to rise at respective two points which correspond to the minimum peaks of the triangular wave output and which appear alternately with each other.

8. An inverter circuit for a discharge tube according to claim 5, wherein

the H-bridge circuit is composed such that two series circuits each comprising a PMOS and an NMOS are connected to each other in parallel, gates of two NMOSs are caused to fall at respective two points which correspond to crossings defined by ascending portions of a predetermined triangular wave output and a voltage output of the error amplifier and which appear alternately with each other, and that gates of two PMOSs are caused to fall lagging behind falling of the gates of the two NMOSs.

9. An inverter circuit for a discharge tube according to claim 1, further comprising a voltage feedback error amplifier for feedback-controlling an output voltage of the transformer.

10. An inverter circuit for a discharge tube according to claim 5, further comprising a protection circuit for inactivating the H-bridge circuit when an output voltage of the error amplifier exceeds a predetermined value.

11. An inverter circuit for a discharge tube according to claim 9, further comprising a protection circuit for inactivating the H-bridge circuit when an output voltage of the voltage feedback error amplifier exceeds a predetermined value.

12. An inverter circuit for a discharge tube according to claim 1, further comprising a protection circuit for inactivating the H-bridge circuit when an output of the transformer exceeds a predetermined value.

13. An inverter circuit for a discharge tube according to claim 10, wherein the predetermined value is a reference voltage of a comparator of the protection circuit.

FIG. 1

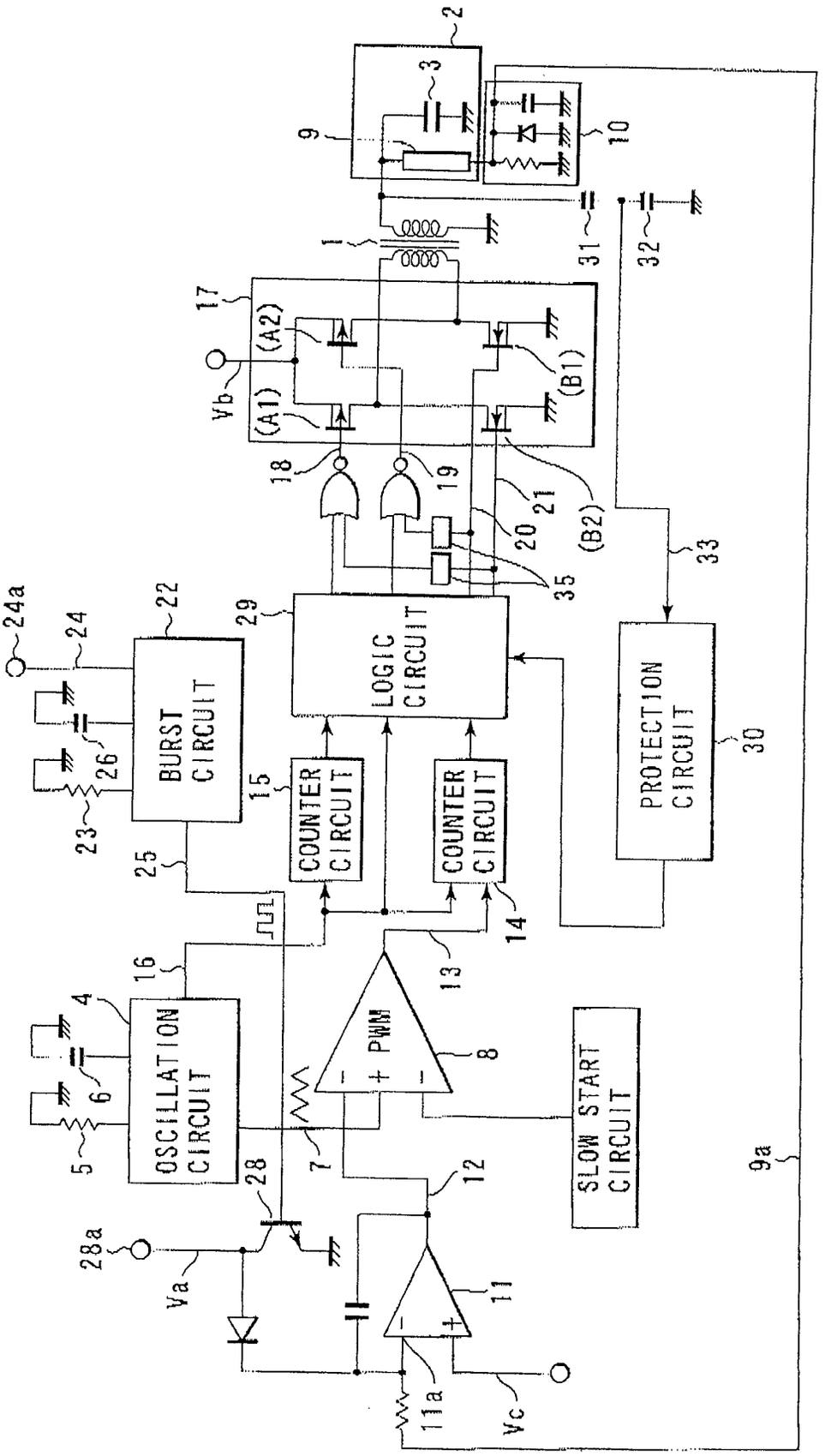

2
3
9
10
1
31
32
17
(A2)
(B1)
Vb
(A1)
18
19
21
(B2)
20
35
33
24a
24
22
29
LOGIC CIRCUIT
BURST CIRCUIT
26
23
25
15
COUNTER CIRCUIT
COUNTER CIRCUIT
PROTECTION CIRCUIT
30
14
13
16
4
6
5
OSCILLATION CIRCUIT
PWM
8
7
SLOW START CIRCUIT
28
12
28a
Va
11
11a
Vc
9a

FIG. 2

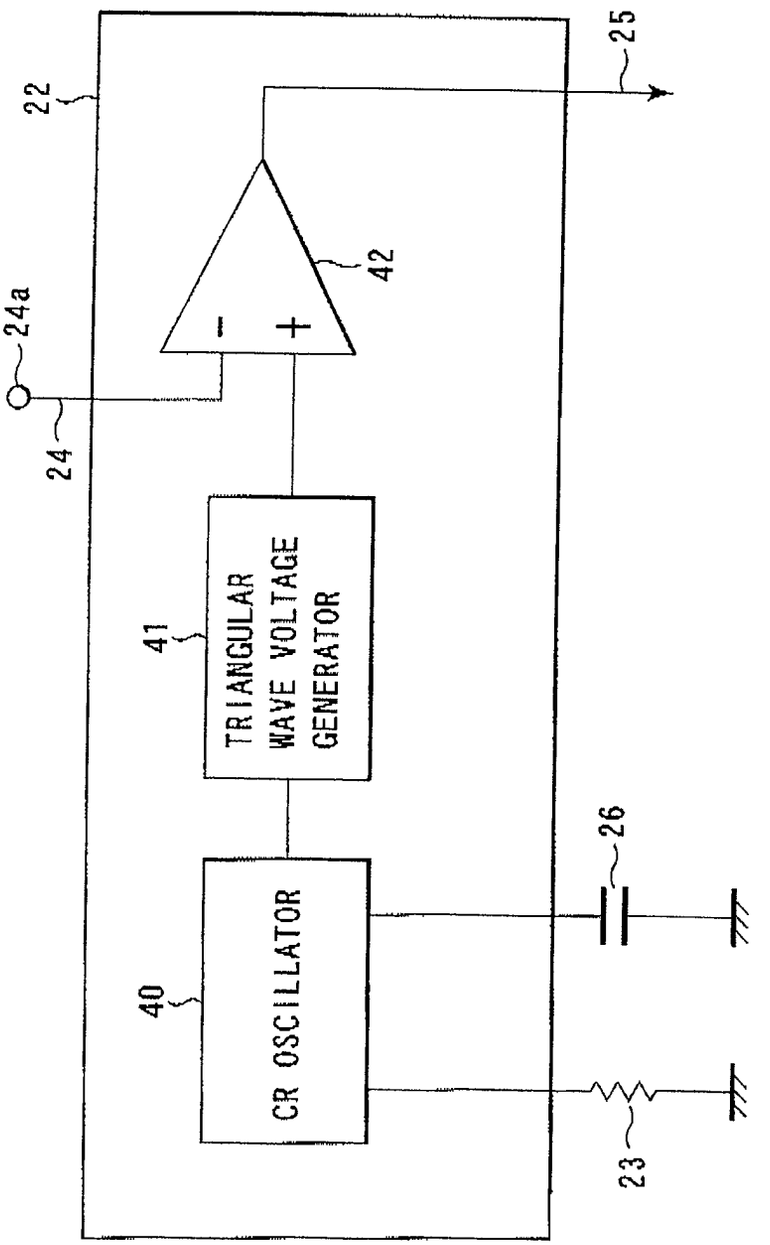
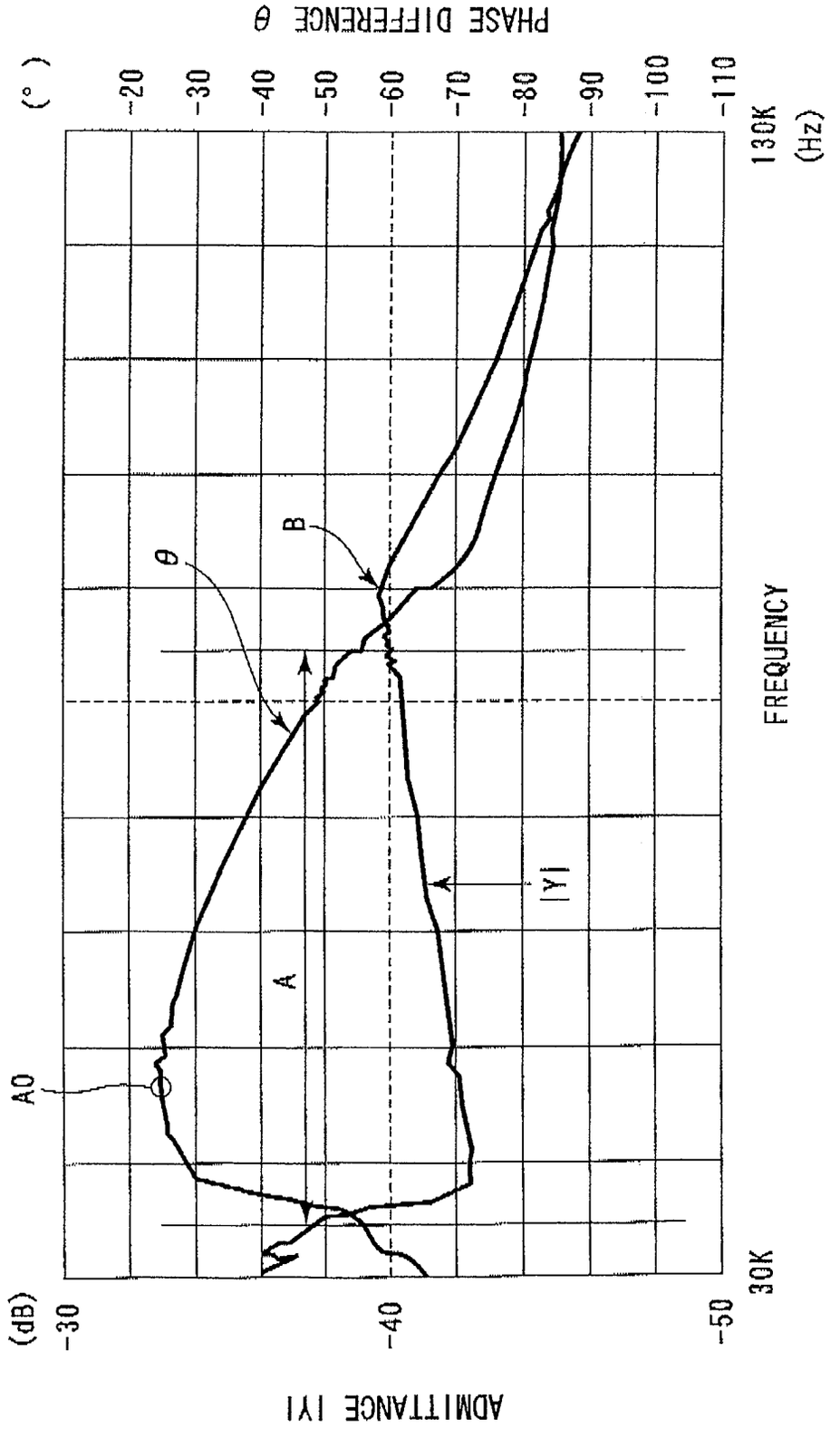

22
25
42
24a
24
41
TRIANGULAR WAVE VOLTAGE GENERATOR
26
40
CR OSCILLATOR
23

FIG. 3


PHASE DIFFERENCE θ
(°)
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
130K
(Hz)
FREQUENCY
30K
B
θ
A
|Y|
A0
(dB)
-30
-40
-50
ADMITTANCE |Y|

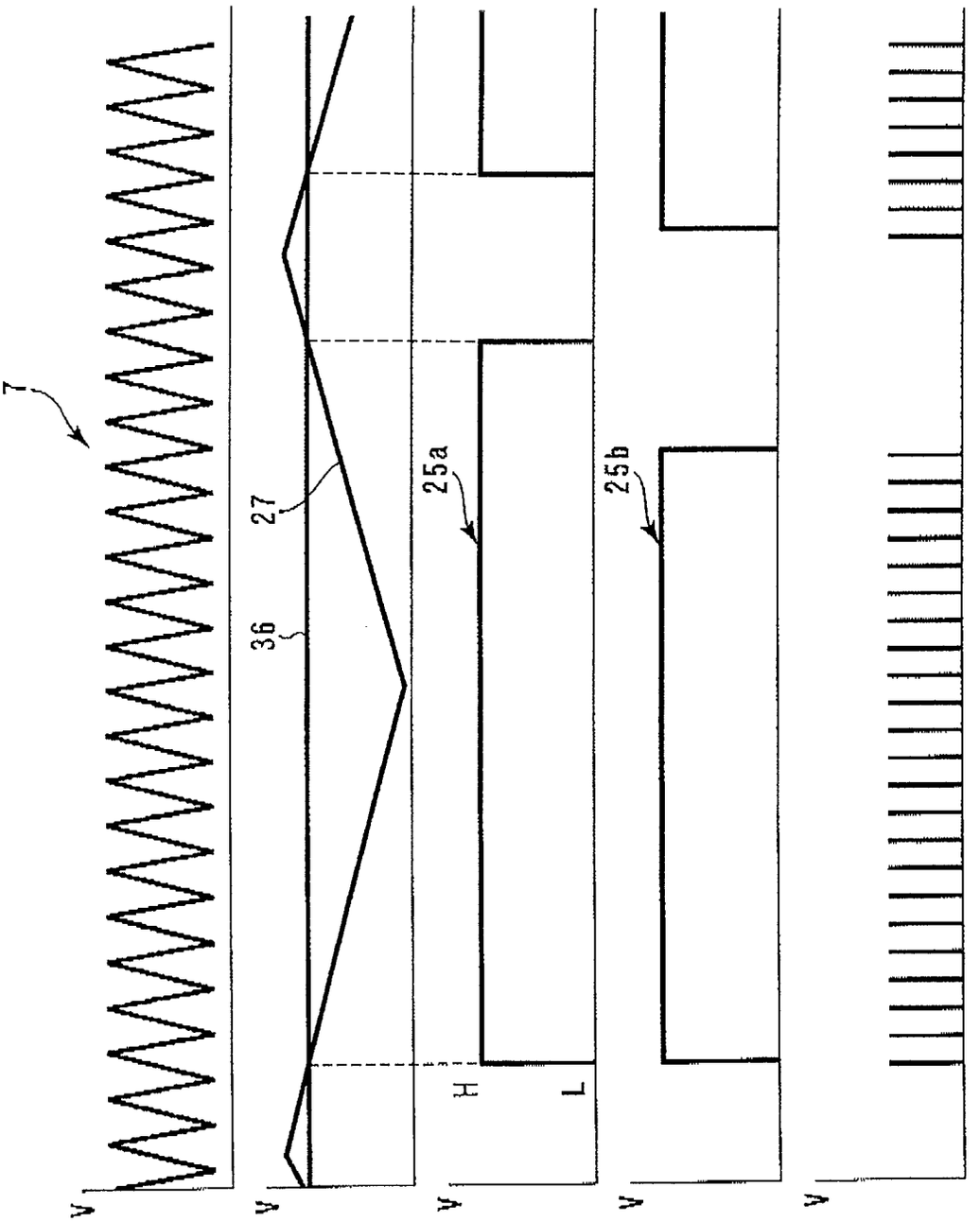


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

FIG. 4E

FIG. 5A

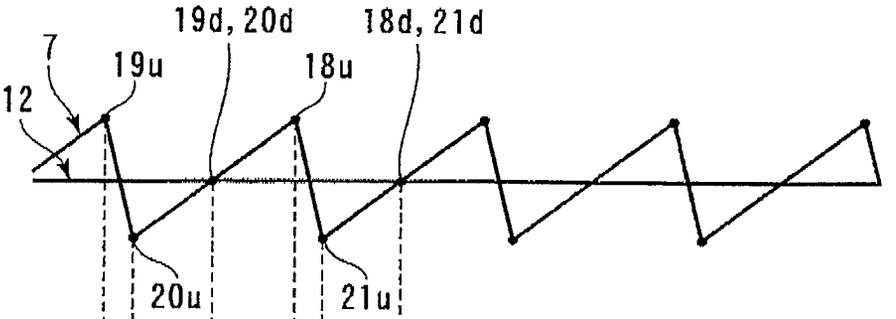


FIG. 5B

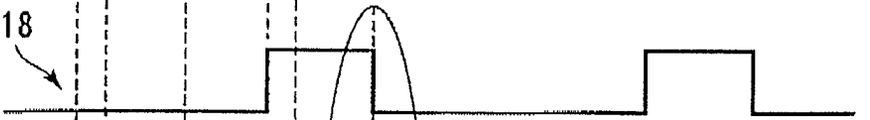


FIG. 5C

FIG. 5D

FIG. 5E

FIG. 5F

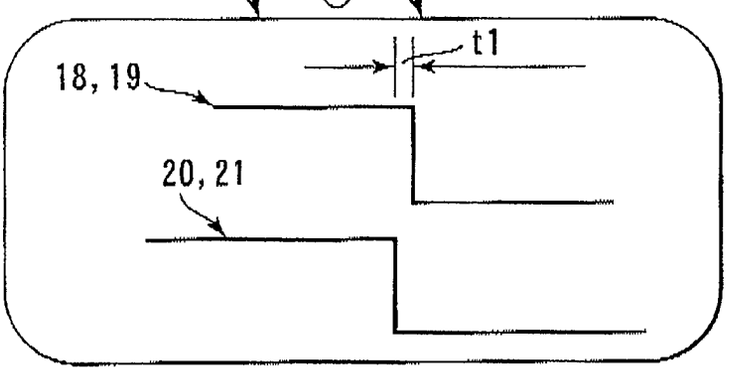
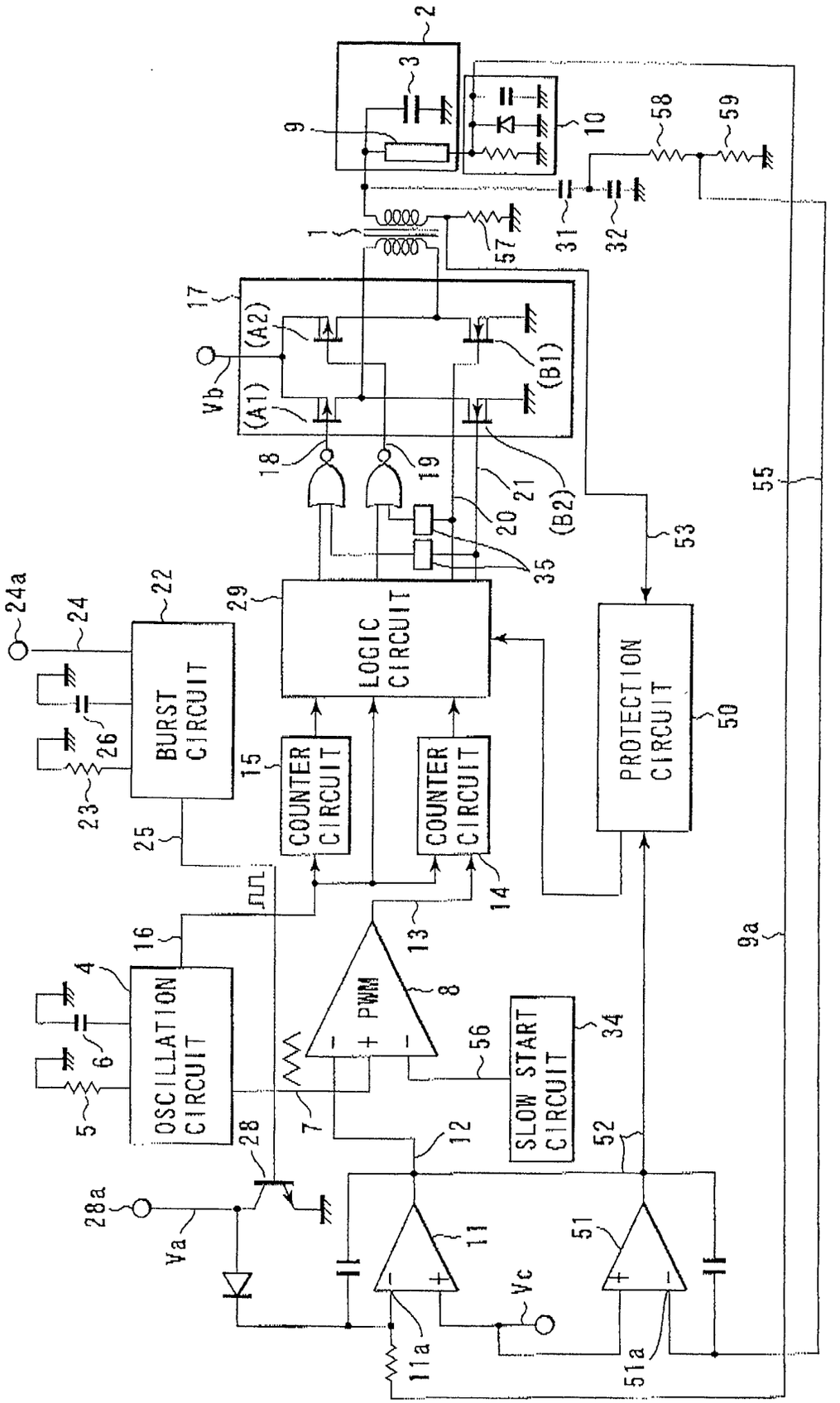


FIG. 6


2
3
9
10
58
59
1
57
31
32
17
(A2)
(B1)
Vb
(A1)
18
19
21
(B2)
20
35
53
55
24a
24
22
29
LOGIC CIRCUIT
BURST CIRCUIT
26
23
25
15
COUNTER CIRCUIT
COUNTER CIRCUIT
14
PROTECTION CIRCUIT
50
16
13
4
6
5
OSCILLATION CIRCUIT
28
PWM
8
56
SLOW START CIRCUIT
34
7
12
52
9a
28a
Va
11
Vc
51
11a
51a

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 6562

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 14, 5 March 2001 (2001-03-05) -& JP 2000 308358 A (TAIYO YUDEN CO LTD), 2 November 2000 (2000-11-02)	1-3,9	H05B41/282 H05B41/285 H05B41/392 H01L41/04
Y	* the whole document *	4-6, 10-13	

Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 05, 14 September 2000 (2000-09-14) -& JP 2000 058289 A (TAIYO YUDEN CO LTD), 25 February 2000 (2000-02-25) * paragraph [0013] - paragraph [0020] * * paragraph [0063] - paragraph [0090]; figure 13 *	4,5	

Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 20, 10 July 2001 (2001-07-10) -& JP 2001 086758 A (TAIYO YUDEN CO LTD), 30 March 2001 (2001-03-30)	6	
A	* paragraph [0050] - paragraph [0051]; figures 12,13 *	7,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H05B H01L

Y	US 6 259 615 B1 (LIN YUNG-LIN) 10 July 2001 (2001-07-10) * column 7, line 62 - column 9, line 4; figure 2 *	10-13	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	20 December 2002	Ferla, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 6562

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

20-12-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2000308358 A	02-11-2000	US 6348755 B1	19-02-2002
JP 2000058289 A	25-02-2000	NONE	
JP 2001086758 A	30-03-2001	NONE	
US 6259615 B1	10-07-2001	US 2002180380 A1	05-12-2002
		US 2001036096 A1	01-11-2001

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82