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(54) Metal Oxide Semiconductor Field Effect Transistor

(57) A metal oxide semiconductor transistor (200) integrated in a wafer of semiconductor material (30) and comprising a gate structure (3, 11) located on a surface of the said wafer and including a gate oxide layer (3). The transistor (200) is characterized in that the said gate oxide layer (3) includes a first portion (4) having a first thickness (t1) and a second portion (5) having a second thickness (t2) differing from the first thickness.

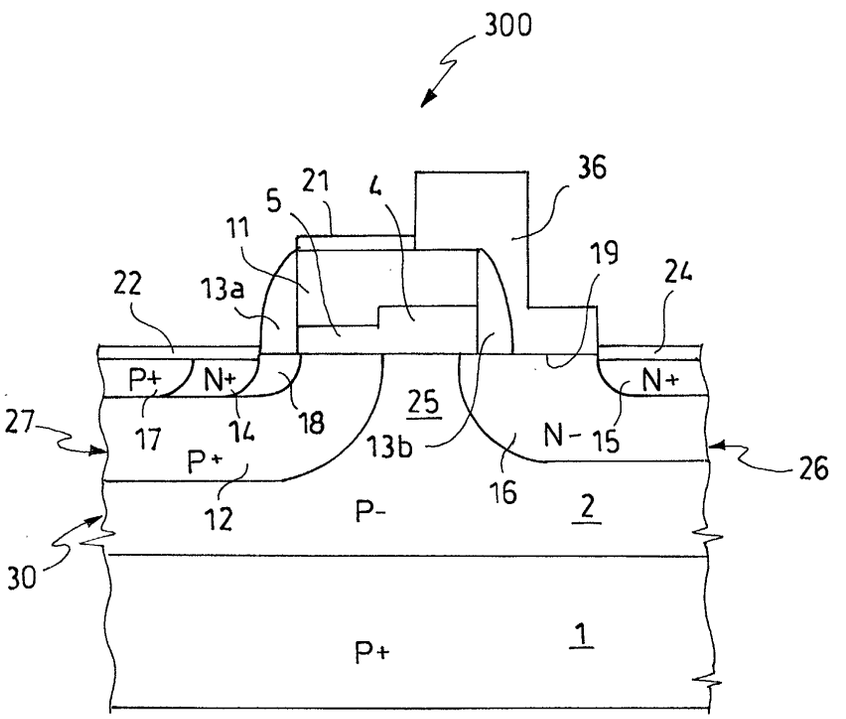

FIG. 6

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Description

[0001] The present invention relates to metal oxide semiconductor field-effect transistors.

[0002] For the purposes of the present invention, the expression "metal oxide semiconductor field-effect transistors" (MOSFET) denotes various field-effect transistor structures, each comprising a wafer of semiconductor material, also called the substrate or body, a drain region and a source region integrated in the wafer, and a gate structure including a layer of conductive material separated from the wafer by a layer of insulating material (typically an oxide, such as silicon dioxide).

[0003] It should be noted that the expression "metal oxide semiconductor" (MOS) is also used for transistors in which the layer of conductive material of the gate is formed by a layer of doped polysilicon, instead of metal. It should also be mentioned that metal oxide semiconductor transistors are also called insulated-gate field-effect transistors (IGFET, insulated-gate FET), to emphasize that the gate electrode is electrically insulated from the wafer or body.

[0004] For example, for the purposes of the present invention the term MOSFET is applied not only to transistors having the standard structure, such as the conventional NMOS and PMOS transistors, but also lateral double-diffusion MOSFETs (LDDMOSFET or LDMOSFET), or other possible MOSFET structures comprising a different number of diffused regions and/or a different arrangement thereof in the substrate, as well as different combinations of the dopants. It will be recalled that an LDMOSFET, referred to for brevity below as an LDMOS transistor, comprises, in addition to the drain and gate regions, a body region which is also diffused under the gate oxide and a drift region associated with the drain.

[0005] As is known, one of the parameters characterizing a MOSFET is the breakdown voltage, BV. With reference to LDMOS transistors for example, the breakdown voltage BV is the voltage of the drain electrode at which the junction between the drain and body is subject to an avalanche effect (avalanche breakdown). The breakdown voltage BV is correlated with the dopants of the drain (or drift) and body regions and with the curvature and denser spacing of the lines of potential induced by the gate electrode.

[0006] In the known art, two different methods are used to obtain sufficiently high values of breakdown voltage (BV) in MOS or LDMOS transistors.

[0007] In the first method, the doping of the drain and body regions is appropriately determined, and, in particular, the doping of the drain region is reduced. This method has the disadvantage of decreasing the performance of the transistor, causing an increase in its series resistance (Ron).

[0008] The second conventional method proposes the use of a relatively thick gate oxide layer. This solution has the disadvantage of reducing the transconductance Gm and the current-carrying capacity of the LDMOS transistor, thus decreasing the performance of the said transistor in terms of gain.

[0009] In the known art, therefore, in the case of LDMOS transistors the doping and thickness of the gate oxide must be determined in such a way as to provide a compromise between the requirements of a suitable breakdown voltage, a convenient gain and an adequate series resistance, and this compromise cannot be considered to be wholly satisfactory.

[0010] The object of the present invention is to propose a metal oxide semiconductor field-effect transistor which overcomes the limitations of conventional transistors.

[0011] The object of the present invention is achieved by a metal oxide semiconductor integrated in a wafer of semiconductor material and comprising a gate structure located on one surface of the said wafer and including a gate oxide layer, characterized in that the said gate oxide layer includes a first portion having a first thickness and a second portion having a second thickness differing from the first thickness.

[0012] Another object of the present invention is a method for manufacturing a metal oxide semiconductor field-effect transistor.

[0013] The characteristics and advantages of the present invention will be more clearly understood from the following detailed description of examples of its embodiment provided without restrictive intent, and illustrated in the attached drawings, in which:

- Figures 1 to 4 show schematically different stages of production of an LDMOS transistor according to a particular embodiment of the invention;
- Figure 5 shows schematically an LDMOS transistor having silicide surface layers according to a first embodiment of the invention,
- Figure 6 shows schematically an LDMOS transistor having silicide surface layers according to a second embodiment of the invention;
- Figure 7 shows schematically an N-channel MOS transistor according to a particular embodiment of the invention,
- Figure 8 shows schematically a P-channel LDMOS transistor which can be constructed according to the method of the invention;
- Figure 9 shows the variation of the transconductance and saturation current as a function of the voltage Vgs relative to an N-channel LDMOS transistor and a P-channel LDMOS transistor according to the invention.

[0014] In the figures to which the following description refers, the same numerical references will be used to indicate identical or similar elements.

[0015] With reference to Figures 1a to 4, a description will be given of a particular example of a process of manufacturing an LDMOS transistor integrated in a wafer 30 of semiconductor material according to the invention.

Preferably, the LDMOS transistor of this example is of a type which can be used for radio-frequency power applications. However, as mentioned above and as will be evident to persons skilled in the art, the teachings of the present invention are also applicable to MOSFETs of types other than those described here by way of example.

[0016] According to the example, the wafer 30 is of the P^+-P^- type, in other words of the type normally used for CMOS platforms, and comprises a P^+-type silicon substrate 1 and a P^--type epitaxial layer 2 grown on the substrate by conventional methods. The epitaxial layer 2 forms a separating surface 10a between the substrate 1 and an outer surface 1b opposed to it.

[0017] The epitaxial layer 2 has a conductivity of the same type as that of the substrate 1, but smaller than this. For example, in terms of resistivity, the silicon substrate 1 has a resistivity in the range from 1 to 100 mΩ cm and a thickness in the range from 10μm to 1000μm. In a particular example, at the end of the production process the thickness of the substrate 1 is 200μm. The epitaxial layer 2 has a resistivity which is, for example, in the range from 1 to 100Ω cm, and has a thickness which is, for example, in the range from 1 to 10μm.

[0018] The method according to the invention comprises the formation of an insulating gate layer 3 on the surface 10b. The insulating gate layer 3 can be made from any suitable dielectric material. For example, the insulating gate layer 3 can be an oxide, particularly silicon dioxide.

[0019] The gate oxide 3 has a non-uniform thickness and comprises a first portion 4 having a thickness t1 and a second portion 5 having a thickness t2 which is different from the thickness t1. As is shown clearly in Figure 1b, the "thickness of the gate oxide" denotes the distance between the surface of the gate oxide facing the surface 10b of the wager 30 and the opposite surface of the gate oxide. In Figure 1b, the first portion 4 and the second portion 5 are located on opposite sides of an ideal separating surface S.

[0020] In particular, the thickness t1 of the first portion 4 is greater than the thickness t2 of the second portion 5.

[0021] For example, the thickness t1 is in the range from 20 A° to 500 A° and the thickness t2 is in the range from 10 to 250 A°.

[0022] Preferably, for radio-frequency power applications, the thickness t1 is in the range from 100 A° to 300 A° and the thickness t2 is in the range from 25 to 150 A°.

[0023] In one particular example, the thickness t1 is approximately 180 A° and the thickness t2 is approximately 70 A°.

[0024] A description is given below (Figures 2a-2e) of a particularly advantageous method which can be used, starting with the wafer 30 of Figure 1a, to form a gate structure, a body region and a drift region of the LDMOS transistor. In particular, according to the example, the gate structure includes the gate oxide 3 and a layer of conductive gate material such as, preferably, a layer of polysilicon.

[0025] A first layer of oxide 6, having a thickness t3 in the range from t2 to t1 for example, is formed, preferably by growing, on the surface 10b of the epitaxial layer 2. According to the values given above, the layer 6 can have, for example, a thickness of t3=160 A°.

[0026] The ideal surface S for separating the two portions 4 and 5 of the gate oxide 3 is then identified in the surface 6. The surface S ideally separates the first layer of oxide 6 in a first region 6a located above the part of the surface 10b on which the first portion 4 of the gate oxide 3 will lie, and a second region 6b located above the part of the surface 10b on which the second portion 4 of the gate oxide 3 will lie.

[0027] The region 6b of the layer 6 is then removed. This removal can be carried out, for example, by a conventional photolithographic method comprising a stage of forming a photoresist mask and a stage of chemical etching. In greater detail, the forming of the photoresist mask requires the use of a layer of photoresist (not shown) placed on a surface 9 of the layer of oxide 6 and the partial irradiation of this photoresist with electromagnetic waves (ultraviolet waves or X-rays, for example) which pass through a suitable photomask (not shown). The irradiation of the photoresist polymerizes the portion of the photoresist lying above the first region 6a of the oxide 6 which is not to be removed.

[0028] Chemical etching is then carried out to remove the non-polymerized portion of the photoresist and the underlying second region 6b of the oxide layer 6 in such a way as to expose a surface 8 of the wafer 30. Finally, the removal of the photoresist is completed.

[0029] A layer of oxide 7 is then grown on the surface 8 of the wafer 30 and on a surface 9 of the second region 6a. This growing stage is carried out in such a way that the portion of the layer of oxide 7 present on the surface 8 has a thickness of t2 and the portion of the layer 7 grown on the surface 9 is such that the layers 6a and 7 have a combined thickness of approximately t1.

[0030] A layer of polysilicon 500, suitably doped, is then deposited on top of the oxide layer 7, as shown in Figure 2d, in order to make it conductive. A portion of this polysilicon layer 500 is designed to form the gate polysilicon of the transistor.

[0031] A first layer of masking made from photoresist 501, or more briefly a photoresist mask, is then formed on top of the polysilicon layer 500. This first photoresist mask 501 is produced from a layer of photoresist placed on the polysilicon layer 500 and suitably irradiated with electromagnetic waves which pass through a suitable photomask in such a way as to cause the polymerization of some of the portions of the layer.

[0032] With the aid of this first photoresist mask 501, the polysilicon layer 500 is etched, by conventional methods for example, to remove the portion of the polysilicon which is not covered by the polymerized portions of this mask 501. As shown in Figure 2a, this etching makes it possible to form a lateral wall W-S (facing the

source side, for example) of the polysilicon gate layer of the transistor.

[0033] It should be noted that, after the chemical etching, the first photoresist mask 501 and the polysilicon layer 500 have an aperture which exposes a surface S1 of the oxide layer 7 having a thickness t2 in the proximity of the lateral wall W-S.

[0034] According to the example, the method continues with a stage of forming a P-type body region 12 which is developed within the epitaxial layer 2.

[0035] In particular, the region 12 is formed by ion implantation. Preferably, boron ions are implanted with an ion beam F1 of suitable energy and density (shown schematically by arrows in Figure 2a) which strikes the surface S1 exposed by the photoresist mask 501, passing through the oxide layer 7.

[0036] Advantageously, an inclined implantation is carried out; in other words, the wafer 30 is inclined at a suitable angle to the ion beam F1 in such a way that the beam of ions can also pass obliquely through the polysilicon layer 500, but at the same time this polysilicon layer is shielded by the first photoresist mask 501. It should be noted that, advantageously, the first photoresist mask 501 is automatically aligned with the underlying polysilicon 500 because it is the product of the same stage of masking (and, in particular, of the same photomask) and etching as that carried out to form the wall W-S.

[0037] This provides a highly accurate alignment between the layers 500 and 501, which could not be obtained by forming a separate photoresist layer on the remaining portion of the polysilicon layer 500 after a stage of etching carried out to form the polysilicon 500. The correct alignment of the overlapping layers 500 and 501 makes the execution of the inclined implantation highly accurate.

[0038] This inclined implantation is used to form a body region 12 extending over the desired length (generally fractions of a μm) under the polysilicon layer 500.

[0039] On completion of the implantation, the first photoresist mask 501 is removed.

[0040] A second layer of masking made from photoresist 502, or more briefly a second photoresist mask 502, is then formed on top of the polysilicon layer 500 (Figure 3a). This second photoresist mask 502 is produced from a layer of photoresist placed on the polysilicon layer 500 and suitably irradiated with electromagnetic waves which pass through a suitable photomask in such a way as to cause the polymerization of some of the portions of the layer.

[0041] With the aid of this second photoresist mask 502, the polysilicon layer 500 is etched, by conventional methods for example, to remove the portion of the polysilicon which is not covered by the polymerized portions of this mask 502. As shown in Figure 3a, this etching makes it possible to form a lateral wall W-D (facing the drain side, for example) of the polysilicon gate layer of the transistor. This second etching of the polysilicon layer 500 forms a polysilicon gate layer 11.

[0042] It should be noted that, after etching, the second photoresist mask 502 and the polysilicon layer 500 have an aperture which exposes a surface S2 of the oxide layer 7 having a thickness t1 in the proximity of the lateral wall W-D. Additionally, the photoresist layer 502 shields the gate polysilicon 11 and the surface of the oxide layer 7 having a thickness t2.

[0043] According to the example, the method continues with a stage of forming an N-type drift region 16 which is developed within the epitaxial layer 2.

[0044] In particular, the region 16 is formed by ion implantation. Preferably, phosphorus ions are implanted with an ion beam F2 of suitable energy and density (shown schematically by arrows in Figure 3a) which strikes the surface S2 exposed by the photoresist mask 502, passing through the oxide layers 7 and 6a. In particular, an inclined implantation is carried out in a similar way to that described for the body region 12, in such a way that the ion beam F2 can pass obliquely through the gate polysilicon 11, but at the same time this polysilicon layer is shielded by the second photoresist mask 502. Thus the implanted ions can occupy a region extending for several fractions of a μm under the gate polysilicon 11.

[0045] It should be noted that, advantageously and similarly to the process described for the formation of the body region 12, the implantation of the drift region 16 is carried out with the same photoresist mask 502 as that made for the forming of the polysilicon gate layer 11, and therefore with a mask automatically aligned with the said layer 11.

[0046] After the two stages of implantation of the body region 12 and the drift region 16, a stage of heat treatment is advantageously carried out to enable the corresponding dopants to be fully diffused and activated.

[0047] It should be noted that this heat treatment can be identical to one of those already specified by the VLSI (Very Large Scale Integration) CMOS platform (carried out, for example, at less than 1000°C and in particular at approximately 900 °C), and can therefore be such that there is no effect on the electrical characteristics of the CMOS components which can be formed on the said wafer 30.

[0048] It should be noted that, in the conventional manufacture of LDMOS transistors not integrated with CMOS devices, the drift and body regions are produced by a diffusion process which requires heat treatment at a high temperature, generally above 1000°C.

[0049] In the particular method described above according to the invention, the use of inclined implantation enables the body region 12 and drift region 16 to be extended under the polysilicon 11 even without the heat treatment.

[0050] According to a preferred example of embodiment of the invention, CMOS devices (not shown), such as conventional N- and P-channel MOSFETs, are formed on the wafer in addition to the LDMOS transistor.

It is clear from the above description that the method according to the invention is compatible with the parallel formation of CMOS devices on the same wafer 30.

[0051] It should also be noted that the advantages offered by inclined implantation and those offered by using the same photoresist layers for forming the polysilicon 11 and the subsequent implantation are also considerable in the manufacture of an LDMOS with a gate oxide layer having a uniform thickness.

[0052] Figure 3b shows the polysilicon gate layer 11, produced by the definition of the layer 500, and the gate oxide 3 produced after a stage of removal of the photoresist 502 and of the layers of oxide (7 and 6a) not lying under the polysilicon gate layer 11.

[0053] In one embodiment of the invention, the body region 12 has a concentration of dopant impurities in the range from 10^{16} to 10^{19} ions/cm^3.

[0054] According to the example described, and as shown in Figure 3b, the N^--type region 18 is then formed, as is usually done for CMOS devices, in other words as an N-type region indicated conventionally by the symbol Nldd (region of weak doping) and having, in the example, a doping in the range from 10^{15} to 10^{19} ions/cm^3. The region 18 can be formed in a conventional way, by the formation of photoresist masks, followed by ion implantation.

[0055] Lateral spacers 13a and 13b, illustrated in Figure 4, are preferably formed on the lateral walls of the polysilicon gate layer 11 and of the gate oxide 3. These lateral spacers are formed by using prior art technologies comprising stages of chemical vapour phase deposition (CVD) of a suitable material, followed by a stage of reactive ion etching.

[0056] The lateral spacers 13a and 13b can consist of any suitable insulating material such as silicon oxide, polysilicon, or, preferably, silicon nitride. As is known, lateral spacers are commonly used in CMOS processes to create less doped areas of the source and drain regions at the body/drain and body/source junctions, in order to reduce the electrical fields, and more doped areas of the source and drain regions, automatically aligned with the former areas by means of the spacers, for more resistive contacting.

[0057] A source region 14 and a drain region 15, both of the N^+ type, are then formed within the regions 18 and 16 respectively, by ion implantation through a photoresist mask, as is usually done for the source and drain regions of CMOS devices.

[0058] For example, the source region 14, the drain region 15 and the drift region 16 have a conductivity in the range from 10^{15} to 10^{19} ions/cm^3 or, preferably, in the range from 10^{16} to 10^{18}. Typically, the region 18 located on the source side is more heavily doped than the drift region 16 on the drain side.

[0059] A body contact region 17, of the P^+ type for example, is formed within the source region 14 in a similar way to that described above.

[0060] It should be noted that the signs of the P/N conductivity of the regions 1, 2, 12, 14, 17, 18 and 15, 16 and the intensity of the corresponding doping, expressed by the symbols +/-, can differ from those indicated above by way of example and shown in the figures. Moreover, the teachings of the present invention are also applicable to LDMOS transistors having a structure different from that of the CMOS platform described, such as a structure comprising P or N substrates with or without buried layers.

[0061] It is important to note that the method described above for manufacturing an N-channel LDMOS transistor on a CMOS platform also enables P-channel LDMOS transistors to be manufactured in parallel on the same wafer 30. In other words, the method according to the present invention can be used to form complementary LDMOS transistors on a VLSI CMOS platform. A P-channel LDMOS transistor 600 which can be formed by the method described above is shown in Figure 8. It will be noted that its layout is similar to that of the transistor of Figure 4, except for the sign of the conductivity of some doped regions. In greater detail, the transistor 600 comprises an N^+ body region 12', a P^+ source region 14', an N^+ source contact region 17', a weakly doped Nldd region 18', a P^-drift region 16', and a P^+ drain region 15'.

[0062] In particular, the body region 12' and drift region 16' can be produced with the same masks and implantation as those used for the body and drain regions 12 and 16 of the N-channel transistor of Figure 4.

[0063] It should be noted that the method according to the invention which makes use of inclined implantation enables the doping and the lengths of the body and drift regions to be defined in such a way as to optimize the performance of the N-channel or P-channel LDMOS.

[0064] We shall now return to the transistor of Figure 4, indicated as a whole by 100, in which we can distinguish a first active region 26 and a second active region 27, which extend from the surface of the epitaxial layer 2 towards the interior of the said layer.

[0065] The first active region 26 comprises the drain region 15 and the drift region 16. The second active region 27 comprises the body region 12, the source region 14, the body contact region 17 and the N-type region 18 located under the source spacer 13a. The first and second active regions are spaced apart from a region 25 included in the epitaxial layer 2 in which part of the transistor's conducting channel will be developed.

[0066] It should be noted that the gate oxide layer 3 extends partially over the separating regions 25 and that its first portion 4 is close to the first active region 26 and its second portion 5 is close to the second active region 27. In other words, the first portion 4 is located on the "drain side" of the transistor 100, and the second portion 5 is located on the "source side" of the said transistor.

[0067] In particular, the first portion 4 and the second portion 5 are superimposed, respectively, on at least one part of the first active region 26 and at least one part

of the second active region 27.

[0068] In greater detail, the first portion 4 of the gate oxide 3 extends in such a way that it is superimposed on the separating region 25 and on one part of the drift region 16, and the second portion 5 of the gate oxide 3 extends in such a way that it is superimposed on at least one part of the body region 12.

[0069] It should be noted that the first portion 4 of the gate oxide 3, close to the drain region 15, has a thickness t1 which can be specified in such a way as to obtain a desired breakdown voltage BV. In particular, the breakdown voltage can be increased by increasing the thickness t1. The breakdown voltage can always be varied by the selection of the thickness t1, provided that the doping of the drain and body regions is not such that the value of the breakdown voltage is predetermined.

[0070] The increase of the breakdown voltage is correlated with an increase in the distance between the gate polysilicon layer 11 and the first active region 26. As this distance increases, there is a decrease in the electrical field responsible for the breakdown which can occur in the surface area of the epitaxial layer 2 facing the gate oxide 3 and corresponding to a portion of the polysilicon layer 11 close to the drain region 16.

[0071] Advantageously, the present invention can be used in the field of radio-frequency power applications to obtain a breakdown voltage BV which is higher than that obtainable with conventional LDMOS transistors having uniform oxide.

[0072] For example, for low-voltage applications, with the values of the thicknesses t1 and t2 indicated above (180 A° and 70 A°) , and where the doping of the body region 12 and drift region 16 is of the order of 10^{17} ions/cm^3, breakdown voltages BV in the range from 16-20 V have been obtained.

[0073] For conventional LDMOS transistors with uniform gate oxide, having a thickness of 70 A°, and doping comparable to that indicated above, a breakdown voltage of approximately 10 V is obtained, in other words one considerably lower than that obtainable by applying the teachings of the present invention.

[0074] Additionally, the increase in the thickness t1, by permitting a limitation of the surface electrical field, reduces the undesired generation of "hot carriers" and enables the gate-drain feedback capacity to be reduced, with a consequent improvement in the performance of the transistor at high frequency.

[0075] It should be noted that the second portion 5 of the gate oxide 3 has a thickness t2 which can be selected in such away as to obtain a predetermined value of the transconductance Gm of the LDMOS transistor. The value of this transconductance is proportional to the gate-body capacity C_{ox}, which is inversely proportional to the distance between the gate electrode and the body region, in other words to the thickness t_2 of the second portion 5. In particular, decreasing the thickness of this portion 5 produces an increase in the transconductance Gm and, therefore, an improvement in the performance of the transistor in terms of amplification gain.

[0076] For example, with thicknesses t1 and t2 of 180 and 70 A° respectively, a Gm of approximately 200 mS/mm was obtained, as against approximately 80 mS/mm which is obtainable with a uniform thickness according to the prior art, and equal to 180 A° =t1=t2 with equal breakdown voltage.

[0077] The possibility of selecting the thicknesses of the first portion 4 and second portion 5 of the gate oxide 3 according to the present invention is particularly advantageous. This is because this possibility enables transistors to be produced with a high breakdown voltage BV and a high transconductance, or, at any rate, makes it unnecessary to accept a decrease of the transconductance Gm of the transistor in order to achieve desired values of the breakdown voltage. By applying the teachings of the invention, it is possible to achieve a dual function of increasing the transconductance Gm while maintaining the breakdown voltage BV at satisfactory levels.

[0078] Advantageously, the method according to the invention provides stages of formation of silicide on suitable surfaces of the wafer 30 of Figure 4.

[0079] In Figure 4, the reference numbers 19 and 20 indicate a first and a second area respectively, corresponding, respectively, to the surface of the first active region 26 and that of the second active region 27.

[0080] Figure 5 shows a transistor 200 with a structure similar to that of the transistor 100. The transistor 200 comprises surface layers of silicide 21, 22 and 23, formed, respectively, on the surface of the gate polysilicon 11, on the first active area 19 and on the second active area 20. The surface layers 21, 22 and 23 are, for example, formed from titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$) or tungsten silicide (WSi_2)

[0081] The silicidizing of the surfaces of the gate 11 and of the active areas 19 and 20 has the advantage of decreasing their surface resistivity while improving the performance of the transistor.

[0082] Preferably, the silicidizing is carried out by the conventional method known as self-aligned silicidizing, or formation of a "salicide" (acronym of "self-aligned silicide") which permits the formation of layers of silicide aligned with the underlying regions of silicon or polysilicon (salicidizing).

[0083] For example, the layers of silicide 21, 22 and 23 are formed by a stage of deposition (by spraying or "sputtering", for example) of a thin layer of a refractory metal over the whole surface of the wafer 30, and in particular over the active areas 19 and 20 and on the surface of the polysilicon layer 11.

[0084] The wafer 30 is then subjected to heating, allowing a chemical reaction to take place between the deposited metal and the underlying silicon, resulting in the formation of the three regions of silicide 21, 22 and 23.

[0085] Preferably, the metal used for silicidizing is titanium or cobalt. For tungsten silicide, direct deposition

of WSi_2 on the polysilicon 11 can be used, instead of the self-aligned silicide method.

[0086] It should be noted that the transistor 200, provided with the three layers of silicide 21, 22 and 23, has a particularly good performance, since the resistances of the gate, source and drain electrodes are significantly reduced. It should also be noted that the transistor 200 can have a sufficiently high breakdown voltage BV as a result of being designed with a suitable thickness t1, without significant losses in terms of transconductance.

[0087] Figure 6 shows a transistor 300 according to a further embodiment of the invention. In the transistor 300, the first active area 19 of the first active region 26 is only partially silicidized.

[0088] In greater detail, the transistor 300 comprises a layer of silicide 24 extending over the drain region 15 but not over the portion of the drift region 16 closest to the gate structure. The transistor of Figure 6 provides a breakdown voltage BV, for the same thickness of the first portion 4, greater than that obtainable with the transistor 200. This is due to the fact that the silicidizing of the first active region is only partial, and therefore increases the "distance" between the surface of the gate polysilicon 11 and the more conductive area of the first active region 26, thus reducing the value of the electrical field which can be formed in the epitaxial layer 2 in the proximity of the gate oxide layer 3 on the side of the drain 16, for the same applied voltage. The increase in the breakdown voltage BV due to the partial silicidizing is possible if the doping of the drift region is not so high as to impose a value of the breakdown voltage BV which cannot be modified.

[0089] The structure of Figure 6 not only provides a high breakdown voltage, but also offers high performance (a high transconductance Gm for example), since the resistance of the layers of silicide 21, 22 and 24 is reduced in any case.

[0090] It should be noted that the considerable advantages in terms of breakdown and performance offered by partial silicidizing as shown in the solution of Figure 6 can also be obtained for LDMOS transistors which use a gate oxide layer of the conventional type, in other words one of uniform thickness.

[0091] The transistor 300 can be produced from the transistor 100 by forming a protective or shielding element 36. In particular, the shielding element 36 is formed from electrically insulating material such as an oxide, and preferably a silicon oxide.

[0092] For example, the forming of the element 36 comprises the formation of an oxide layer (not shown) over the surface of the transistor 100, the forming of a layer of photoresist positioned over this oxide layer, and the partial irradiation of this photoresist with ultraviolet rays through a suitable photomask to cause its polymerization.

[0093] Chemical etching is then carried out to remove suitable portions of the layer of photoresist and of the underlying oxide. The chemical etching forms the oxide element 36 which is positioned in such a way as to shield at least the part of the first active area 19 which is to be kept free of silicide. In particular, the precision achievable by the oxide masking process described above is such that it is possible to prevent the oxide from covering only the desired portion of the first active region 19. In this case, as shown in Figure 6, the oxide element 36 also extends over part of the surface of the gate polysilicon 11.

[0094] After the formation of the oxide element 26, the layers of silicide 21, 22 and 24 are formed in a similar way to that described above with reference to the transistor 20 (sputtering of the metal, followed by heat treatment). The oxide element 36 shields the underlying portion of the first active area 19, which is therefore not covered by the refractory metal during the sputtering. The oxide element 36 also acts as a lateral spacer.

[0095] It should be noted that the method described above for the partial silicidizing of the active area 19 for the LDMOS transistor is particularly advantageous where the LDMOS transistor 300 is integrated in the wafer 30 with CMOS devices. This is because, for conventional CMOS devices, there is a known method of using total silicidizing of the active area and of the gate polysilicon. The aforementioned method, in which the protective element 36 is used, enables the total silicidizing of the CMOS devices to be carried out simultaneously with the partial silicidizing for the LDMOS device formed in the same wafer.

[0096] Additionally, it is possible to apply in an advantageous way the process of total or partial silicidizing of active areas 19' and 20' (similar to the active areas 19 and 20) and of the polysilicon layer 11' to the P-channel LDMOS transistor 600 of Figure 8, in a similar way to that described with reference to Figures 5 and 6.

[0097] In particular, in the partial silicidizing of the active area 19', the portion of the active area 26' close to the polysilicon layer 11' is kept free of silicide, by means of a protective element similar to the element 36.

[0098] Additionally, computer simulation was used to compare the performance in terms of saturation current Ids and transconductance Gm of an N-channel LDMOS transistor similar to that of Figure 6 (in other words, having partial silicidizing) with that of a P-channel LDMOS transistor, similar to that of Figure 8, having partial silicidizing of the active area 19'.

[0099] With reference to this comparison, Figure 9 shows the variation of the gate-source voltage (Vgs) due to the simulation of the transconductance of the N-channel transistor (curve Gm-N), the transconductance of the P-channel transistor (curve Gm-P), the Ids current of the N-channel transistor (curve Ids-N), and the Ids current of the P-channel transistor (curve Ids-P). These variations were obtained for a drain-source voltage (Vds) of 5 V.

[0100] It should be noted that the threshold voltages Vt for both transistors are very similar, being approximately 0.5 V in each case. An N-channel transistor of

the type shown in Figure 6 was also constructed and tested, showing a performance closely matching that found by the simulations. In particular, a cut-off frequency of more than 20 GHz was measured. For the P-channel transistor, since the cut-off frequency is correlated with the maximum transconductance and the gate capacities, which can be considered similar to those of the N-channel transistor, the cut-off frequency for the P-channel transistor can be estimated as approximately 14-15 GHz.

[0101] Additionally, since the same parameters for the implantation of the doped regions were assumed for the simulation which was conducted, the P-channel transistor can be considered to have a breakdown voltage of 15 V, in other words a value similar to that of the N-channel transistor.

[0102] As stated above, the present invention is also applicable to conventional P-channel or N-channel MOS transistors which can be formed on the same wafer 30 or on a different wafer.

[0103] In relation to the above, in Figure 7 the number 400 indicates an example of an N-channel MOS transistor according to the present invention. The transistor 400 comprises the wafer 30, a first and a second active region 33 and 34, a gate oxide layer 32 formed over a surface 45 of the epitaxial layer 2, a layer of conductive material 35 (polysilicon or metal, for example) and two lateral spacers 36a and 36b. The first active region 33 comprises a drain region 37 which is strongly doped (N^+) and a region 38 which is weakly doped (N^-). The second active region 34 comprises a source region 39 which is strongly doped (N^+) and a region 40 which is weakly doped (N^-).

[0104] The gate oxide layer 32 has a first portion 41 having a first thickness T1 and a second portion 42 having a second thickness T2 which is different from the thickness T1. In particular, the first portion 41 is close to the first active region 33, and its thickness T1 is greater than the thickness T2.

[0105] The first portion 41 of the gate oxide 32 advantageously has a thickness such that it is possible to obtain breakdown voltages higher than those of conventional MOS transistors using a gate oxide with uniform thickness.

[0106] With reference to the transconductance Gm of the transistor 400, it should be noted that by using different thicknesses of the gate oxide the value of the breakdown voltage can be increased at a cost in terms of transconductance which is smaller than the cost incurred when the uniform thickness is increased with the thickness of the gate oxide in a conventional MOS.

[0107] Additionally, the process of silicidizing the polysilicon layer 35, a first active area 33 including the surfaces of the regions 37 and 38, and a second active area 34 including the surfaces of the regions 39 and 40 can also be applied to the transistor 400, in a similar way to that described with reference to Figures 5 and 6.

[0108] In particular, it is possible to arrange for the first active area 33 to be only partially silicidized. For example, the weakly doped region 38 can be kept free of silicide by using a protective oxide element (not shown) similar to the element 36 of Figure 6.

[0109] The method of manufacturing the transistors 100, 200, 300, and 400 is completed with the formation of suitable metallic contacts (not shown) on the corresponding drain and source regions, and on the body contact region if present.

[0110] Clearly, a person skilled in the art may further modify and vary the method and transistors according to the present invention, in order to meet contingent and specific requirements, all such modifications and variations being included within the scope of protection of the invention as defined by the following claims.

Claims

1. Metal oxide semiconductor transistor (100; 200; 300; 400; 600) integrated in a wafer of semiconductor material (30; 31) and comprising a gate structure (3, 11; 32, 35) located on one surface (10b; 45) of the said wafer and including an insulating gate layer (3; 32),

   characterized in that the said insulating gate layer (3; 32) includes a first portion (4; 41) having a first thickness (t1; T1) and a second portion (5; 42) having a second thickness (t2; T2) differing from the first thickness.

2. Transistor (100; 200; 300; 400) according to Claim 1, comprising a first active region (26; 33) including a drain region (15; 37) and a second active region (27; 34) spaced apart from the first active region and including a source region (14; 39), the said first and second active region being integrated in the wafer (30), the first portion (4; 41) of the insulating gate layer being close to the first active region, and the second portion (5; 42) being close to the second active region.

3. Transistor (100; 200; 300; 400) according to Claim 2, in which the first thickness (t1; T1) of the first portion (4; 41) is greater than the second thickness (t2; T2) of the second portion (5; 42).

4. Transistor (100; 200; 300) according to Claim 2, in which the first portion (4) and the second portion (5) of the gate insulation (3) are superimposed, respectively, on at least one part (16) of the first active region (26) and at least one part (12) of the second active region (27).

5. Transistor (100; 200; 300; 400) according to Claim 1, in which the said first thickness (t1; T1) is specified in such a way as to provide a predetermined value of the breakdown voltage of the transistor.

6. Transistor (100; 200; 300) according to Claim 1, in which the said second thickness (t2; T2) is specified in such a way as to provide a predetermined value of the transconductance of the transistor.

7. Transistor (100; 200; 300) according to Claim 1, in which the said transistor is a lateral double-diffusion MOS.

8. Transistor (400) according to Claim 1, in which the said transistor is a MOS.

9. Transistor (100; 200; 300) according to Claim 7, in which the second active region (27) comprises a body region (12) and the second portion (5) of the gate insulation (3) is superimposed on at least one part of the body region (12).

10. Transistor (100; 200; 300; 400) according to Claim 1, in which the said gate structure (3; 32) comprises a layer of electrically conductive material (11; 35) positioned on the gate oxide layer (3; 32).

11. Transistor (200; 300) according to Claim 10, in which the said layer of electrically conductive material (11) is made from polysilicon and is provided on one of its surfaces with a layer of silicide (21).

12. Transistor (200; 300) according to Claim 10, in which the said first (26) and second (27) active regions extend from the surface of the wafer (30) of semiconductor material towards the interior of the said wafer and comprise, respectively, a first (23; 24) and a second (22) silicide surface layer.

13. Transistor (300) according to Claim 12, in which the first silicide surface layer (24) only partially covers the said first active region (26).

14. Transistor (300) according to Claims 2 and 13, in which the first silicide surface layer (24) is such that it covers at least the said drain region (15) and is interrupted in such a way that a surface area of the first active region (26) close to the first portion (4) of the gate oxide is not covered with silicide.

15. Transistor (200; 300) according to Claim 12, in which the said silicide belongs to the group comprising titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$), and tungsten silicide (WSi_2).

16. A transistor (100; 200; 300; 400; 600) according to Claim 1, in which the said wafer of semiconductor material (30) comprises a substrate (1) having a first type of conductivity and an epitaxial layer (2) having a conductivity of the first type, the epitaxial layer having a conductivity lower than the conductivity of the substrate.

17. Method for manufacturing a metal oxide semiconductor field-effect transistor (100; 200; 300) integrated in a wafer (30) of semiconductor material, the said method comprising a stage of forming a layer of gate oxide (3) on one surface (10b) of the said wafer;

characterized in that the said layer of gate oxide (3) includes a first portion (4) having a first thickness (t1) and a second portion (5) having a second thickness (t2) differing from the first thickness.

18. Method according to Claim 17, in which the said stage of forming the gate oxide (3) comprises a stage of selecting the first thickness (t1) in such a way as to obtain a specified breakdown voltage of the transistor, the said first thickness being greater than the second thickness.

19. Method according to Claim 18, in which the said forming the gate oxide (3) comprises a stage of selecting the second thickness (t2) in such a way as to obtain a specified value of transconductance of the transistor, the said second thickness being smaller than the first thickness.

20. Method according to Claim 17, in which the said insulating gate layer (3) is a layer of oxide and the stage for forming the gate insulation (3) comprises the stages of:

forming a first layer of oxide (6a, 6b) on the surface of the said wafer (30), the said first layer of oxide having a thickness (t3) in the range from the second thickness to the first thickness,
a portion (6b) of the said first layer of oxide is removed to expose a region (8) of the surface of the said wafer (30),
a second layer of oxide (7) is grown on the said region (8) of the surface of the wafer (30) and on a remaining portion (6a) of the first layer of oxide positioned on the said region (8) of the surface of the wafer (30) having a thickness essentially equal to the second thickness (t2) and a further portion of the said second layer of oxide (7) being such that the total thickness of the said further portion of the second layer of oxide (7) and the said remaining layer of oxide (6a) underlying it is essentially equal to the first thickness (t1),
delimiting the said insulating gate layer (3) formed in oxide, by removing a portion of the second layer (7) of the region (8) of the surface of the wafer (30) and portions (6a) of the superimposed first layer of oxide (6) and second layer of oxide (7).

21. Method according to Claim 17, additionally com-

prising a stage of forming in the wafer (30) a first active region (26), including a drain region (15), and a second active region (27) spaced apart from the first region and including a source region (14), the first portion (4) and the second portion (5) of the gate oxide (3) being close, respectively, to the first region (26) and to the second region (27).

22. Method according to Claim 21, in which the said transistor is a lateral double-diffusion MOSFET and in which the stage of forming the first (26) and the second (27) active region comprises a stage of forming a drift region (16) and a body region (12).

23. Method according to Claim 17, in which the said transistor is a MOS transistor.

24. Method according to Claim 22, in which the said active region extends at least partially under the said second portion (5).

25. Method according to Claim 17, additionally comprising the stage of forming a layer of conductive material (11) over the said layer of gate insulation (3).

26. Method according to Claim 21, additionally comprising a stage of forming a first layer of silicide (23; 24) on at least one portion of a first surface (19) of the said first active region (26) and a second layer of silicide (22) on a second surface (20) of the said second active region (27).

27. Method according to Claim 26, in which the first silicide surface layer (24) only partially covers the said first active region (26).

28. Method according to Claim 27, in which the first silicide surface layer (24) is formed in such a way that it covers at least the said drain region (15) and is interrupted in such a way that an area of the surface of the first active region (26) close to the first portion (4) of the gate oxide is not covered with silicide.

29. Method according to Claim 27, in which the said silicide layer is produced by the method of self-aligned silicidizing.

30. Method according to Claim 28, in which the stage of forming the first silicide layer comprises the stages of:

forming a shielding element (36) on the said area of the surface of the first active region,
depositing a refractory metal on at least the said drain region (15),
applying heat treatment to the wafer (30) in such a way as to form the said first silicide layer (24).

31. Structure integrated in a wafer (30) of semiconductor material, the said structure comprising:

- at least one MOS field-effect transistor (400) including an active region (37, 38) which forms an active area (33) on a surface of the wafer, and a silicide surface layer which at least partially covers the said first active area,

characterized in that it also comprises at least one LDMOS transistor (300) including a first active region (26) which forms a first active area (19) on the surface of the wafer, and a first silicide surface layer (24) which only partially covers the said first active area.

32. Structure according to Claim 31, in which the said LDMOS field-effect transistor (300) comprises a gate structure (3, 11) and the said first active region (26) of the LDMOS transistor (300) comprises a drain region (15) and a drift region (16), the said first silicide surface layer (24) being such that it covers the drain region (15) and is interrupted in such a way that a portion of the drift region (16) close to the said gate structure (3, 11) is not covered with silicide.

33. Structure according to Claim 32, in which at least one electrically insulating element (36, 13b) is positioned on one surface of the said non-silicide-covered portion of the drift region (16).

34. Structure according to Claim 32, in which the said gate structure (3, 11) comprises a layer of conductive gate material (11) superimposed on an insulating gate layer (3) positioned on the surface of the wafer (30), and in which the said LDMOS transistor (300) comprises a second active region (27) including a body region (12) and a source region (14), each of the said conductive gate layer (11) and the said second active region (27) being covered with a corresponding layer of silicide.

35. Structure according to Claim 34, in which the said insulating gate layer (3) includes a first portion (4) having a first thickness (t1) and a second portion (5) having a second thickness (t2) differing from the first thickness.

36. Structure according to Claim 35, in which the first thickness (t1) of the first portion (4) of the gate insulation (3) is greater than the said second thickness, the said first portion being close to the drift region (16) and the said second portion being close to the body region (12).

37. Structure according to Claim 31, in which the said wafer of semiconductor material (30) comprises a substrate (1) having a first type of conductivity and an epitaxial layer (2) having a conductivity of the first type, the epitaxial layer having a conductivity which is less than the conductivity of the substrate and the said first (26) and the said second (27) active region being formed within the said epitaxial layer.

38. Method of manufacturing at least one MOS field-effect transistor (400) and at least one LDMOS field-effect transistor (300) integrated in a wafer (30) of semiconductor material, the said method comprising the stages of:

a) forming in the wafer (30) two active regions (37, 38, 39, 34) of the said at least one MOS transistor (400), the said active regions forming corresponding active areas (33, 34) on the surface of the wafer,
b) forming in the wafer (30) a first (26) and a second (27) active region of the said at least one LDMOS transistor (300), the said first and second active regions forming a first and a second active area (19; 20) on a surface of the wafer,
c) forming a layer of silicide on at least one portion of each of the two active areas (33, 34) of the said at least one MOS transistor (600),
d) forming a first (24) and a second (22) layer of silicide on the said first (19) and second (20) active area of the at least one LDMOS transistor (300), the said first layer of silicide (24) only partially covering the first active area (19).

39. Method according to Claim 38, additionally comprising the stages of:

- forming on the wafer (30) a gate structure (3, 11) of the said at least one LDMOS transistor (300), the said gate structure including an insulating gate layer and a layer of conductive gate material (11) ;
- forming a further layer of silicide (21) on a surface of the layer of insulating gate material (11).

40. Method according to Claim 39, in which the said first active region (26) comprises a drain region (15) and a drift region (16), and the said second active region comprises a body region (12) and a source region (14), the said stage d) comprising a stage of:

e) forming the first layer of silicide (24) in such a way that it covers the drain region (15) and in such a way that a portion of the drift region (16) close to the said gate structure (3, 11) is not silicidized.

41. Method according to Claim 40, in which the said stage e) comprises the stages of:

- shielding the said portion of the drift region (16) by means of a protective element (36) located at least on the said portion,
- depositing a layer of refractory metal on the first active area (19), on the second active area (20) and on the shielding element (36),
- carrying out a heat treatment of the wafer (30) in such a way that the layer of refractory metal reacts with portions of the first and second active area on which it is deposited to form silicide.

42. Method according to Claim 41, in which the said stage of shielding the portion of the drift region (16) comprises the stages of forming a layer of protective material on the wafer (30) and delimiting the said protective element (36) by stages of masking and etching the layer of protective material.

43. Method according to Claim 40, in which the gate structure (3, 11) of the at least one LDMOS transistor (300) comprises an insulating gate layer (3) positioned on the wafer (30) and including a first portion (4) having a first thickness (t1) and a second portion (5) having a second thickness (t2) which is less than the first thickness, the said first portion being close to the drift region (16).

44. Method according to Claim 40, in which the said stage of forming the gate structure (3, 11) includes the stages of:

- forming at least one oxide layer (7, 6a) on the surface of the said wafer (30), a portion of the said oxide layer being designed to form the insulating gate layer (3);
- forming a layer of polysilicon (500) on a surface of the said oxide layer (7, 6a), a portion of the said layer of polysilicon being designed to form the layer of conductive gate material (11),
- forming a first masking layer (501) over the said layer of polysilicon to allow a first stage of etching to be carried out in such a way as to form at least a first lateral wall (W-S) of the said layer of conductive gate material (11) and a first aperture in the layer of polysilicon,
- removing the first masking layer and forming a second masking layer (502) over the said layer of polysilicon (500) to allow a second stage of etching to be carried out in such a way as to form at least a second lateral wall (W-D) of the said layer of conductive gate material (11) and a second aperture in the layer of polysilicon.

45. Method according to Claim 44, additionally com-

prising the stages of:

- stages of inclined ion implantation (F1; F2) through the first aperture of the said first mask (501) and through the second aperture of the said second mask to form the body region (12) and the drift region (16), the said inclined ion implantation enabling the body regions (12) and the drift regions (16) to be extended into the wafer (30) at least partially under the gate structure (3, 11) .

46. Method according to Claim 45, in which, after the ion implantation stage, a heat treatment is applied to the wafer (30) to permit a further diffusion and activation of the drift (16) and body (12) regions.

47. Method according to Claim 46, in which the said heat treatment is applied at a temperature of less than 1000° C.

48. Method according to Claim 47, in which the said first (501) and second (502) masking layer are formed from photoresist and by irradiation with electromagnetic waves through a corresponding photomask.

49. Method according to Claim 38, in which the said at least one LDMOS transistor comprises an N-channel LDMOS transistor (300) and a P-channel LDMOS transistor (600).

50. Method according to Claims 48 and 49, in which the said N-channel transistor (300) and P-channel transistor (600) are both produced by ion implantation in the wafer (30) through the apertures in the said first masking layer (501) and in the said second masking layer (502).

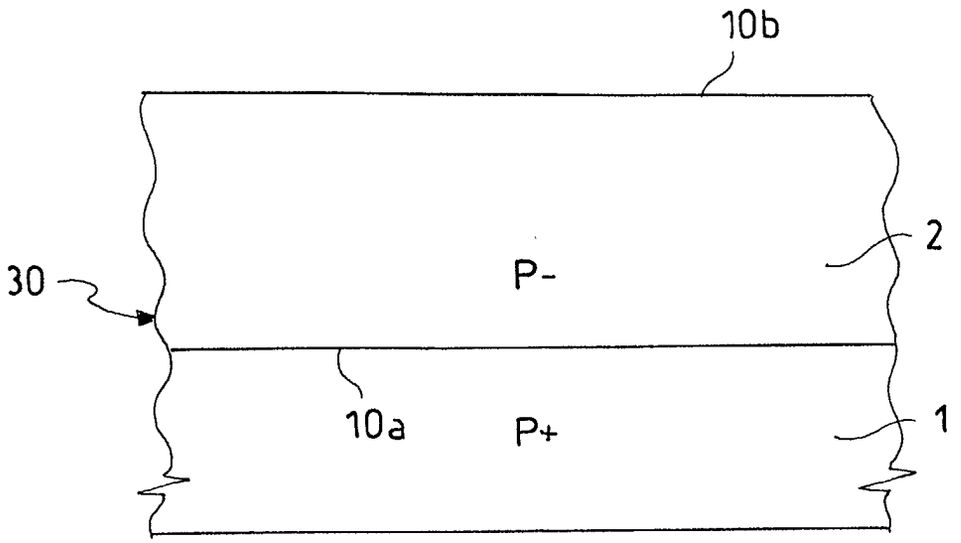

FIG.1a

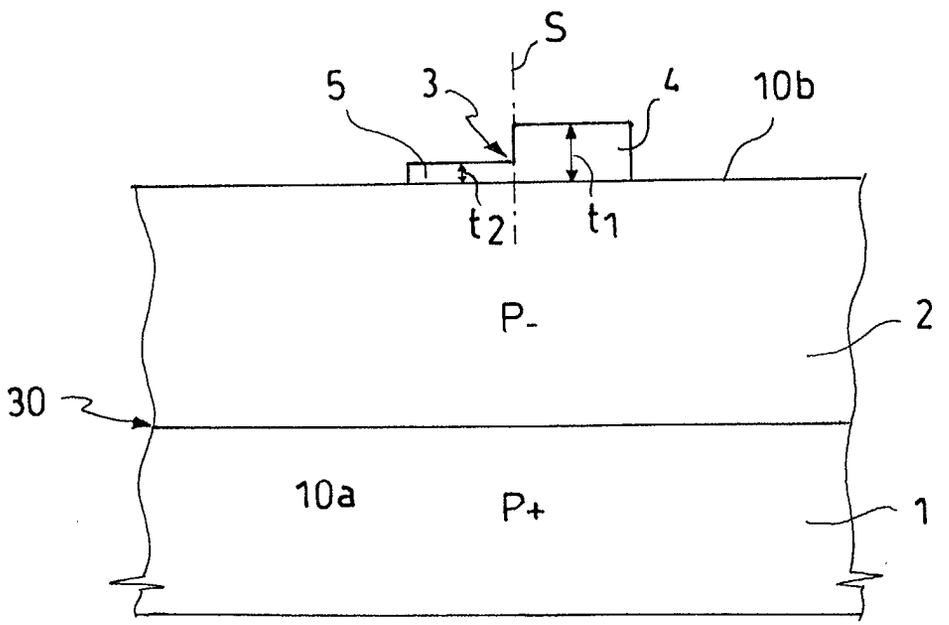

FIG.1b

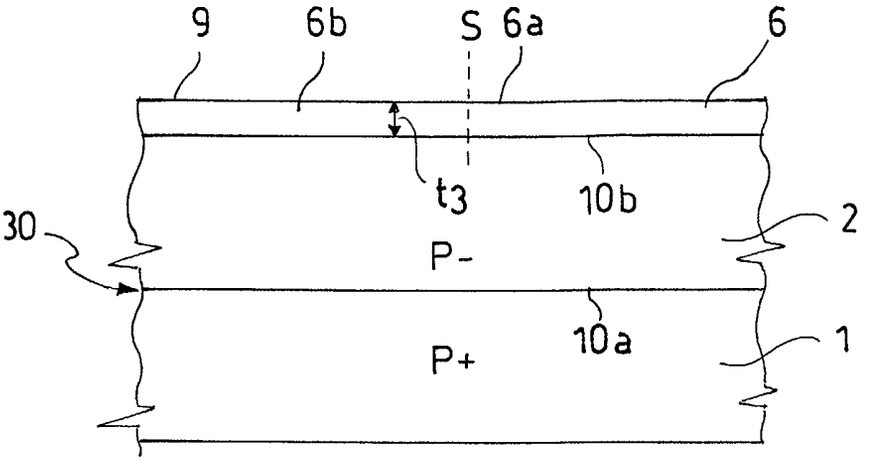

FIG.2a

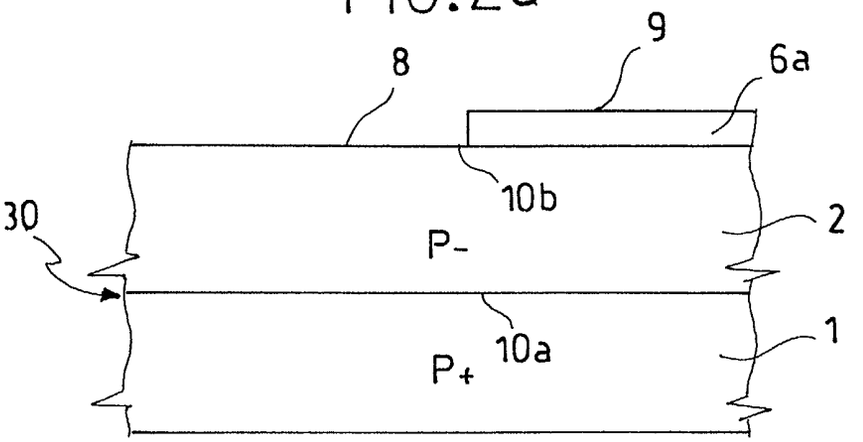

FIG.2b

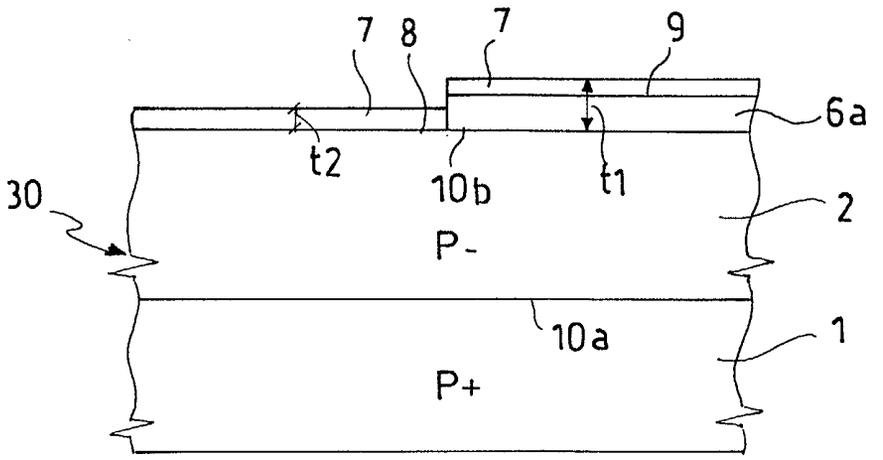

FIG.2c

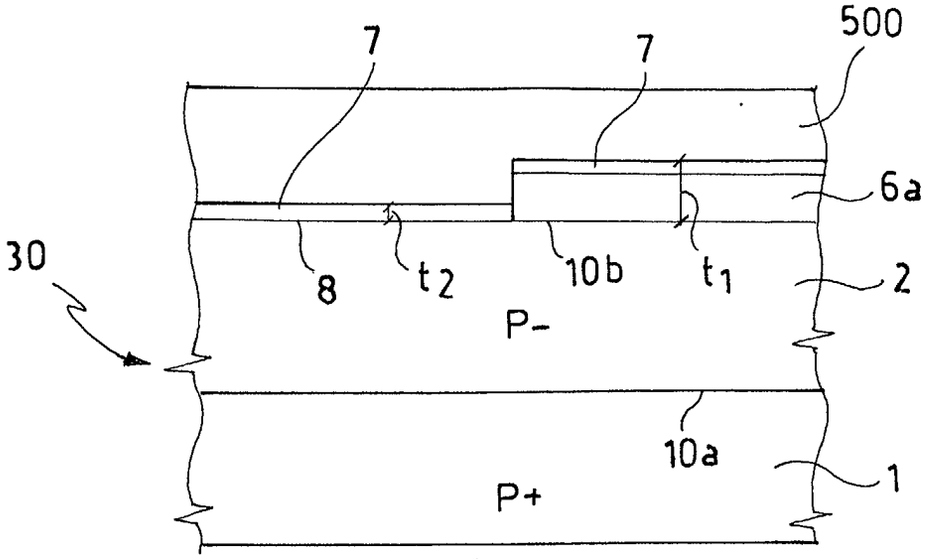
7
7
500
6a
30
8
t2
10b
t1
2
P-
10a
1
P+

FIG. 2d

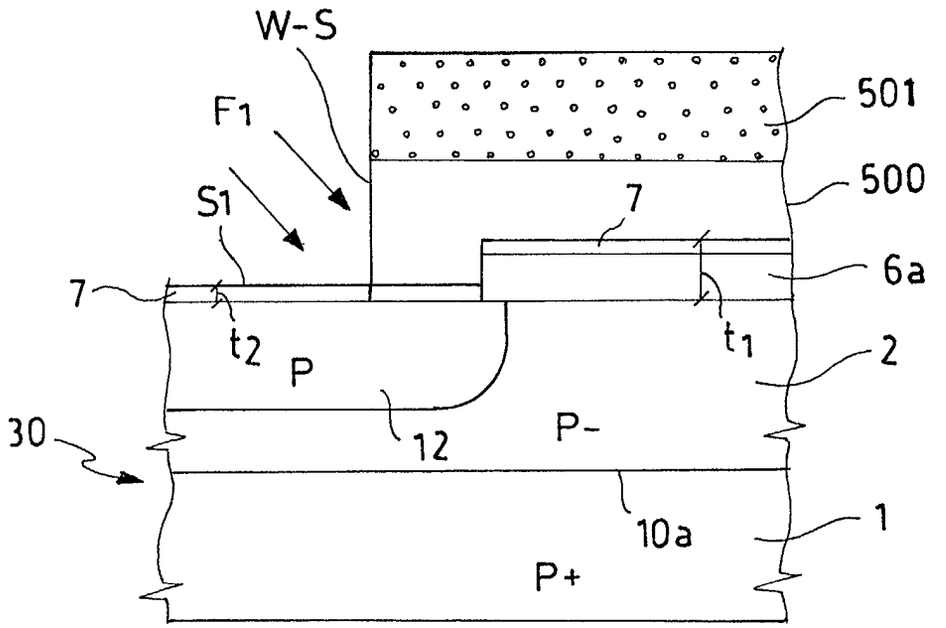
W-S
501
F1
500
S1
7
6a
7
t2
t1
P
2
30
12
P-
10a
1
P+

FIG. 2e

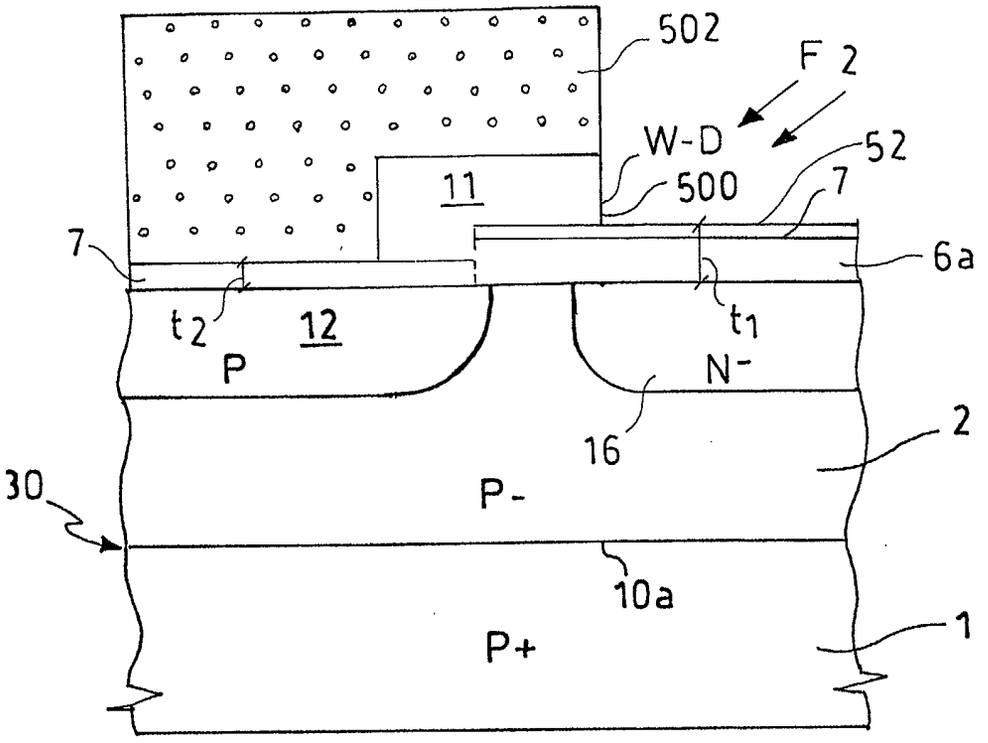
502
F 2
W-D
52
11
500
7
7
6a
t2
12
t1
P
N-
16
2
30
P-
10a
1
P+

FIG.3a

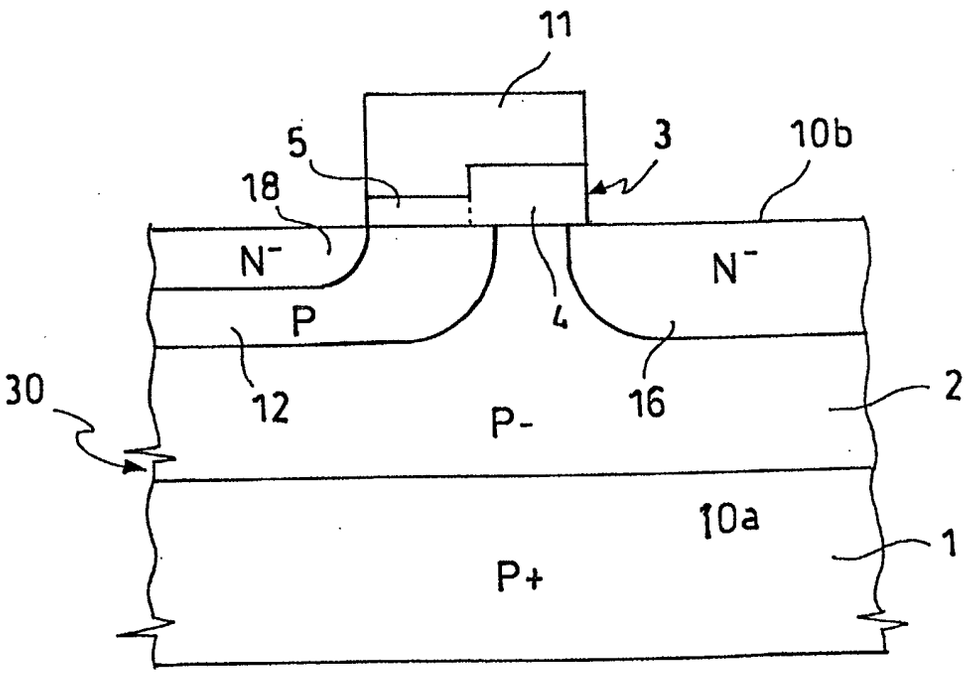
11
5
3
10b
18
N-
N-
P
4
30
12
16
2
P-
10a
1
P+

FIG.3b

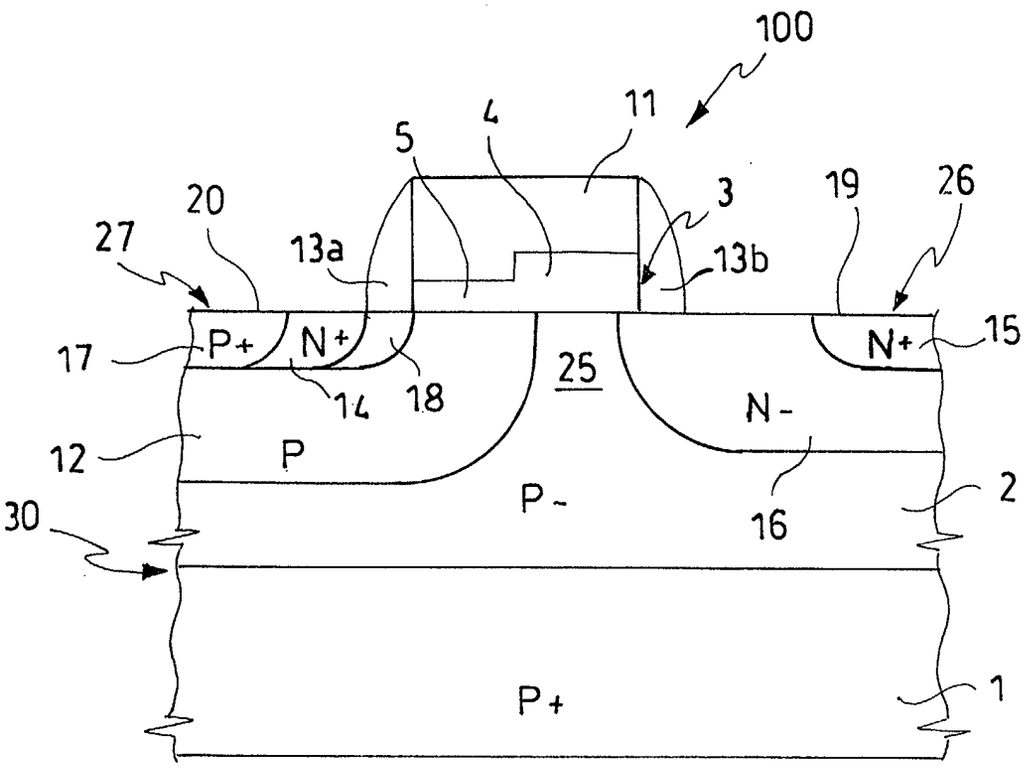
100
11
4
5
3
20
19
26
27
13a
13b
P+
N+
N+
15
17
25
14
18
N-
12
P
P-
2
30
16
P+
1

FIG.4

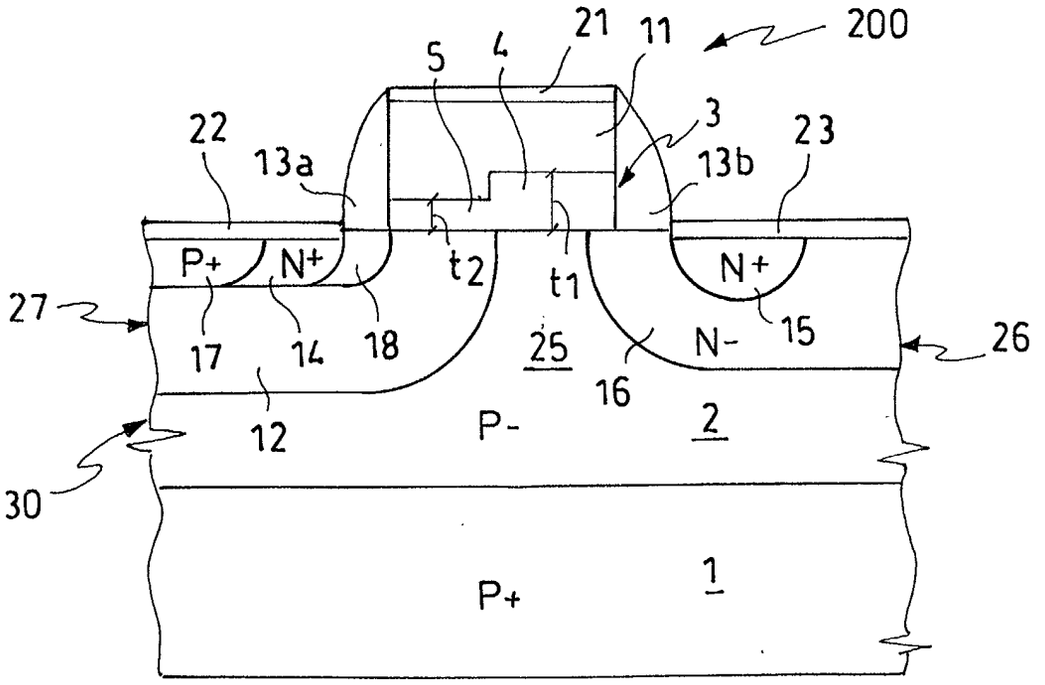
200
21
11
5
4
3
22
23
13a
13b
P+
N+
N+
t2
t1
27
17
14
18
25
N-
15
26
16
12
P-
2
30
P+
1

FIG.5

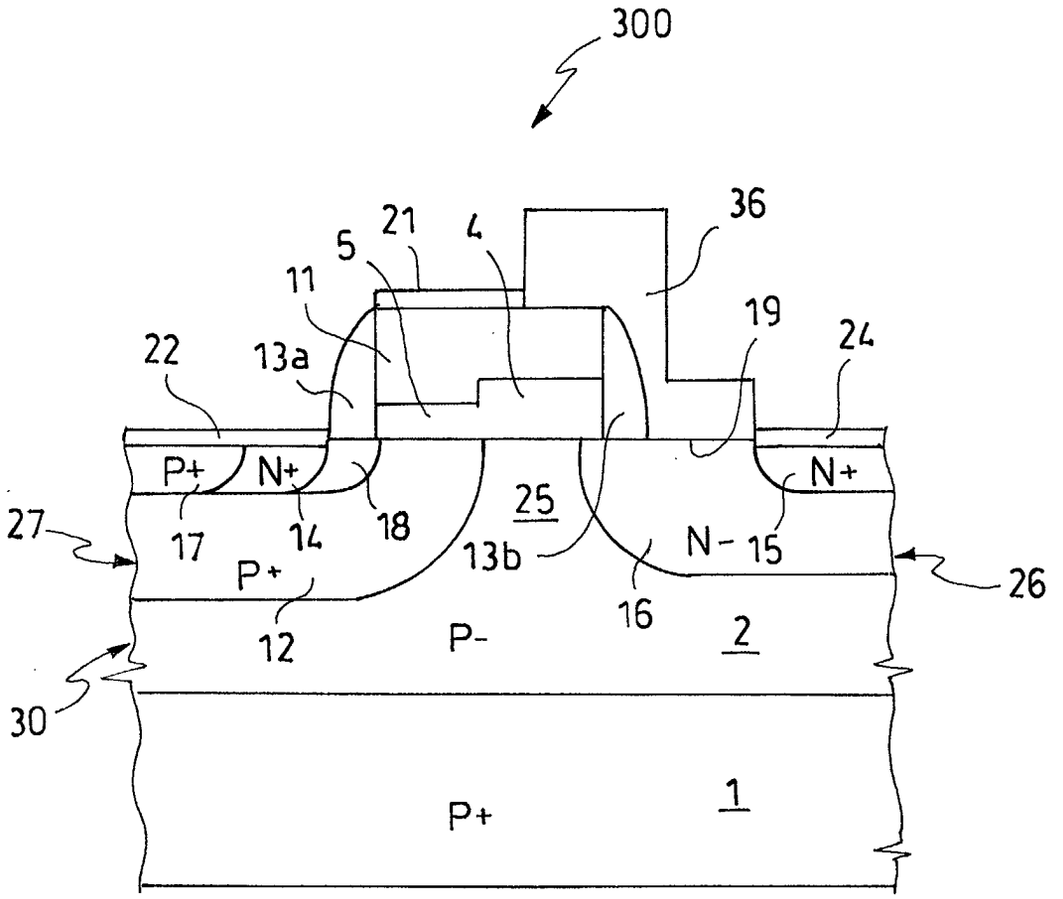
300
36
21
5
4
11
19
24
22
13a
P+
N+
N+
25
27
17
14
18
13b
N- 15
26
P+
16
12
P-
2
30
P+
1

FIG. 6

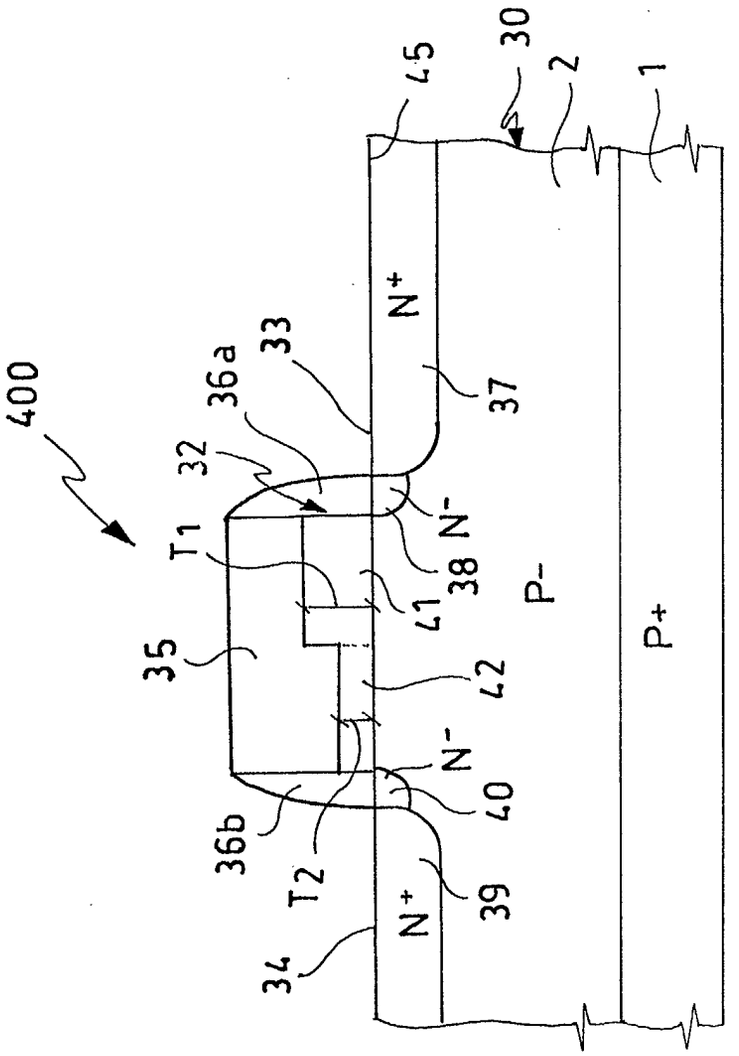

FIG. 7

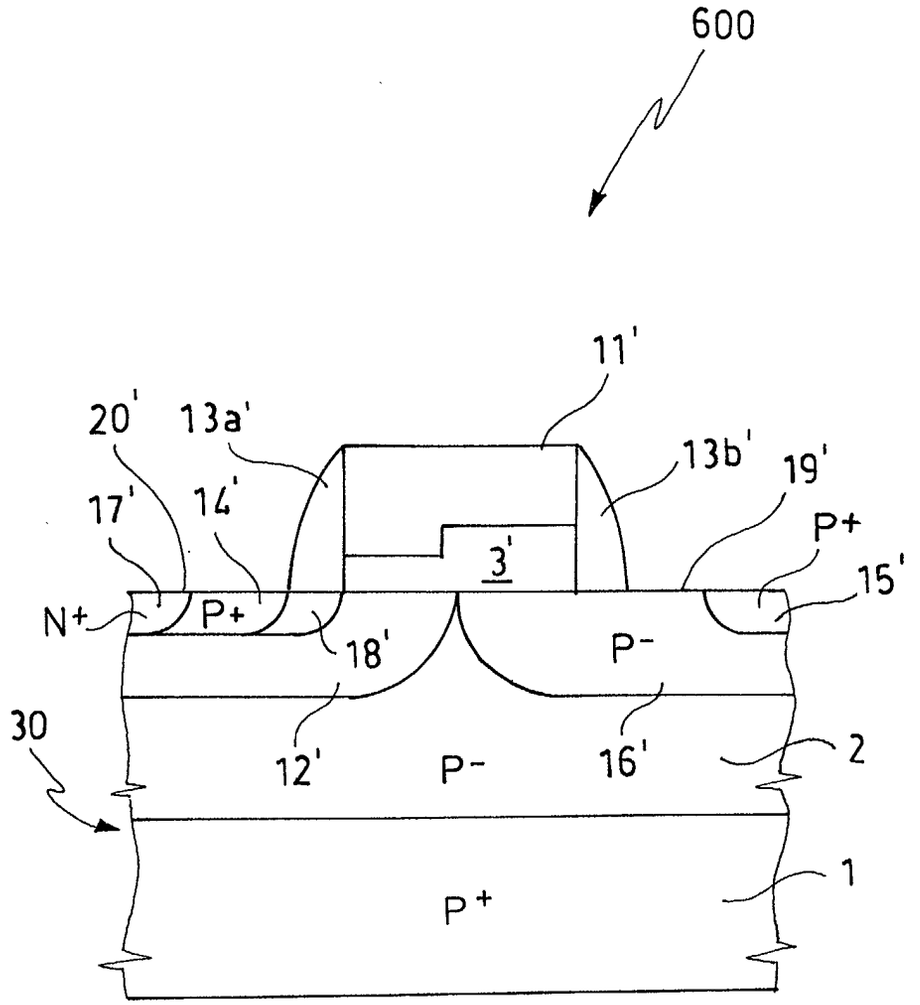

FIG. 8

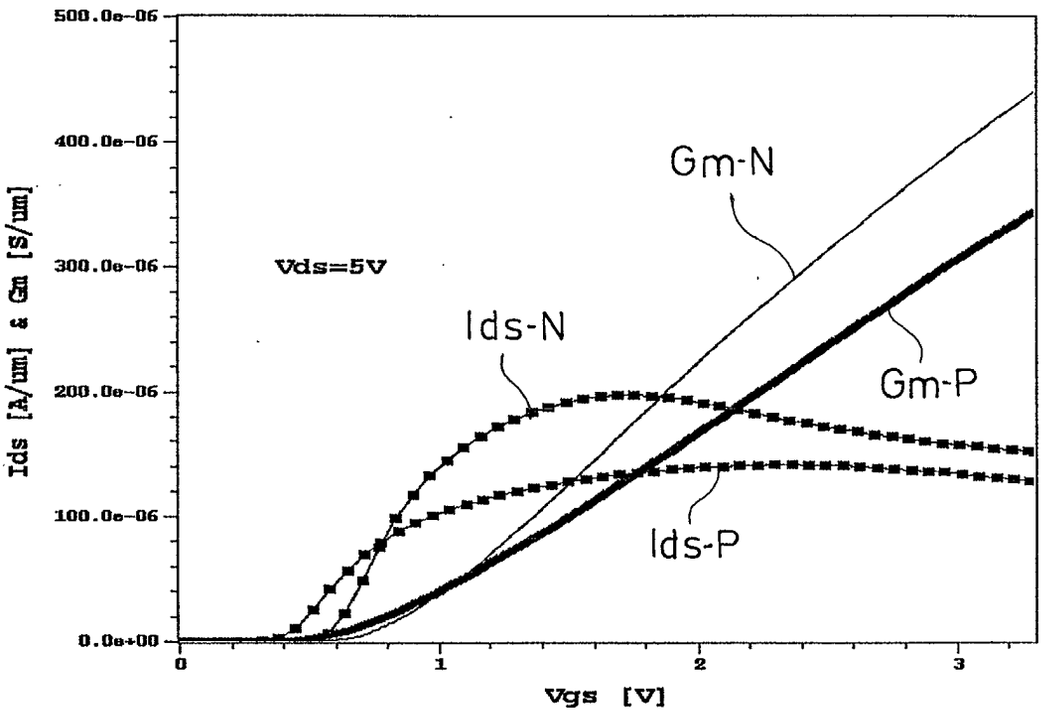
500.0e-06
400.0e-06
300.0e-06
200.0e-06
100.0e-06
0.0e+00
Ids [A/um] & Gm [S/um]
Vds=5V
Gm-N
Ids-N
Gm-P
Ids-P
0
1
2
3
Vgs [V]

FIG. 9

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EUROPEAN SEARCH REPORT

Application Number
EP 01 83 0786

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 February 2003	Nesso, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 February 2003	Nesso, S

CATEGORY OF CITED DOCUMENTS

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
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The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-30

   MOS transistor having an insulating gate with a non-uniform thickness and method of manufacturing the same.

2. Claims: 31-50

   Structure including one MOS transistor having an active area only partially covered by a silicide layer, one LDMOS transistor having an active area only partially covered by a silicide layer and method of manufacturing such structure.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 83 0786

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