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(54) **METHOD OF FABRICATING A SELF-ALIGNED BIPOLAR JUNCTION TRANSISTOR IN SILICON CARBIDE AND RESULTING DEVICES**

VERFAHREN ZUR HERSTELLUNG EINES SELBSTJUSTIERTEN SILIZIUMKARBID-BIPOLARTRANSISTORS UND ERHALTENE PRODUKTE

PROCEDE DE FABRICATION D'UN TRANSISTOR AUTOALIGNE A JONCTION BIPOLAIRE EN CARBURE DE SILICIUM ET DISPOSITIFS CORRESPONDANTS

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WO-A-00/74129 **WO-A-91/07778**
US-A- 4 945 394 **US-A- 5 424 227**

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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a method of fabricating a bipolar junction transistor in silicon carbide, and in particular relates to a method of fabricating a bipolar junction transistor in silicon carbide wherein the base and emitter contacts are self-aligned, and devices resulting therefrom.

2. Description of the Related Art

[0002] The bipolar junction transistor (BJT) is a well-known and frequently used semiconductor electronic device. A bipolar junction transistor is generally defined as a device formed of a semiconductor material having two opposing p-n junctions in close proximity to one another. Because of their respective structures and conductivity types, bipolar junction transistors are generally referred to as n-p-n or p-n-p transistors.

[0003] In the operation of an n-p-n BJT, current carriers enters a region of the semiconductor material adjacent one of the p-n junctions which is called the emitter. Most of the charge carriers exit the device from a region of the semiconductor material adjacent the other p-n junction which is called the collector. The collector and emitter have the same conductivity type, either p or n. A small portion of semiconductor material known as the base, having the opposite conductivity type (either p or n) from the collector and the emitter, is positioned between the collector and the emitter. The BJT's two p-n junctions are formed where the collector meets the base and where the base meets the emitter.

[0004] When current is injected into or extracted from the base, depending upon whether the BJT is n-p-n or p-n-p, the flow of charge carriers (i.e. electrons or holes) which can move from the collector to the emitter is greatly affected. Typically, small currents applied to the base can control proportionally larger currents passing through the BJT, giving it its usefulness as a component of electronic circuits. The structure and operation of BJTs are described in detail in B. Streetman, SOLID STATE ELECTRONIC DEVICES, 2d ed. (1980), chapter 7.

[0005] One of the requirements for an operable and useful bipolar junction transistor is an appropriate semiconductor material from which it can be formed. The most commonly used semiconductor material is silicon (Si), although attention has been given to other semiconductor materials such as gallium arsenide (GaAs) and indium phosphide (InP). For given circumstances and operations, these materials all have appropriate applications.

[0006] Another candidate material for bipolar junction transistors is silicon carbide (SiC). Silicon carbide has well-known advantageous semiconductor characteristics: a wide bandgap, a high electric field breakdown strength, a reasonably high electron mobility, a high thermal conductivity, a high melting point, and a high saturated electron drift velocity. Taken together, these qualities mean that, as compared to devices formed in other semiconductor materials, electronic devices formed in silicon carbide have the capability of operating at higher temperatures, at high power densities, at high speeds, at high power levels and even under high radiation densities.

[0007] Due to their ability to function at high frequencies, high temperatures, and high power levels, silicon carbide transistors are highly desirable for use in applications such as high power radio frequency transmitters for radar and communications, for high power switching applications, and for high temperature operations such as jet engine control. Accordingly, methods of producing device quality silicon carbide and devices formed from silicon carbide have been of interest to scientists and engineers for several decades.

[0008] Silicon carbide crystallizes in over 150 different polytypes, or crystal structures, of which the most common are designated 3C, 4H and 6H where "C" stands for "cubic" and "H" for "hexagonal." At the present time, the 6H polytype is the most thoroughly characterized, but the 4H polytype is more attractive for power devices because of its higher electron mobility.

[0009] At present time, silicon carbide is a difficult material to fabricate devices with. Silicon carbide's high melting point renders techniques such as alloying and diffusion of dopants more difficult, usually because a number of the other materials necessary to perform such operations tend to break down at the high temperatures required to affect silicon carbide. Silicon carbide is also an extremely hard material, and indeed its most common use is as an abrasive.

[0010] Attempts have been made with some success in manufacturing junctions, diodes, transistors and other devices from silicon carbide. One example of a bipolar junction transistor is disclosed in Palmour et al., U.S. Patent No. 4,945,394. Palmour et al. disclose a bipolar junction transistor formed in silicon carbide wherein the base and emitter are formed as wells using high temperature ion implantation. However, since the emitter and base regions are formed using photolithographic techniques, the precision with which the base and emitter regions may be spaced is limited; typically the spacing must be about 1-5 μm or more using conventional lithographic techniques (with about 2μm being most typical), which may result in undesirably high base resistance, and also in unwanted base-collector capacitance, both of which reduce the ability of the device to operate at high frequencies. Moreover, since bipolar devices in silicon carbide exhibit relatively short minority carrier lifetimes, typically 40 nsec-3μsec, it is imperative that the physical dimensions of such devices be tightly controlled.

[0011] Self alignment techniques, i.e. manufacturing techniques through which device features automatically

and inherently align as a result of the manufacturing process, have been used to produce silicon carbide MOSFETs. For example, US Patent No. 5,726,463, discloses a silicon carbide MOSFET having a self-aligned gate structure in which self-alignment of the gate contacts is achieved by filling steep-walled grooves with conductive gate material over a thin oxide layer, and applying contacts to the gate material through windows opened in a dielectric layer. Such techniques are designed to reduce stray capacitance by reducing the overlap of the gate contacts with the drain and source regions, and are thus not applicable to the fabrication of bipolar junction transistors.

[0012] Accordingly, there is a need in the art for a method of fabricating a bipolar junction transistor in silicon carbide which enables precise and close spacing of the base and emitter contacts.

[0013] PCT patent application, publication number WO00/74129 discloses the manufacture of a low voltage high frequency silicon power transistor epitaxial mesa structure using a minimized number of masks.

[0014] PCT patent application, publication number WO91/07778 discloses a bipolar junction transistor comprises a substrate, a lightly doped base region on the substrate, a heavily doped base contact region around the lightly doped base region, and an emitter positioned above the lightly doped base region. By etching away the peripheral portion of the emitter a portion of the periphery of the lightly doped base region, a planar junction is created between emitter and base.

[0015] US-5,424,227 describes a semiconductor array of integrated silicon-germanium heterobipolar transistors.

OBJECTS AND SUMMARY OF THE INVENTION

[0016] It is an object of the present invention to enable precise and close spacing of the base and emitter contacts in a bipolar junction transistor formed in silicon carbide.

[0017] It is a further object of the present invention to simplify the process of fabricating a bipolar junction transistor in silicon carbide.

[0018] A still further object of the invention is to reduce the number of photolithographic steps required to fabricate a bipolar junction transistor in silicon carbide.

[0019] According to the present invention, the foregoing and other objects are attained by a method of fabricating a self-aligned bipolar junction transistor in accordance with claim 1.

[0020] In another aspect, the invention includes a bipolar junction transistor in accordance with claim 8.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

FIG. 1 depicts, in cross section, a semiconductor structure comprising a silicon carbide substrate having a plurality of epitaxial layers deposited thereon.

FIG.2 is a cross section of the semiconductor structure depicted in FIG.1 on which a layer of oxide has been deposited.

FIG.3 is a cross section of the semiconductor structure depicted in FIG. 2 which has been etched to form a series of pillars.

FIG. 3A is a plan view of a semiconductor structure fabricated in accordance with the present invention.

FIG. 4 is a cross section of the semiconductor structure depicted in FIG. 3 on which a second layer of oxide has been deposited.

FIG. 5 depicts the semiconductor structure shown in FIG. 4 after an anisotropic etch has removed the horizontal oxide surfaces, and well regions have been implanted.

FIG. 6 depicts the semiconductor structure shown in FIG. 5 following removal of the remaining oxide surfaces and isolation of the mesa in which a bipolar junction transistor is fabricated.

FIG.7 is a cross section of the structure depicted in FIG. 6 following JTE implantation.

FIG. 8 depicts the structure shown in FIG. 7 after deposition of another oxide layer.

FIG. 9 depicts the structure shown in FIG. 8 after removal of the horizontal oxide surfaces with an anisotropic etch.

FIG. 10 is a cross section of a completed device including ohmic contacts to the collector, emitter and base regions of the transistor.

FIG. 11 is a cross section of a second semiconductor structure not in accordance with the present invention comprising a silicon carbide substrate having a plurality of epitaxial layers deposited thereon.

FIG. 12 depicts the semiconductor structure shown in FIG. 11 following formation of pillars and implantation of well regions.

FIG. 13 is a cross section of a completed device formed using the structure depicted in FIG. 11.

FIG. 14 depicts an embodiment of the present invention wherein the substrate is semi-insulating.

FIG. 15 depicts an embodiment not in accordance with the present invention wherein the substrate is semi-insulating.

DETAILED DESCRIPTION

[0022] The present invention is directed to a method of fabricating a bipolar junction transistor in silicon carbide. As discussed above, silicon carbide is a difficult material to work with because of its high melting point and the difficulty of growing large, device quality single crystals. However, the characteristics of silicon carbide (i.e. wide bandgap, high thermal conductivity, high melting point, high electric field breakdown strength, low dielectric constant, and high saturated electron drift velocity) make it an ideal material for fabricating electronic

devices for use in high-temperature, high frequency applications in products ranging from cellular base stations to jet aircraft engines.

[0023] As discussed above, a bipolar junction transistor (BJT) is an active, three terminal semiconductor device comprising two p-n junctions in close proximity. BJTs are broadly characterized as n-p-n or p-n-p depending on the conductivity types of their respective bases, collectors and emitters. For simplicity, only the manufacture of an n-p-n BJT will be described in detail. However, it will be immediately realized by those having skill in the art that the same method could be used to manufacture a p-n-p transistor by reversing the described conductivity types.

[0024] The method of the present invention introduces a novel self-alignment technique for aligning the base and emitter contacts of a bipolar junction transistor formed in silicon carbide. The method of the present invention may be implemented using as a starting structure a silicon carbide substrate on which there is deposited one or more epitaxial layers of silicon carbide. Epitaxial layers of silicon carbide may be applied as described in U.S. Patents No. 5,011,549 and 4,912,064 to Kong, et al.

[0025] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. As will also be appreciated by those having skill in the art, while the present invention is described with respect to layers, such layers may be formed epitaxially, by ion implantation, or by other suitable means. The present invention is not limited to the relative size and spacing illustrated in the accompanying figures.

[0026] Accordingly, FIG.1 depicts a semiconductor structure 1 comprising a heavily doped silicon carbide substrate 2 (with conductivity designated as n+). Although substrate 2 may be formed from any of a number of different silicon carbide polytypes (i.e. crystal structures), substrate 2 preferably comprises a single crystal 4H alpha-SiC material (Si-face). To obtain n-type material, substrate 2 may be doped during the growth phase with a donor dopant such as nitrogen.

[0027] A first epitaxial layer 4 having the same conductivity type as substrate 2 is disposed on substrate 2. Layer 4 is doped with a donor dopant such as nitrogen at a concentration of between about 1E14 cm^{-3} and 1E16 cm^{-3}. Preferably, doping is performed during the epitaxial growth process. Layer 4 has a thickness of approximately 3μm to approximately 200μm, and most preferably from about 6μm to about 20μm. Together, substrate 2 and layer 4 form the collector region of the transistor under fabrication.

[0028] A second epitaxial layer 6 having a conductivity type opposite that of substrate 2 and layer 4 is formed on layer 4. Layer 6 is doped with an acceptor dopant such as boron or aluminum at a concentration of about 5E17 to 5E18 cm^{-3}. Layer 6 has a thickness of approximately 0.3μm to approximately 5μm, and most preferably from about 0.7μm to about 1μm. Finally, epitaxial layer 8, having a conductivity type the same as layer 6, is formed on layer 6. Layer 8 is a heavily doped layer having a thickness of approximately 0.05μm to approximately 2μm, and most preferably from about 0.2μm to about 0.5μm. Layer 8 is doped with an acceptor dopant such as boron or aluminum at a concentration above 1E18 cm^{-3} and preferably of about 1E20 cm^{-3} to 1E21 cm^{-3}. Layers 6 and 8 form the base region of the transistor under fabrication.

[0029] As used herein, the descriptive phrase "opposite conductivity type" merely refers to whether a given region of semiconductor material demonstrates opposite n-type or p-type conductivity in comparison with another region of material, without regard to the doping concentration of either sample of material. Thus, for example, n+ material and p-type material have opposite conductivity types, while p+ material and p-type material are considered to have the same conductivity types, albeit with different doping concentrations.

[0030] Referring to FIG. 2, an oxide layer 10, preferably silicon dioxide, is formed on the exposed surface of layer 8, preferably using the Plasma Enhanced Chemical Vapor Deposition (PECVD) process. The PECVD process is described in Chapter 6 of S.M. Sze, VLSI TECHNOLOGY, 2nd Ed., McGraw-Hill 1988. Methods of forming high quality silicon dioxide layers on silicon carbide are described in U.S. Patent No. 5,459,107.

[0031] Oxide layer 10 preferably has a thickness between 0.2 and 3μm, and most preferably has a thickness between 0.6 and 1.5μm.

[0032] Next, oxide layer 10 is patterned using an etch mask in accordance with conventional photolithographic techniques, and portions of the oxide layer 10 and layer 8 are etched away to form pillars 12, shown in cross section in FIG. 3. Each pillar 12 comprises a raised portion 16 formed from layer 8 and a cap portion 13 formed from oxide layer 10. The etching process is stopped once layer 8 is etched completely down to the surface 6B of layer 6 (thereby exposing the surface 6B of layer 6). Pillars 12 define trenches 14 having bottom walls 14B along the surface 6B of layer 6 and side walls 14A. Raised portions 16 will ultimately define the base region in the completed BJT device.

[0033] FIG 3A is a top view of one embodiment of the structure shown in FIG. 3. As is apparent from FIG. 3A,

pillars 12 actually may have a linear structure. Other configurations, such as circular configurations, are possible and will be appreciated by those having skill in the art as being within the scope of the present invention.

[0034] Referring now to FIG. 4, an oxide spacer layer 18 is formed across the top surface of structure 1 including side walls 14A of trenches 14, preferably using the PECVD process. Oxide spacer layer 18 preferably has a thickness of between about 0.05 μm and 0.5 μm, and most preferably has a thickness of about 0.1-0.25μm. As will be apparent from the discussion below, the thickness of oxide spacer layer 18 will determine the spacing of the base and collector contacts of the bipolar junction transistor manufactured according to the present invention. The thickness of oxide spacer layer 18 is determined by the amount of time the layer is deposited. Typical deposition rates vary from machine to machine. In general, however, the thickness of oxide spacer layer 18 may be carefully controlled to within +/- 0.1 μm. The thickness of the layer as deposited may be confirmed through measurement with an ellipsometer.

[0035] Oxide spacer layer 18 includes portions 18C disposed on an exposed surface of pillars 12 substantially parallel to the exposed surface 6B of layer 6, portions 18A disposed on the side walls of pillars 12, and portions 18B disposed on the exposed surface 6B of layer 6, including bottom walls 14B of trenches 14.

[0036] Although layer 18 is described in reference to the preferred embodiments as an oxide layer, it will be understood that layer 18 may be formed of any material that is may be controllably deposited on a layer of silicon carbide and which is suitably susceptible to anisotropic etching such that it will permit the alignment and formation of adjacent well regions as described more fully hereinafter.

[0037] As illustrated in FIG. 5, an anisotropic etch is next performed to remove portions of the oxide spacer layer 18. As is familiar to those skilled in the art, an anisotropic process is one which affects a material along certain axes or planes and not others. Thus, an anisotropic etch may remove material along one surface more efficiently than another surface. For example, as illustrated in FIG. 5, an anisotropic etch may remove material from a horizontal surface and not a vertical surface of a structure.

[0038] As seen in FIG. 5, following the anisotropic etch, the horizontal portions 18B and 18C of the oxide spacer layer 18 have been removed to expose layers 10C of the pillars 12 and the surface 6B of layer 6 including bottom walls 14B of trenches 14, while the vertical portions 18A of the oxide spacer layer 18 disposed on the side walls of pillars 12 remain substantially intact.

[0039] Next, heavily doped well regions 20 of n-type conductivity, which will ultimately form the emitter in the completed device, are formed in layer 6. Such well regions may be formed using high temperature ion implantation techniques described in U.S. Patents No. 4,945,394 and 5,087,576. Ion implantation is typically necessary because thermal diffusion coefficients in silicon carbide are too small for diffusion of impurities to be practical. Using ion implantation, silicon carbide can be implanted with impurities to a concentration of 1E18 to 1E21 cm^{-3}. In preferred embodiments, the implantation is conducted with the wafer at an elevated temperature, and the implants are activated at 1200 to 1700C in a suitable ambient.

[0040] Well regions 20 extend preferably between about 0.25 μm and 1 μm deep into layer 6, and are most preferably about 0.3-0.6 μm deep. In the embodiment illustrated in FIG. 5, well regions 20 do not extend all the way through layer 6 into layer 4. Well regions 20 preferably have a doping density from about 1E18 cm^{-3} to about 1E21 cm^{-3}, with a range of 1E20 - 1E21 cm^{-3} being most preferable.

[0041] Because the side wall portions 18A of the oxide spacer layer 18 are present during creation of the well regions 20, the edges 20A of well regions 20 are spaced from the side walls 16A of raised portions 16 by a distance equal to the thickness of the oxide spacer layer 18. Thus, the spacing of the base contacts and the emitter contacts is determined by oxide thickness, and not by lithography, permitting much closer alignment of the base and emitter contacts. Spacing of 0.1-0.25 μm can be achieved using the method of the present invention, whereas a spacing of at least 1 μm is required using conventional lithography techniques. The improved spacing achieved with the method of the present invention reduces base resistance and base collector capacitance, and enables the production of devices which operate at higher frequencies.

[0042] Referring now to FIG. 6, the remaining oxide layers 18A and 10 are stripped using conventional wet etching techniques. Next, the periphery of layer 6 is etched away by reactive ion etching to form a mesa 24 comprising layer 6, well regions 20, and raised portions 16. Mesa isolation is performed in order to isolate the base-collector junction and to isolate devices fabricated on the same substrate.

[0043] Following these steps, peripheral surface 4C of layer 4 is exposed. As illustrated in FIG. 7, junction termination extension (JTE) implantation is next performed to create p-type regions 22 beneath the exposed peripheral surface 4C of layer 4. The p-type regions 22 serve to spread the depletion region of the transistor in a controlled manner.

[0044] The entire structure 1 is then annealed to activate implanted dopant atoms. The anneal temperature is preferably between about 1200C and 1800C. The device may be annealed for a time period ranging from one minute to eighteen hours, and preferably from three minutes to fourteen minutes.

[0045] Having described the fabrication of the basic structure of a bipolar junction transistor, formation of ohmic contacts on the device will now be described with reference to FIGs 8-10. First, a PECVD oxide layer 26 is formed along the top surface of the structure 1 (FIG. 8) followed by an anisotropic etch to remove the horizontal

portions 26C of the oxide layer 26 from mesa 24, but not from peripheral surface 4C (FIG. 9). Following the anisotropic etch, surfaces 14C of raised portions 14 are exposed, as are surfaces 14B of well regions 20. Finally, emitter contacts 28 are applied to the surfaces 14B of well regions 20 and base contacts 30 are applied to the surfaces 14C of raised portions 14.

[0046] A number of metals and metal composites are appropriate for these ohmic contacts. For example, nickel or nickel-titanium combinations are appropriate ohmic contacts to n-type silicon carbide while aluminum or aluminum-titanium combinations are useful ohmic contacts to p-type silicon carbide. In addition, cobalt silicide ($CoSi_2$) has shown promise as an ohmic contact material to p-type silicon carbide. Appropriate ohmic contact structures are described in U.S. Patents No. 5,323,022 and 5,409,859. The contacts 28, 30, 32 are high temperature annealed in a conventional manner to create ohmic contacts, and a wet etch is performed to remove unreacted metal.

[0047] Since the substrate 2 in the embodiment illustrated in FIGs 1-10 is conductive, a collector contact 32 is applied to the bottom surface of substrate 2. However, it will be readily understood by those skilled in the art that the present invention could be implemented using a nonconducting substrate such as semi-insulating silicon carbide or sapphire (Al_2O_3), in which case the collector contact 32 would not be applied to the bottom surface of substrate 2, but rather would be applied to another surface of layer 4 as illustrated, for example, in FIG. 14. In that case, n+ region 50 should have a thickness of from about 1-20 μm (preferably about 1-5 μm) and is preferably doped at a concentration of about 1E18 cm^{-3}. Such an embodiment is expected to have a lower pad capacitance and therefore a better high frequency performance.

[0048] An embodiment not in accordance with the present invention is illustrated in FIGs 11-13 in which the epitaxial structure 11 shown in FIG. 11 is used as the starting structure- As shown in FIG. 11, structure 11 includes a heavily doped n-type substrate 2 of 4H silicon carbide on which is deposited an n-type epitaxial layer 4, also of silicon carbide. As with the structure shown in FIG. 1, substrate 2 and layer 4 form the collector of the bipolar transistor, and a p-type epitaxial layer 6 is formed on layer 4. Unlike the structure shown in FIG. 1, however, a heavily doped epitaxial layer 7 of n-type conductivity is deposited on layer 6. Layer 7 is doped with a donor dopant such as nitrogen at a concentration of about 1E18 to 1E21 cm^{-3}. Layer 7 has a thickness of approximately 0.05μm to approximately 2μm, and most preferably from about 0.2μm to about 0.5μm.

[0049] The steps for processing structure 10 are similar to that described above with respect to FIGs 1-4, i.e., the structure is coated with an oxide mask which is etched away to form pillars 12 including raised portions 15 formed out of the top epitaxial layer (in this case layer 7), after which oxide layer 18 is formed over the top surface of the structure 10 by, for example, PECVD.

[0050] Following an anisotropic etch of the oxide layer 18, and as illustrated in FIG. 12, heavily doped well regions 21 are formed in the structure such that the edges of well regions 21 are spaced a distance from the pillars 12 approximately equal to the thickness of the oxide layer 18. In the embodiment illustrated in FIGs 11-13, however, the well regions 21 are doped to have a p-type conductivity. In one embodiment, well regions 21 extend through layer 6 and partially into layer 4. Consequently, well regions 21, together with the p-type regions 23 from layer 6, form the base of the transistor.

[0051] The remainder of the processing is similar to that described with respect to FIGs 6-10, except that as shown in FIG. 13, the emitter contacts are formed on exposed surfaces of raised portions 15, while the base contacts are made to the top surfaces of well regions 21.

[0052] As illustrated in FIG. 15, the embodiment described in FIGs 11-13 may be implemented using a nonconductive or semi-insulating substrate, in which case collector contacts 32' to the n-type layer 4 may be made on the top surface of the device over n+ well regions 50 formed in layer 4.

[0053] A preferred technique for performing the etching steps described above comprises reactive ion etching with nitrogen trifluoride (NF_3). Nitrogen trifluoride has demonstrated a number of advantages in silicon carbide etching processes. A more complete discussion of reactive ion etching using NF_3 is provided Palmour et al., Surface Characteristics of Monocrystalline Beta-SiC Dry Etched in Fluorinated Gases, Mat. Res. Soc. Symp. Proc., Vol. 76, 1987, p. 185. Appropriate techniques for etching silicon carbide are also described in U.S. Patents No. 4,865,685 and 4,981,551.

[0054] The invention which has been set forth is a method of fabricating a bipolar junction transistor (BJT) in silicon carbide (all polytypes) as opposed to silicon, gallium arsenide, or other semiconductor materials. The disclosed embodiment aligns the base and emitter contacts of the transistor by means of oxide formation rather than lithographic techniques, permitting closer and more precise positioning of the base and emitter contacts with respect to one another. Because silicon carbide is a wide bandgap semiconductor that has the ability to operate at much higher temperatures than other common semiconductors, transistors fabricated according to the present invention likewise demonstrate superior operating characteristics at high temperatures. Moreover, transistors fabricated according to the present invention also have the ability to operate at higher power levels and higher frequencies. The inventive method can be used to fabricate either n-p-n or p-n-p transistors.

[0055] In the specification and drawings, there has been set forth a preferred and exemplary embodiment of the invention which has been included by way of example and not by way of limitation, the scope of the invention being set forth in the accompanying claims.

Claims

1. A method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure (1, 11) having a first layer (6) of silicon carbide and a second layer (8) of silicon carbide, the method comprising:

   forming a cap layer (10) on the second layer of silicon carbide;
   etching the cap layer and the second layer of silicon carbide (8) to form a pillar (12) having a first surface opposite the first layer of silicon carbide (6) and side walls, and a horizontal surface adjacent the pillar;
   depositing a spacer layer (18) having a predetermined thickness on the first surface of the pillar, the side walls and the horizontal surface adjacent the pillar;
   anisotropically etching the spacer layer from the horizontal surface adjacent the pillar while at least a portion of the spacer layer remains on the side walls of the pillar, thereby exposing the horizontal surface;
   doping a portion (20) of the first layer of silicon carbide below the exposed portion of the horizontal surface with a dopant to create a doped well region in the first layer; and
   removing the portion of the spacer layer remaining on the sidewalls; and

   wherein the first layer (6) and the second layer (8) form a base region and the well region (20) forms an emitter region.

2. A method according to claim 1 further comprising the step of providing ohmic contacts (28, 30) to the base and emitter regions.

3. A method according to any preceding claim wherein said doping step comprises high temperature ion implantation.

4. A method according to any preceding claim further comprising the step of etching a portion of the first layer (6) to form a mesa (24) containing the transistor.

5. A method according to claim 4, further comprising:

   forming an oxide layer on the mesa (24), and anisotropically etching the oxide layer to reveal contact surfaces.

6. A method according to any preceding claim wherein the second layer (8) comprises a layer of heavily doped, p-type silicon carbide.

7. A method according to any preceding claim wherein the spacer layer (18) is deposited to a thickness of between 0.05 and 0.5 μm.

8. A bipolar junction transistor fabricated in silicon carbide, comprising:

   a substrate (2, 4) having a first conductivity type, having a top surface and a bottom surface and forming a collector region of the transistor;
   an epitaxial layer (6) of silicon carbide deposited above the substrate, having a second conductivity type opposite the first conductivity type; and
   a pillar (12) having a top wall and side walls formed above the epitaxial layer, the pillar forming part of a base region of the transistor, **characterised by** a doped well region (20) in the epitaxial layer adjacent the pillar, a distance from the pillar of between 0.05 and 0.5 μm, the doped well region having the first conductivity type and forming the emitter region of the transistor.

Patentansprüche

1. Verfahren zur Herstellung eines selbst-ausgerichteten (engl.: self-aligned) Bipolartransistors in einer Halbleiterstruktur (1, 11), welche eine erste Schicht (6) aus Siliciumcarbid und eine zweite Schicht (8) aus Siliciumcarbid aufweist, wobei das Verfahren umfasst:

   Bilden einer Deckschicht (10) (engl.: cap layer) auf der zweiten Schicht aus Siliciumcarbid;
   Ätzen der Deckschicht und der zweiten Schicht aus Siliciumcarbid (8), um eine Säule (12), welche eine erste Oberfläche, gegenüber der ersten Schicht aus Siliciumcarbid (6), und Seitenwände aufweist, und eine horizontale Oberfläche, angrenzend an die Säule, zu bilden;
   Aufbringen einer Abstandsschicht (18), welche eine vordefinierte Dicke hat, auf die erste Oberfläche der Säule, die Seitenwände und die horizontale Oberfläche, angrenzend an die Säule;
   anisotropes Ätzen der Abstandsschicht von der horizontalen Oberfläche, angrenzend an die Säule, während mindestens ein Teil der Abstandsschicht auf den Seitenwänden der Säule verbleibt, wodurch die horizontale Oberfläche freigelegt wird;
   Dotieren eines Teils (20) der ersten Schicht aus Siliciumcarbid, unterhalb des freigelegten Teils der horizontalen Oberfläche, mit einem Dotiermittel, um einen dotierten Vertiefungsbereich in der ersten Schicht zu erzeugen; und
   Entfernen des Teils der auf den Seitenwänden verbleibenden Abstandsschicht; und
   wobei die erste Schicht (6) und die zweite

Schicht (8) einen Basisbereich bilden und der Vertiefungsbereich (20) einen Emitterbereich bildet.

2. Verfahren nach Anspruch 1, weiterhin umfassend den Schritt des Bereitstellens von ohmschen Kontakten (28, 30) an den Basis- und Emitterbereichen.

3. Verfahren nach einem der vorangehenden Ansprüche, wobei der Dotierungsschritt Hochtemperatur-Ionenimplantation umfasst.

4. Verfahren nach einem der vorangehenden Ansprüche, weiterhin umfassend den Schritt des Ätzens eines Teils der ersten Schicht (6), um eine Mesa (24) zu bilden, welche den Transistor enthält.

5. Verfahren nach Anspruch 4, weiterhin umfassend Bilden einer Oxidschicht auf der Mesa (24) und anisotropes Ätzen der Oxidschicht, um Kontaktoberflächen freizulegen.

6. Verfahren nach einem der vorangehenden Ansprüche, wobei die zweite Schicht (8) eine Schicht von stark dotiertem p-Typ Siliciumcarbid enthält.

7. Verfahren nach einem der vorangehenden Ansprüche, wobei die Abstandsschicht (18) auf eine Dicke von zwischen 0,05 und 0,5 μm aufgebracht wird.

8. Bipolartransistor, hergestellt in Siliciumcarbid, umfassend:

ein Substrat (2, 4), welches einen ersten Leitfähigkeitstyp aufweist, welches eine obere Oberfläche und eine untere Oberfläche hat und einen Kollektorbereich des Transistors bildet;
eine Epitaxialschicht (6) aus Siliciumcarbid, aufgebracht oberhalb des Substrats, welche einen zweiten Leitfähigkeitstyp aufweist, entgegengesetzt zu dem ersten Leitfähigkeitstyp; und
eine Säule (12), welche eine obere Wand und Seitenwände, gebildet oberhalb der Epitaxialschicht, aufweist, wobei die Säule einen Teil einer Basisregion des Transistors bildet, **gekennzeichnet durch** einen dotierten Vertiefungsbereich (20) in der Epitaxialschicht, angrenzend an die Säule, einen Abstand von der Säule von zwischen 0,05 und 0,5 μm, wobei der dotierte Vertiefungsbereich den ersten Leitfähigkeitstyp aufweist und den Emitterbereich des Transistors bildet.

Revendications

1. Procédé de fabrication d'un transistor à jonction bipolaire auto-aligné dans une structure semi-conductrice (1, 11) comportant une première couche (6) de carbure de silicium et une deuxième couche (8) de carbure de silicium, le procédé comprenant :

la formation d'une couche d'encapsulation (10) sur la deuxième couche de carbure de silicium ;
la gravure de la couche d'encapsulation et de la deuxième couche de carbure de silicium (8) pour former un pilier (12) ayant une première surface face à la première couche de carbure de silicium (6) et des parois latérales, et une surface horizontale adjacente au pilier ;
le dépôt d'une couche d'espacement (18) ayant une épaisseur prédéterminée sur la première surface du pilier, les parois latérales et la surface horizontale adjacente au pilier ;
la gravure anisotrope de la couche d'espacement à partir de la surface horizontale adjacente au pilier tandis qu'au moins une partie de la couche d'espacement reste sur les parois latérales du pilier, exposant de ce fait la surface horizontale ;
le dopage d'une partie (20) de la première couche de carbure de silicium au-dessous de la partie exposée de la surface horizontale avec un dopant pour créer une région de puits dopée dans la première couche ; et
le retrait de la partie de la couche d'espacement restant sur les parois latérales ; et
dans lequel la première couche (6) et la deuxième couche (8) forment une région de base et la région de puits (20) forme une région d'émetteur.

2. Procédé selon la revendication 1, comprenant en outre l'étape de prévision de contacts ohmiques (28, 30) sur les régions de base et d'émetteur.

3. Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite étape de dopage comprend une implantation ionique à température élevée.

4. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape de gravure d'une partie de la première couche (6) pour former une mésa (24) contenant le transistor.

5. Procédé selon la revendication 4, comprenant en outre :

la formation d'une couche d'oxyde sur la mésa (24), et
la gravure anisotrope de la couche d'oxyde pour révéler les surfaces de contact.

6. Procédé selon l'une quelconque des revendications précédentes, dans lequel la deuxième couche (8)

comprend une couche de carbure de silicium de type p fortement dopée.

7. Procédé selon l'une quelconque des revendications précédentes, dans lequel la couche d'espacement (18) est déposée en une épaisseur entre 0,05 et 0,5 μm.

8. Transistor à jonction bipolaire fabriqué en carbure de silicium, comprenant :

un substrat (2, 4) ayant un premier type de conductivité, comportant une surface supérieure et une surface inférieure et formant une région de collecteur du transistor ;
une couche épitaxiale (6) de carbure de silicium déposée au-dessus du substrat, ayant un deuxième type de conductivité opposé au premier type de conductivité ; et
un pilier (12) comportant une paroi supérieure et des parois latérales formé au-dessus de la couche épitaxiale, le pilier constituant une partie d'une région de base du transistor, **caractérisé par** une région de puits dopée (20) dans la couche épitaxiale adjacente au pilier, une distance par rapport au pilier entre 0,05 et 0,5 μm, la région de puits dopée ayant le premier type de conductivité et formant la région d'émetteur du transistor.

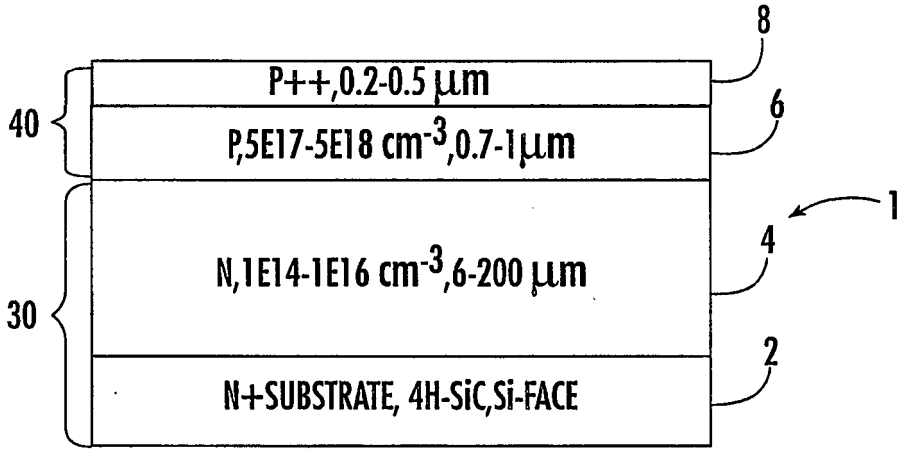
8
P++,0.2-0.5 µm
6
40
P,5E17-5E18 cm-3,0.7-1µm
1
4
N,1E14-1E16 cm-3,6-200 µm
30
2
N+SUBSTRATE, 4H-SiC,Si-FACE

FIG. 1.

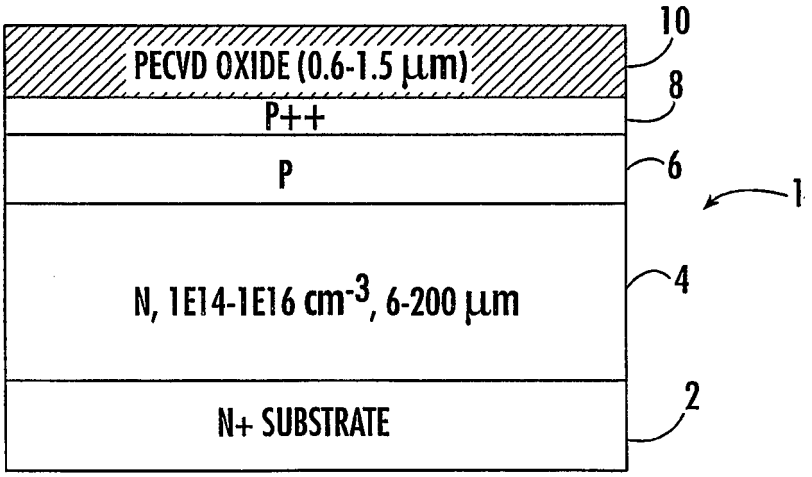
10
PECVD OXIDE (0.6-1.5 µm)
8
P++
6
P
1
4
N, 1E14-1E16 cm-3, 6-200 µm
2
N+ SUBSTRATE

FIG. 2.

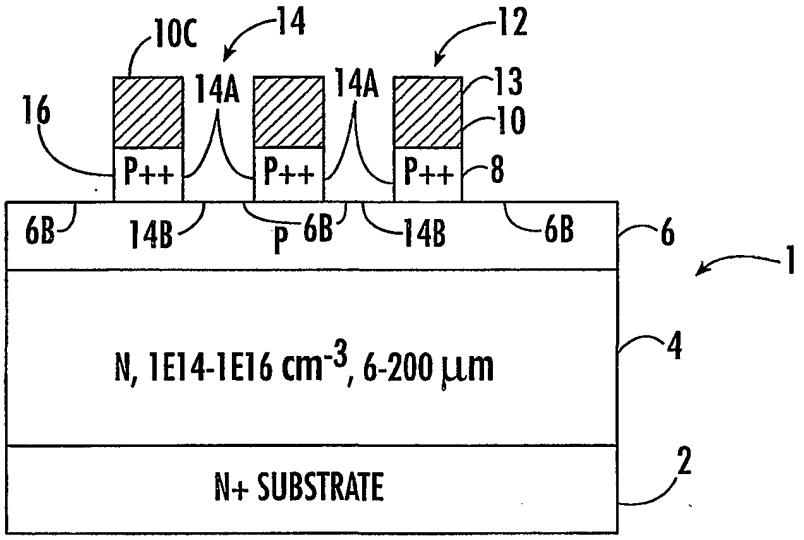

FIG. 3.

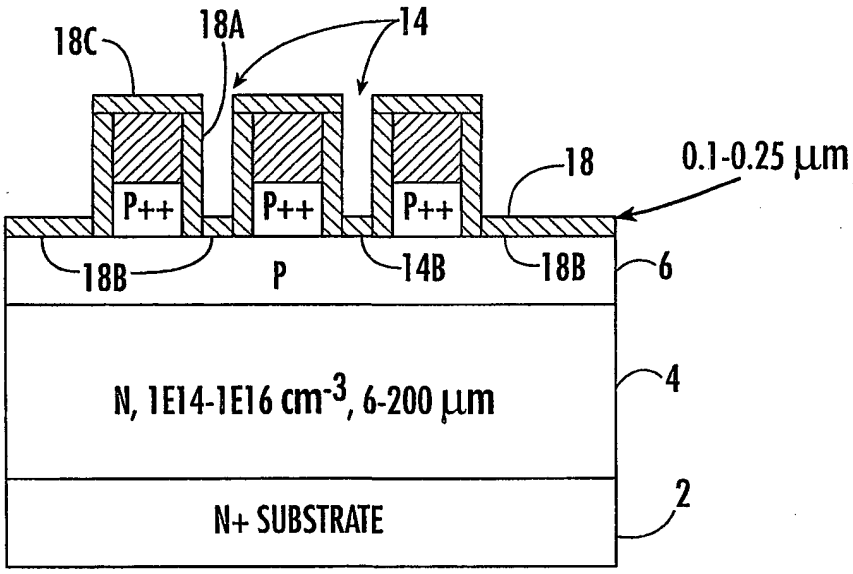

FIG. 4.

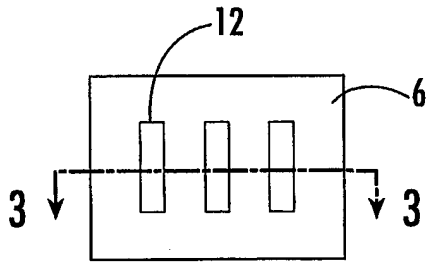

FIG. 3A.

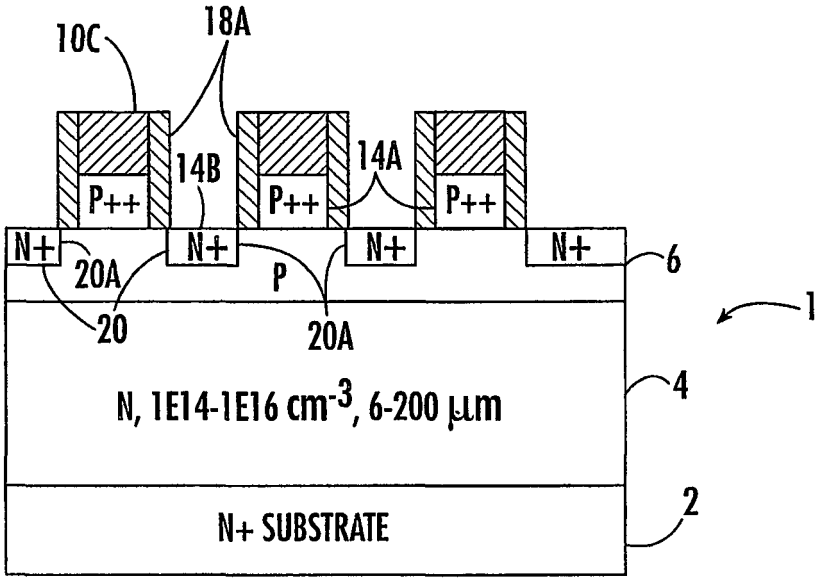
10C
18A
14B
14A
P++
P++
P++
N+
N+
N+
N+
6
20A
20
P
20A
1
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2

FIG. 5.

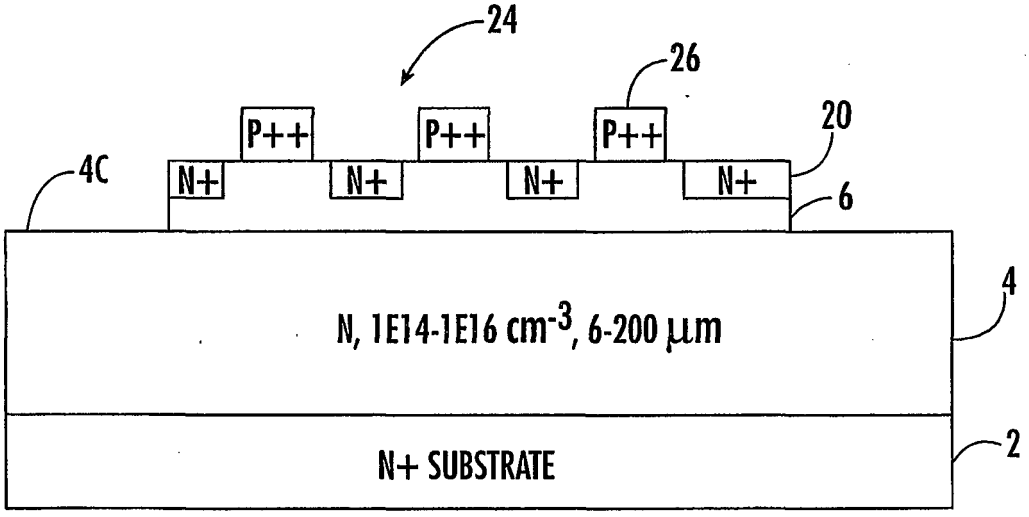
24
26
P++
P++
P++
20
4C
N+
N+
N+
N+
6
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2

FIG. 6.

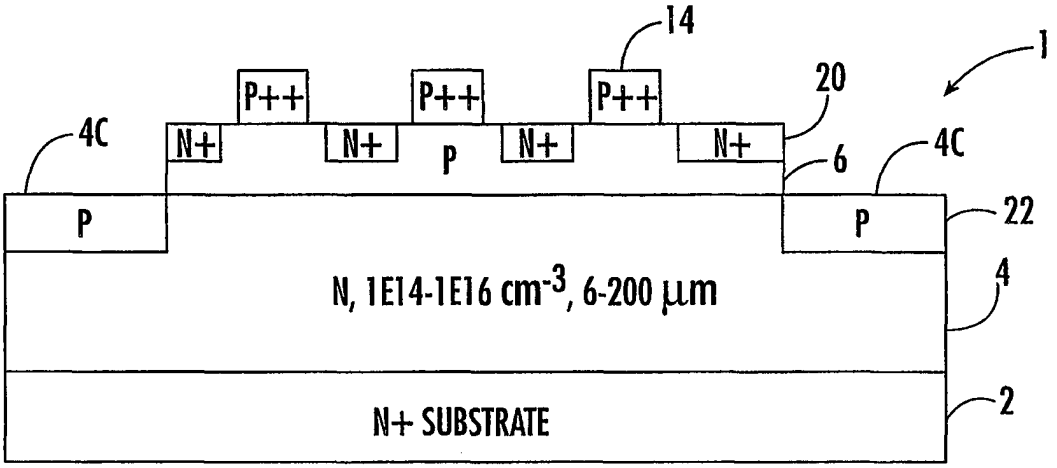
14
1
20
P++
P++
P++
4C
N+
N+
P
N+
N+
6
4C
P
P
22
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2

FIG. 7.

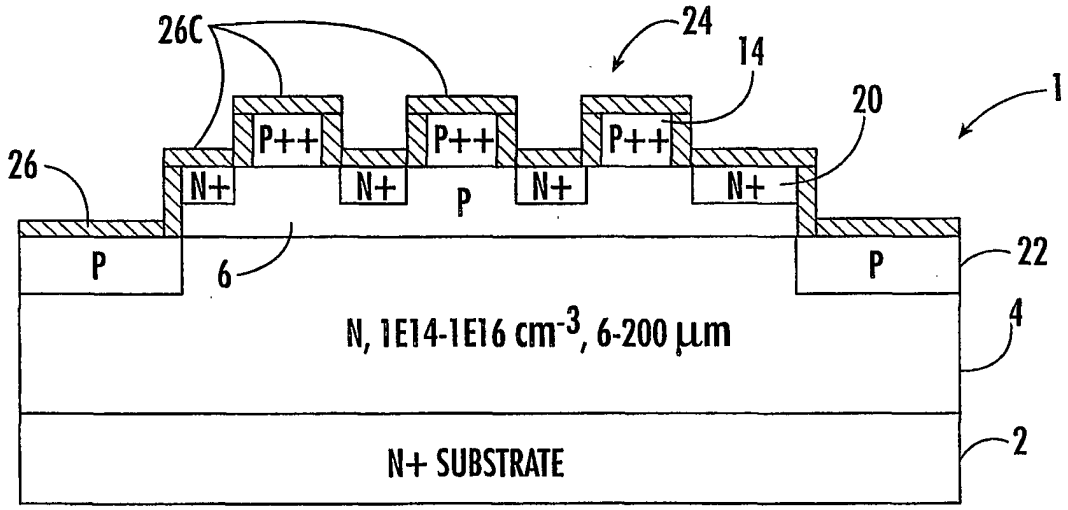
26C
24
14
1
20
P++
P++
P++
26
N+
N+
P
N+
N+
P
6
P
22
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2

FIG. 8.

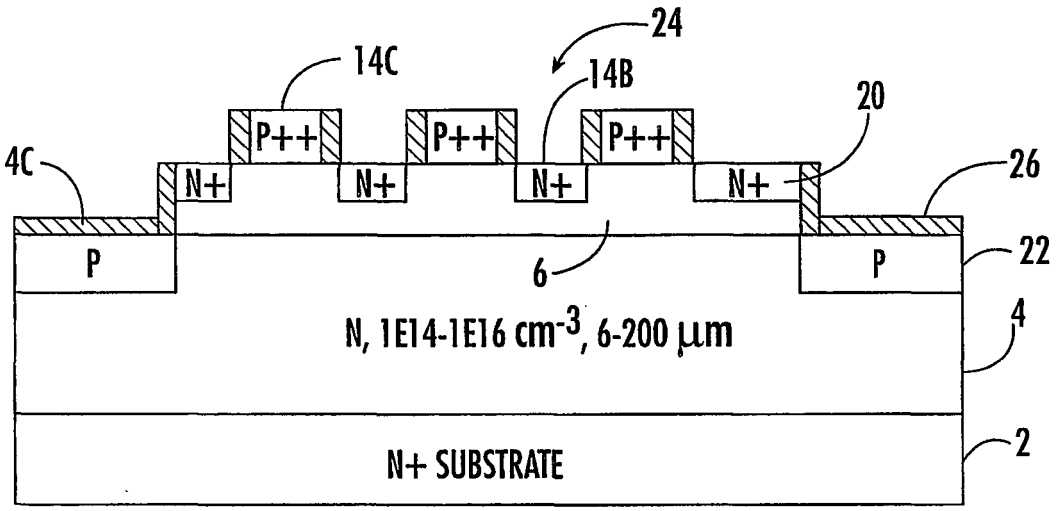
24
14C
14B
20
4C
P++
P++
P++
N+
N+
N+
N+
26
P
P
22
6
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2

FIG. 9.

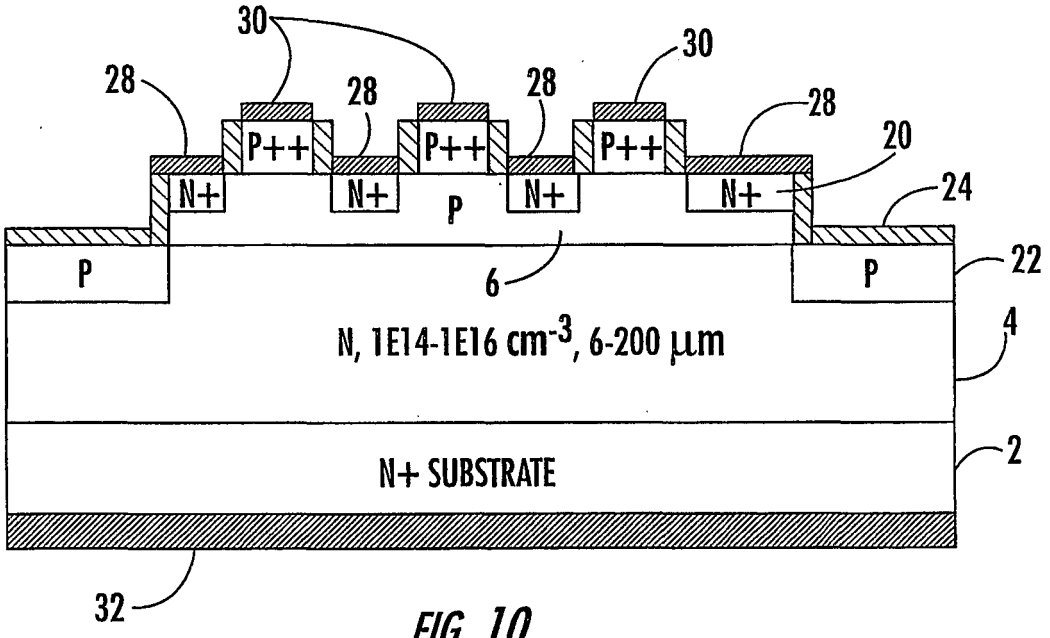
30
30
28
28
28
28
P++
P++
P++
20
N+
N+
P
N+
N+
24
P
P
22
6
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2
32

FIG. 10.

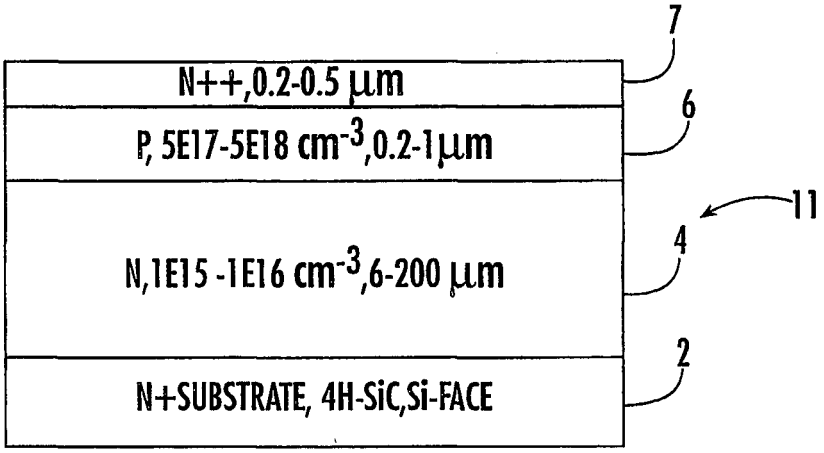
7
N++,0.2-0.5 µm
6
P, 5E17-5E18 cm-3,0.2-1µm
11
4
N,1E15 -1E16 cm-3,6-200 µm
2
N+SUBSTRATE, 4H-SiC,Si-FACE

FIG. 11.

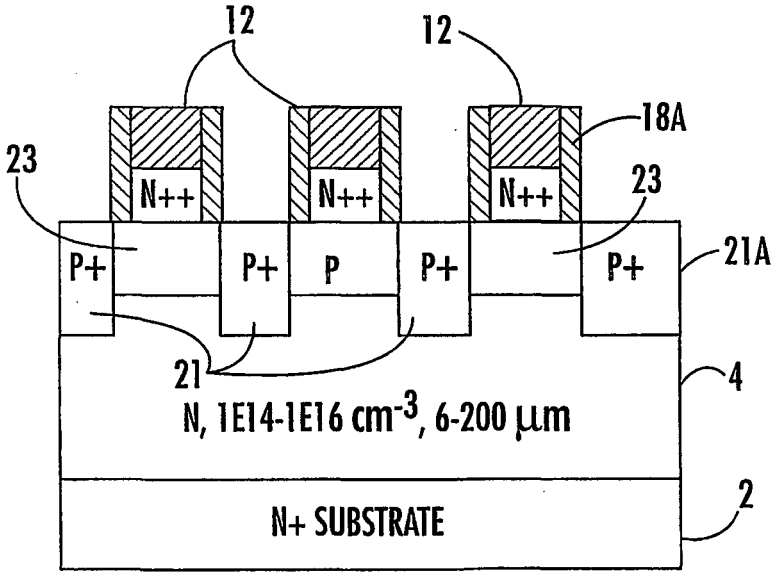
12
12
18A
23
23
N++
N++
N++
P+
P+
P
P+
P+
21A
21
4
N, 1E14-1E16 cm-3, 6-200 µm
2
N+ SUBSTRATE

FIG. 12.

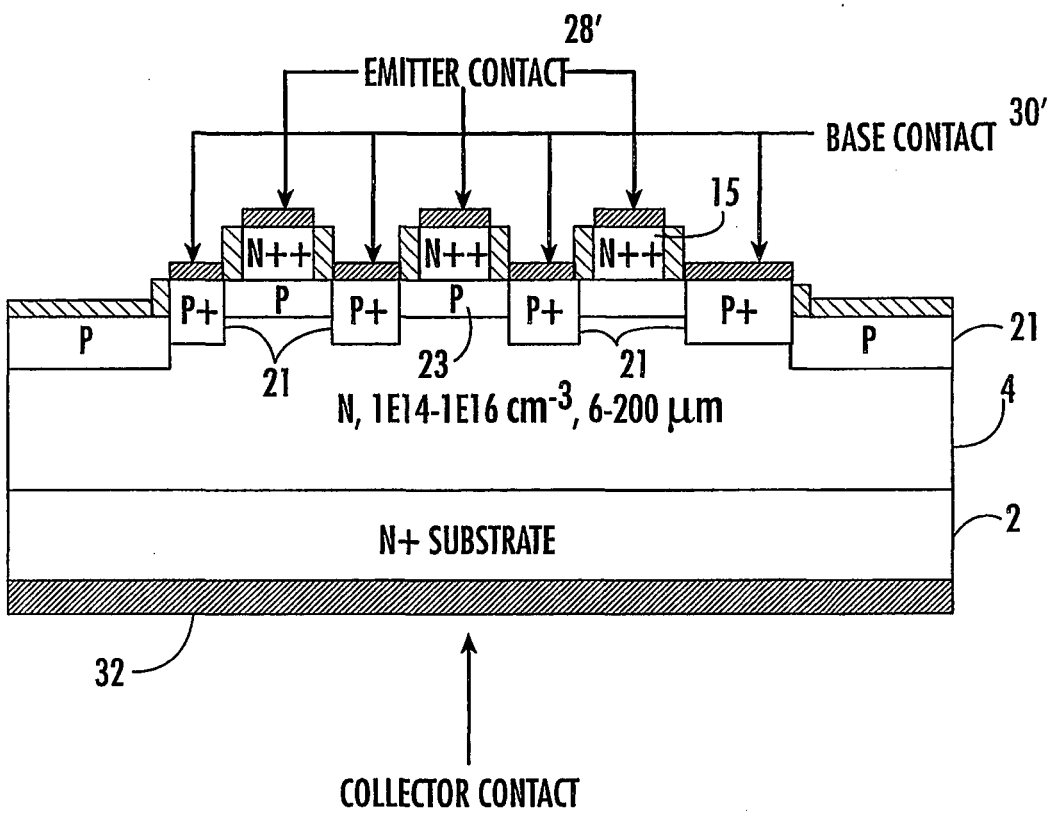
28'
EMITTER CONTACT
BASE CONTACT
30'
15
N++
N++
N++
P+
P
P+
P
P+
P+
P
P
21
21
23
21
N, 1E14-1E16 cm-3, 6-200 µm
4
N+ SUBSTRATE
2
32
COLLECTOR CONTACT

FIG. 13.

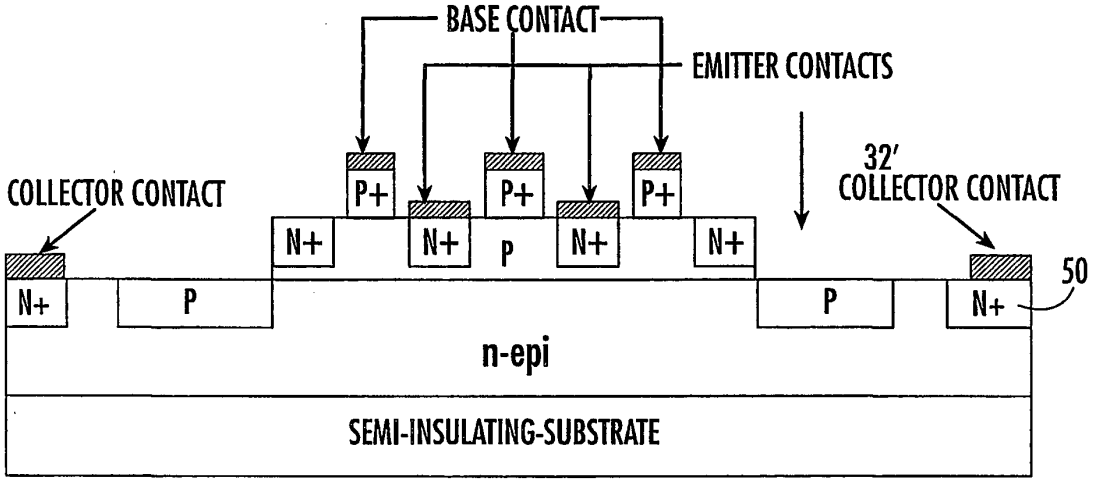
BASE CONTACT
EMITTER CONTACTS
32'
COLLECTOR CONTACT
COLLECTOR CONTACT
P+
P+
P+
N+
N+
P
N+
N+
N+
P
P
N+
50
n-epi
SEMI-INSULATING-SUBSTRATE

FIG. 14.

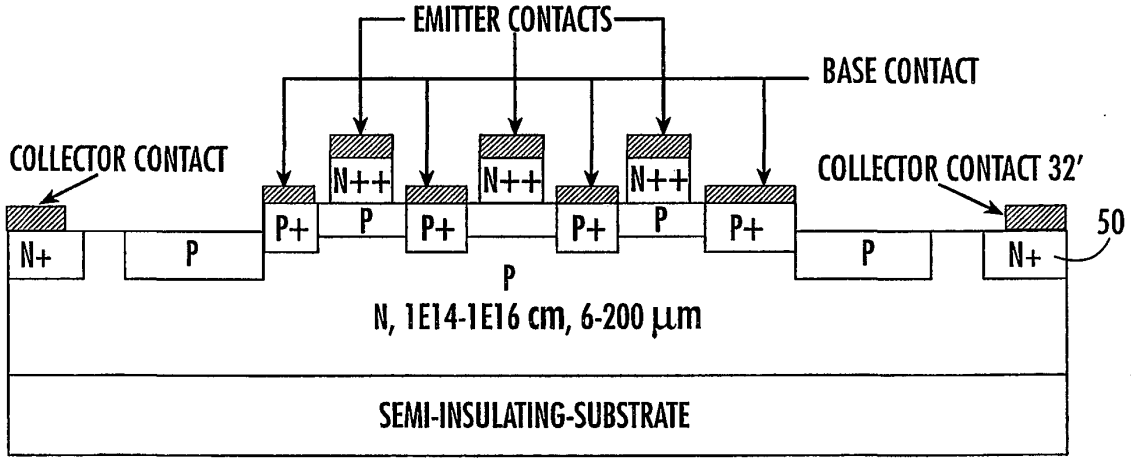
EMITTER CONTACTS
BASE CONTACT
COLLECTOR CONTACT
COLLECTOR CONTACT 32'
N++
N++
N++
P+
P
P+
P+
P
P+
N+
P
P
N+
50
P
N, 1E14-1E16 cm, 6-200 µm
SEMI-INSULATING-SUBSTRATE

FIG. 15.

REFERENCES CITED IN THE DESCRIPTION

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